4.8 GHz Ultrahigh Dynamic Range, Dual Differential Amplifier

Preliminary Technical Data

ADL5567

FEATURES

–3 dB bandwidth of 4.8 GHz (A_V = 20 dB)
Fixed 20 dB gain
Channel-to-channel gain error: TBD at 100 MHz
Channel-to-channel phase error: TBD at 100 MHz
Differential or single-ended input to differential output
I/O dc-coupled or ac-coupled
Low noise input stage: 1.2 nV/√Hz RTI at A_V = 20 dB
Low broadband distortion (A_V = 20 dB), supply = 5 V
10 MHz: –93dBc (HD2), –97dBc (HD3)
100 MHz: –94 dBc (HD2), –100 dBc (HD3)
200 MHz: –94 dBc (HD2),-104dBc (HD3)
500 MHz: –83dBc (HD2), -85 dBc (HD3)
IMD3 of -102 dBc at 200 MHz center
Low single-ended input distortion to 500 MHz
Slew rate: 20 V/ns
Maintains low distortion down to 1.2 V VCOM
Fixed 20 dB gain can be reduced by adding external resistors
Single-supply operation: 2.8 V to 5.2 V
Power down
Low dc power consumption, 455mW at 3.3 V supply
Low Power modes for 5V and 3.3v Supplies

APPLICATIONS

Differential ADC drivers
Single-ended-to-differential conversion
RF/IF gain blocks
SAW filter interfacing

FUNCTIONAL BLOCK DIAGRAM

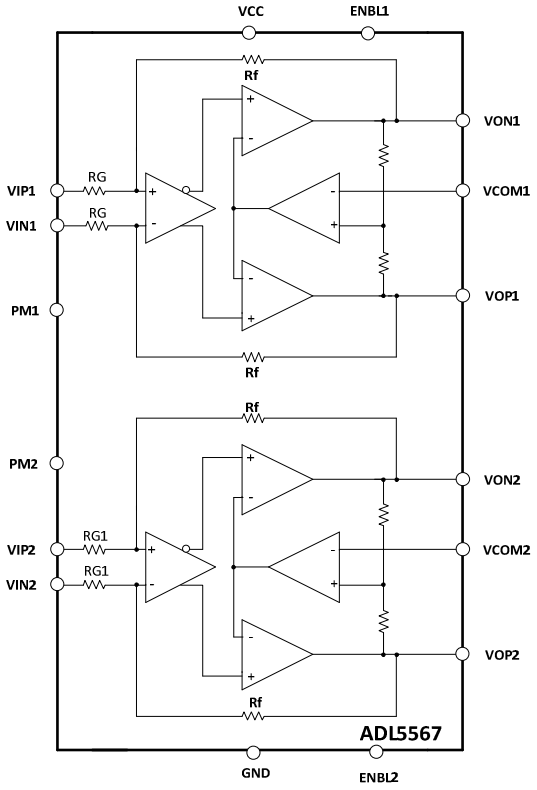

Figure 1.

GENERAL DESCRIPTION

The ADL5567 is a high performance, dual differential amplifier optimized for IF and dc applications. The amplifier offers low noise of 1.2 nV/√Hz and excellent distortion performance over a wide frequency range, making it an ideal driver for high speed 16-bit analog-to-digital converters (ADCs). The ADL5567 is ideally suited for use in high performance zero IF/complex IF receiver designs. In addition, this device has excellent low distortion for single-ended input drive applications.

The ADL5567 provides a gain of 20 dB. For the single-ended input configuration, the gain is reduced to 18 dB. Using two external series resistors for each amplifier expands the gain flexibility of the amplifier and allows for any gain selection from 0 dB to 20 dB for a differential input and 0 dB to 18 dB for a single-ended input. In addition, this device maintains low distortion down to output (VOCM) levels of 1.2 V; therefore, providing an added capability for driving CMOS ADCs at ac levels up to 2 V p-p.

The quiescent current of the ADL5567 using a 5 V supply is typically 74 mA, per amplifier. When disabled, it consumes less than 3.5 mA per amplifier and has –25 dB of input-to-output isolation at 100 MHz.

The device is optimized for wideband, low distortion, and noise performance, giving it unprecedented performance for overall spurious-free dynamic range (SFDR). These attributes, together with its adjustable gain capability, make this device the amplifier of choice for driving a wide variety of ADCs, mixers, pin diode attenuators, SAW filters, and multi-element discrete devices.

Fabricated on an Analog Devices, Inc., high speed SiGe process, the ADL5567 is supplied in a compact 4 mm × 4 mm, 24-lead LFCSP package and operates over the –40°C to +85°C temperature

Rev. PrB **Document Feedback**

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TABLE OF CONTENTS

Features 1
Applications 1
Functional Block Diagram 1
General Description 1
Specifications 3
Absolute Maximum Ratings 6
Thermal Resistance 6
ESD Caution 6
Pin Configuration and Function Descriptions 7
Typical Performance Characteristics 9
Circuit Description 13
Applications Information 14
Basic Connections 14
Input and Output Interfacing 15
Gain Adjustment and Interfacing 16
Layout Considerations 17
Soldering Information and Recommended Land Pattern 18
Evaluation Board 19
Outline Dimensions 21
Ordering Guide ..... **Error! Bookmark not defined.**

SPECIFICATIONS

V_S = 3.3 V, V_{CM} = 1.65 V, V_S = 5 V, V_{CM} = 2.5 V, R_L = 200 Ω differential, A_V = 20 dB, C_L = 1 pF differential, f = 100 MHz, T_A = 25°C, parameters specified ac-coupled differential input and differential output, unless otherwise noted.

Table 1.

	Test Conditions/	3.3 V			5 V			
Parameter	**Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE								
−3 dB Bandwidth	A_V = 20 dB, V_{OUT} ≤ 0.5 V p-p		4.8			4.8		GHz
Bandwidth 0.1 dB Flatness	V_{OUT} ≤ 1.0 V p-p		TBD			TBD		MHz
Gain Accuracy			TBD			TBD		dB
Gain Error	≤1000 MHz, Channel A to Channel B		TBD			TBD		dB
Phase Error	≤1000 MHz, Channel A to Channel B		TBD			TBD		Degrees
Gain Supply Sensitivity	V_S ± 5%		TBD			TBD		mdB/V
Gain Temperature Sensitivity	−40°C to +85°C		TBD			TBD		mdB/°C
Slew Rate	Rise, A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V step		20			20		V/ns
	Fall, A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V step		20			20		V/ns
Settling Time	2 V step to 1%		380			380		ps
Overdrive Recovery Time	V_{IN} = 4 V to 0 V step, V_{OUT} ≤ ±10 mV		780			780		ns
Reverse Isolation (S12)			57			57		dB
Channel Isolation	Channel A-to-Channel B A_V = 20 dB		75			75		dB
INPUT/OUTPUT CHARACTERISTICS								
Input Common-Mode Range		1.2		1.8	1.3		3.5	V
Input Resistance (Differential)	A_V = 20 dB		100			100		Ω
Input Resistance (Single-Ended)	A_V = 18dB		TBD			TBD		Ω
Input Capacitance (Single-Ended)			TBD			TBD		pF
Input Bias Current			TBD			TBD		µA
CMRR			TBD			TBD		dB
Output Common-Mode Range		1.25		1.8	1.25		3	V
Output Common-Mode Offset	Referenced to VCC/2	−100		+20	−100		+20	mV
Output Common-Mode Drift	−40°C to +85°C		TBD			TBD		mV/°C
Output Differential Offset Voltage		−20		+20	−20		+20	mV
Output Differential Offset Drift	−40°C to +85°C		TBD			TBD		mV/°C
Output Resistance (Differential)			10			10		Ω
Maximum Output Voltage Swing	1 dB compressed		3.4			5		V p-p
POWER INTERFACE								
Supply Voltage		3.15	3.3	3.45	4.75	5	5.25	V
Digital Input V_{IH}	ENBL1/ENBL2,PM1/PM2	2.1		3.45	2.1		3.45	V
Digital Input V_{IL}		-0.3		1.0	-0.3		1.0	V
ENBL1/ENBL2 Input Bias Current	ENBL high		500			500		nA
	ENBL low		−165			−165		µA
High Power Quiescent Current (PM = 0)	ENBL high		138	150		148	160	mA
	ENBL low		7			9		mA
Low Powe Quiescent Current (PM = 1)	ENBL high		80			85		mA
	ENBL low		7			9		mA

Parameter	Test Conditions/ Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
NOISE/HARMONIC PERFORMANCE								
10 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		-92 / -90			-93 / -97		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		43/ -90			45 / -94		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		91.7 / -93.7			93/ -95		dBm/dBc
1 dB Compression Point, RTO (OP1dB)	A_V = 20 dB		12.7			16.5		dBm
Noise Spectral Density, RTI (NSD)	A_V = 20 dB		1.21			1.23		nV/√Hz
Noise Figure (NF)	A_V = 20 dB		6.7			6.8		dB
100 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		-94 / -85			-94/ -100		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		43.3 / -91			47/ -98		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		91.7 / -93.7			92.5/ -94.5		dBm/dBc
1 dB Compression Point, RTO (OP1dB)	A_V = 20 dB		12.6			16.5		dBm
Noise Spectral Density, RTI (NSD)	A_V = 20 dB		1.25			1.26		nV/√Hz
Noise Figure (NF)	A_V = 20 dB		6.9			7		dB
200 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		-94 / -79			-94 / -104		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		43.4 / -91			49 / -102		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		89.5 / -91.5			91.2 / -93.2		dBm/dBc
1 dB Compression Point, RTO (OP1dB)	A_V = 20 dB		12.5			16.2		dBm
Noise Spectral Density, RTI (NSD)	A_V = 20 dB		1.21			1.23		nV/√Hz
Noise Figure (NF)	A_V = 20 dB		6.7			6.8		dB
500 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		-80 / -70			-83/ -85		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		38 / -80			44 / -92		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		75.4 / -77.4			77.7 / -79.7		dBm/dBc
Noise Spectral Density,	A_V = 20 dB		1.19			1.23		nV/√Hz

Parameter	Test Conditions/ Comments	3.3 V Min	3.3 V Typ	3.3 V Max	5 V Min	5 V Typ	5 V Max	Unit
RTI (NSD)								
Noise Figure (NF)	A_V = 20 dB		6.6			6.8		dB
1000 MHz								
Second/Third Harmonic Distortion (HD2/HD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p		-64 / -56			-68 / -61		dBc
Output IP3/Third-Order Intermodulation Distortion (OIP3/IMD3)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		33.5 / -71			36.5/-77		dBm/dBc
Output IP2 Second-Order Intermodulation Distortion (OIP2/IMD2)	A_V = 20 dB, R_L = 200 Ω, V_{OUT} = 2 V p-p composite (2 MHz spacing)		62/ -64			66.5/ -68.5		dBm/dBc
Noise Spectral Density, RTI (NSD)	A_V = 20 dB		1.89			1.89		nV/√Hz
Noise Figure (NF)	A_V = 20 dB		10			10		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Output Voltage Swing X Bandwidth Product, High Performance Mode	5V-GHz
Output Voltage Swing X Bandwidth Product, Low Power Mode	3V-GHz
Supply Voltage, V_{CC}	5.25 V
VIPx, VINx	V_{CC} + 0.5 V
$\pm I_{OUT}$ Maximum	±30 mA
Internal Power Dissipation	900 mW
Maximum Junction Temperature	135°C
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3 lists the junction-to-air thermal resistance (θ_{JA}) and the junction-to-paddle thermal resistance (θ_{JC}) for the ADL5567.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
24-Lead LFCSP	34.0	1.8	°C/W

[1] Measured on Analog Devices evaluation board. For more information about board layout, see the Soldering Information and Recommended Land Patternsection.
[2] Based on simulation with JEDEC standard JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

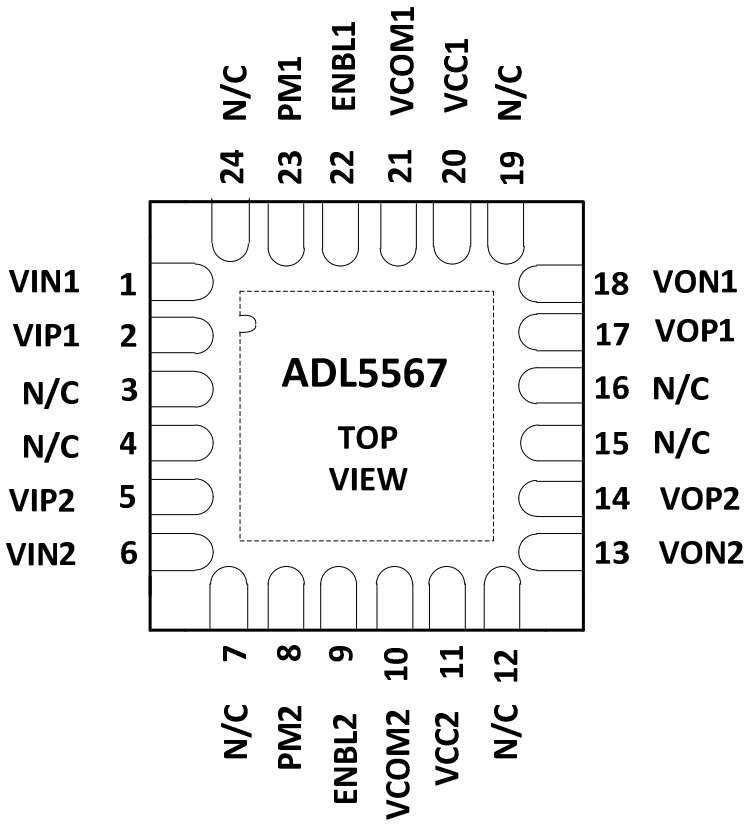


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN1	Balanced Differential Input for Amplifier 1. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 20 dB.
2	VIP1	Balanced Differential Input for Amplifier 1. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 20 dB.
3, 4, 7,12, 15, 16, 19, 24	NC	No Connect. Solder to ground.
5	VIP2	Balanced Differential Input for Amplifier 2. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 20 dB.
6	VIN2	Balanced Differential Input for Amplifier 2. Biased to $V_{CC}/2$, typically ac-coupled. Input for A_V = 20 dB.
8	PM2	Power mode control for Amplifier 2. A low on the pin is high performance and a high(1.6V<PM2<3.3V) is low power.
9	ENBL2	Enable for Amplifier 2. Apply positive voltage (1.6 V < ENBL2 < 3.3V) to activate device.
10	VCOM2	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of Amplifier 2. If left open, VCOM2 = $V_{CC}/2$. Typically, it is decoupled to ground with a 0.1 µF capacitor.
11	VCC2	Positive Supply for Amplifier 2.

13	VON2	Balanced Differential Output for Amplifier 2. Biased to V_{CC}/2, typically ac-coupled.
14	VOP2	Balanced Differential Output for Amplifier 2. Biased to V_{CC}/2, typically ac-coupled.
17	VOP1	Balanced Differential Output for Amplifier 1. Biased to V_{CC}/2, typically ac-coupled.
18	VON1	Balanced Differential Output for Amplifier 1. Biased to V_{CC}/2, typically ac-coupled.
20	VCC1	Positive Supply for Amplifier 1.
21	VCOM1	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of Amplifier 1. If left open, VCOM1 = V_{CC}/2. Typically, it is decoupled to ground with a 0.1 µF capacitor.
22	ENBL1	Enable for Amplifier 1. Apply positive voltage (1.6 V < ENBL1 < 3.3V) to activate device.
	EP	The exposed paddle is internally connected to GND and must be soldered to a low impedance ground plane.
23	PM1	Power mode control for Amplifier 1. A low on the pin is high power and high(1.6V<PM1<3.3V) is low power.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, V_{CM} = 2.5 V, R_L = 200 Ω differential, A_V = 20 dB, C_L = 1 pF differential, f = 100 MHz, T_A = 25°C, parameters specified ac-coupled differential input and differential output, unless otherwise noted.

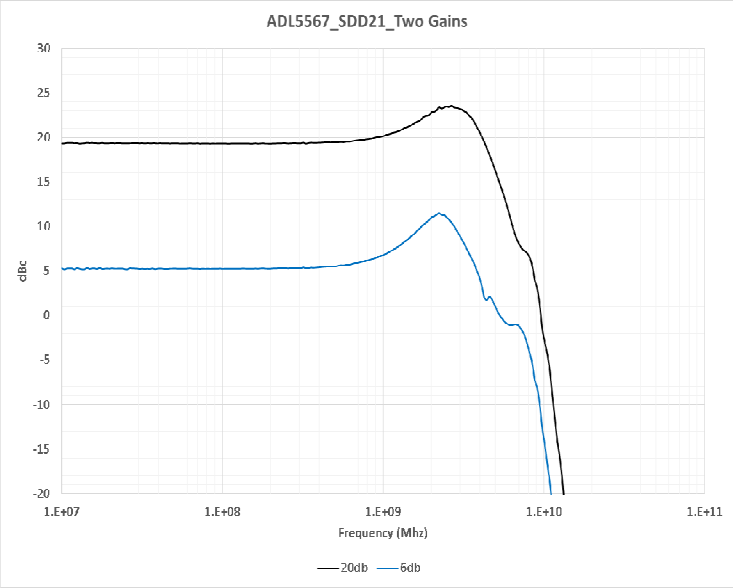


Figure 3. Gain vs. Frequency Response: Two Gains

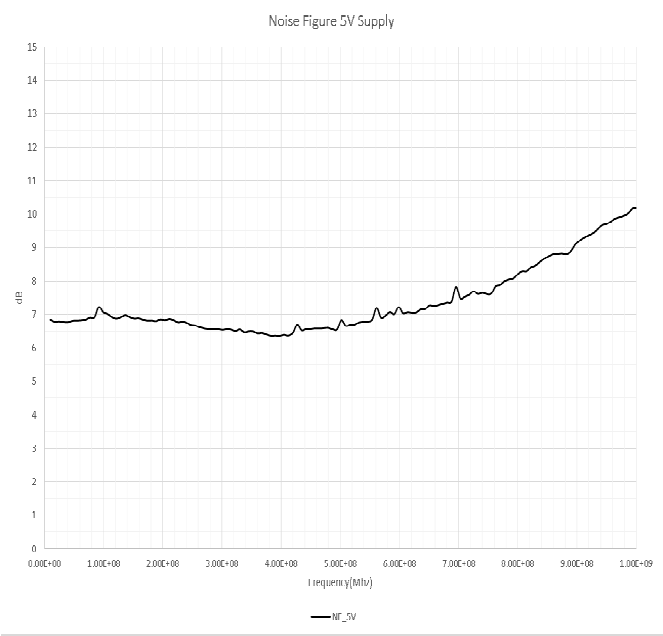


Figure 4. Noise Figure vs. Frequency: 5V supply, Av=20dB

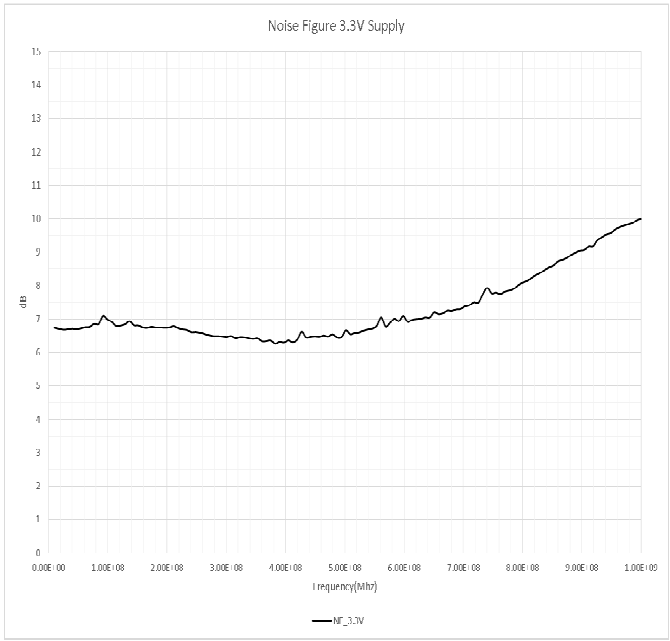


Figure 5. Noise Figure vs. Frequency: 3.3V supply, Av=20dB

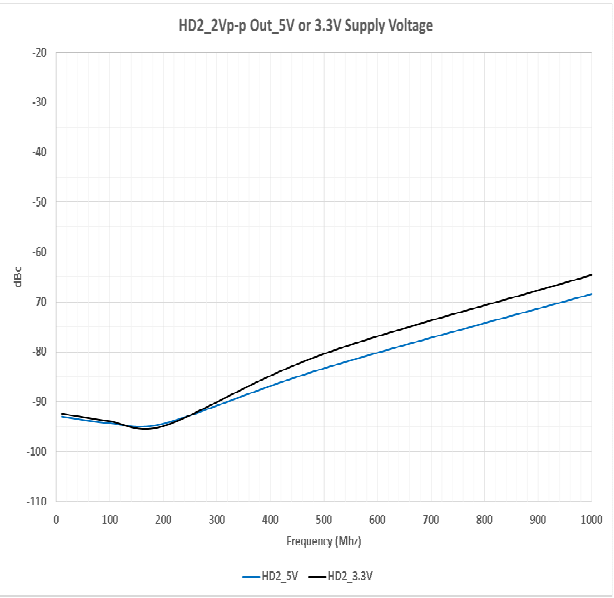


Figure 6. HD2: 2Vp-p Out into 200 ohms,Two Supplies

High Power Mode

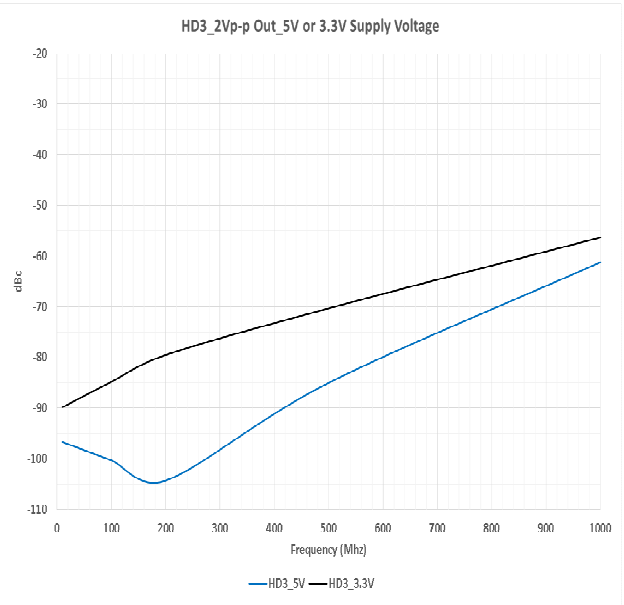


Figure 7. HD3: 2Vp-p Out into 200ohms, Two supplies

High Power Mode

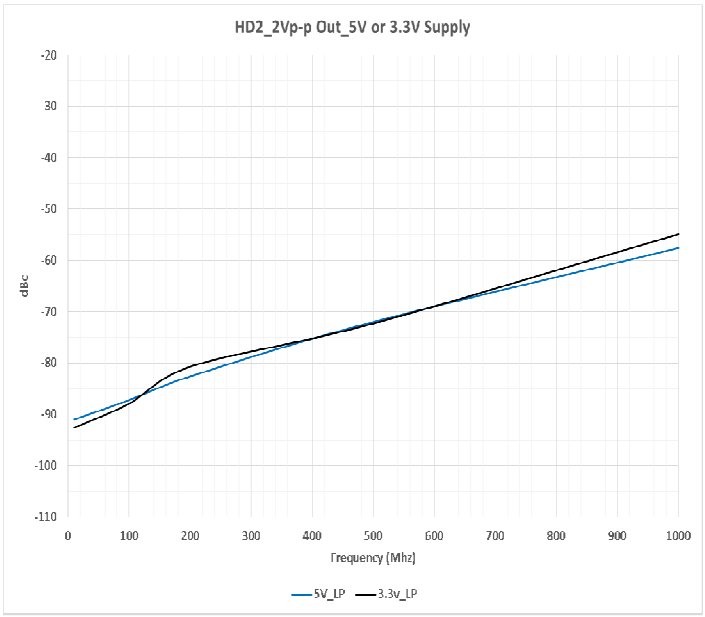


Figure 8. HD2: 2Vp-p Out into 200 ohms,Two Supplies

Low Power Mode

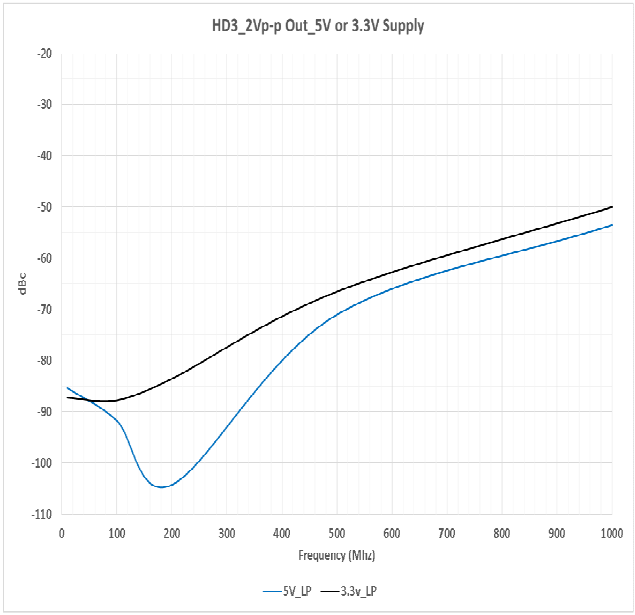


Figure 9. HD3: 2Vp-p Out into 200ohms, Two supplies

Low Power Mode

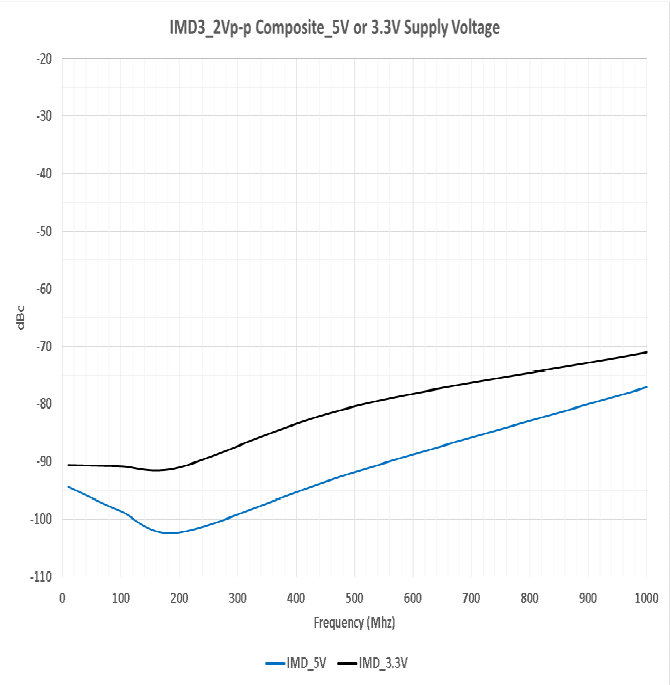


Figure 10. IMD3: 2Vp-p Composite, Two supplies

High Power Mode

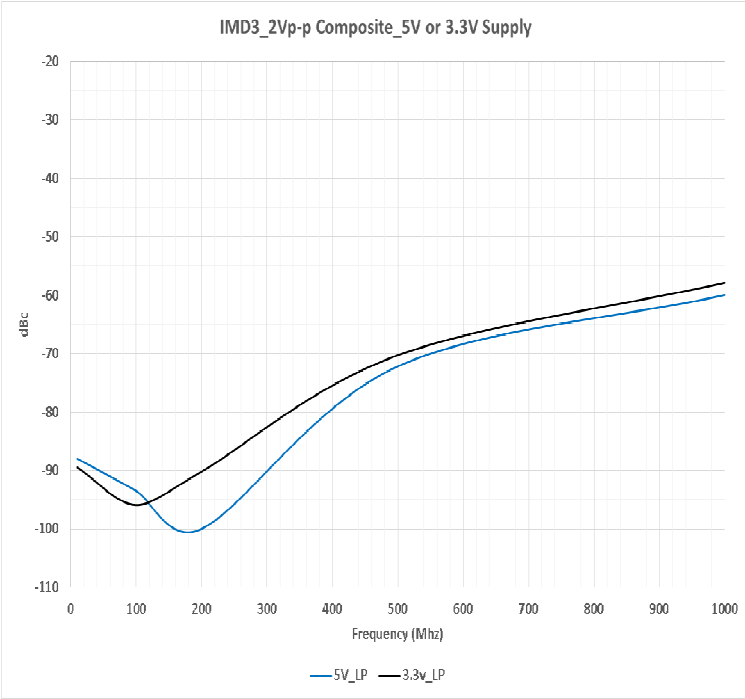


Figure 12. IMD3: 2Vp-p Composite, Two supplies

Low Power Mode

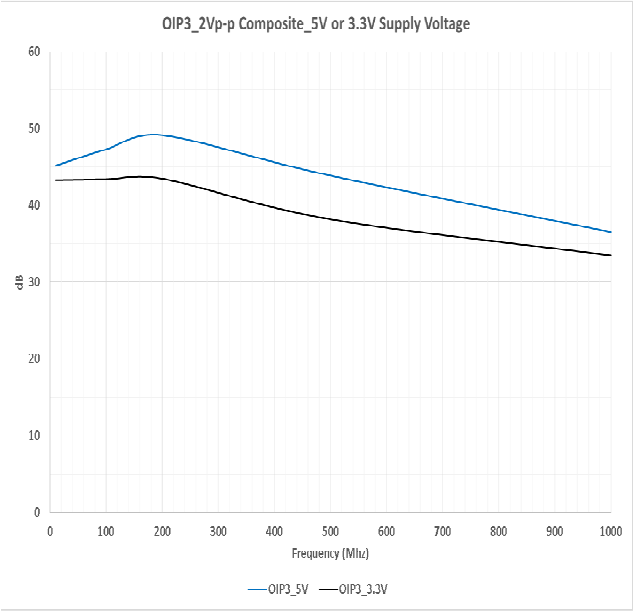


Figure 11. OIP3: 2Vp-p Composite, Two supplies

High Power Mode

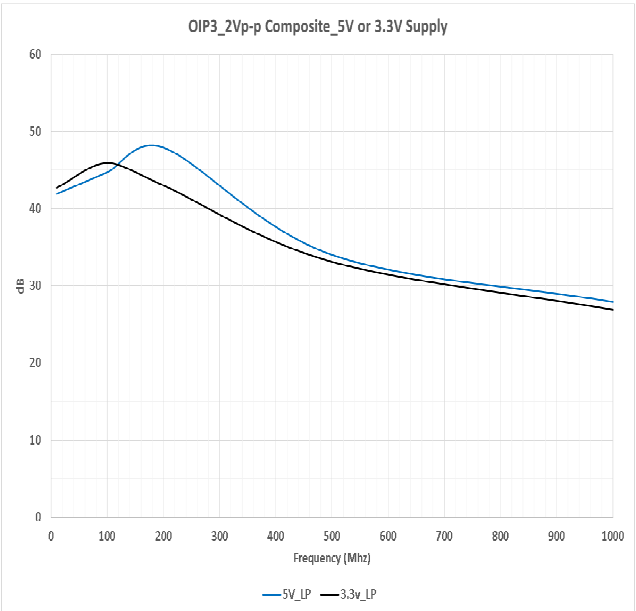


Figure 13. OIP3: 2Vp-p Composite, Two supplies

Low Power Mode

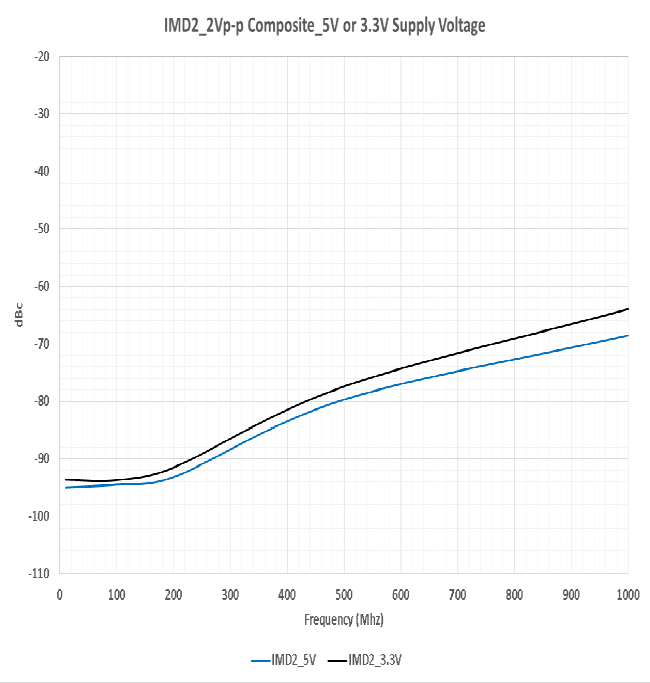


Figure 14. IMD2: 2Vp-p Composite, Two supplies

High Power Mode

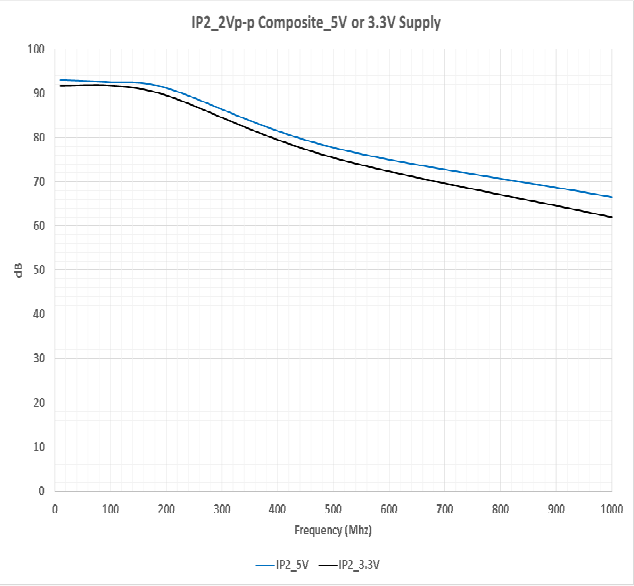


Figure 15. IP2: 2Vp-p Composite, Two supplies

High Power Mode

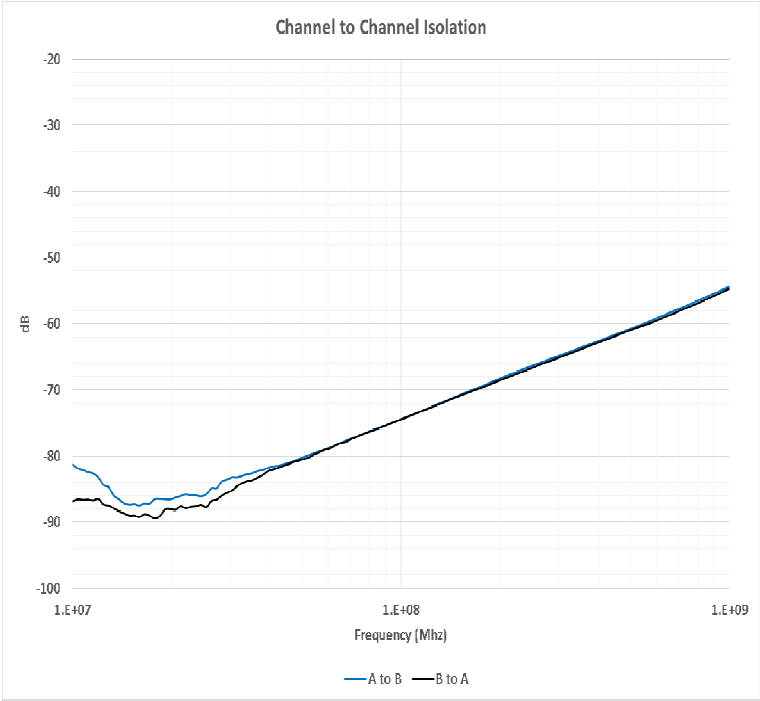


Figure 16. Channel to channel Isolation

High Power Mode

CIRCUIT DESCRIPTION

The ADL5567 is high gain fully differential dual amplifier/ADC driver that uses a 2.8 V to 5 V supply. It provides a 20 dB gain that can be reduced by adding external series resistors. The 3 dB bandwidth is 4.8 GHz, and it has a differential input impedance of 100 Ω. It has a differential output impedance of 10 Ω and an output common-mode adjust voltage of 1.2 V to 2.8 V.

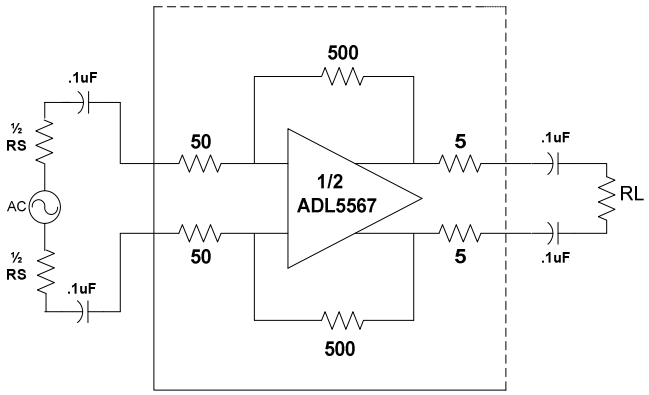


Figure 17. Basic Structure

The ADL5567 is composed of a dual fully differential amplifier with on-chip feedback and feed-forward resistors. The gain is fixed at 20 dB but can be reduced by adding two resistors in series with the two inputs (see Gain Adjustment and Interfacing section). The amplifier is designed to provide a high differential open-loop gain and has an output common-mode circuit that enables the user to change the output common-mode voltage by applying a voltage to a VCOMx pin. The amplifier is designed to provide superior low distortion at frequencies to and beyond 500 MHz with low noise and low power consumption. The low distortion and noise are realized with a 3.3 V power supply at 140 mA. . This amplifier achieves better than −92 dBc IMD3 at 500 MHz and −102 dBc at 200 MHz for 2 V p-p operation. In addition, the ADL5567 can also deliver 5 V p-p operation under heavy loads. The internal gain is set at 20 dB, and the part has a noise figure of 6.8 dB and a RTI of 1.2 nV/√Hz . When comparing noise figure and distortion performance, this amplifier delivers the best in category spurious-free dynamic range (SFDR).

The ADL5567 is very flexible in terms of I/O coupling. It can be ac- or dc-couplied. For dc coupling, the output common-mode voltage, VCOMx can be adjusted (using the VCOMx pin) from 1.1 V to 1.9 V output for VCCx at 3.3 V and up to 3 V with VCCx at 5 V. For the best distortion, the common-mode output should not go below 1.3 V at VCCx equal to 3.3 V and 1.75 V for 5 V VCCx operation. Note that the input common-mode voltage slaves to the VCOMx output voltage when ac-coupled at the inputs. For dc-coupled inputs ,the input common-mode voltage should also stay between 1.25 V and 1.8 V for a 3.3 V supply and 1.35 V to 3.5 V for a 5 V supply. Note again that for ac-coupled applications with series capacitors at the inputs, as in Figure 20, the output common-mode voltage, VCOMx, sets the common-mode input to the same level. Because of the wide input common-mode range, this part can easily be dc-coupled to many types of mixers, demodulators, and amplifiers. Forcing a higher input VCOMx does not affect the output VCOMx in dc-coupled mode. Note that if the outputs are ac-coupled no external VCOMx adjust is required because the amplifier common-mode outputs are set at VCCx/2.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 19 shows the basic connections for operating the ADL5567 Apply a voltage between 3 V and 5 V to the VCC1and VCC2 pins through two 5.1 nH inductors and decouple the supply side of the inductor with at least one low inductance, 0.01 µF surface-mount ceramic capacitor. In addition, decouple the VCOM1 and VCOM2 pins (Pin 21 and Pin 10) using a 0.1 µF capacitor. The ENBL1 and ENBL2 pins (Pin 22 and Pin 9) are tied to 3.3V to enable each amplifier. A differential signal is applied to Amplifier 1 through Pin 1 (VIN1) and Pin 2 (VIP1) and to Amplifier 2 through Pin 5 (VIP2) and Pin 6 (VIN2). Each amplifier has a gain of 20 dB.

The input pins, Pin 1 (VIN1) and Pin 2 (VIP1), and the output pins, Pin 18 (VON1) and Pin 17 (VOP1), can be externally biased by applying a voltage to Pin 21 (VCOM1). If VCOM1 is left open, VCOM1 equals ½ of VCC1. The input pins, Pin 5 (VINP) and Pin 6 (VIN2), and the output pins, Pin 13 (VON2) and Pin 14 (VOP2), can be externally biased by applying a voltage to VCOM2. If VCOM2 is left open, VCOM2 equals ½ of VCC2.Pin 8 is the power mode pin for side 2 and pin 23 is the power mode pin for side 1. When tied low the side will be in the high performance mode. When tied high (3.3V) the part will be in the low power mode. The ADL5567 can be ac-coupled as shown in

Figure 19, or can be dc-coupled if within the specified input and output common-mode voltage ranges (see the Circuit Description section). To enable the ADL5567, the ENBL1 and ENBL2 pins must be pulled high (3.3V). Pulling the ENBL1/ENBL2 pins low puts the ADL5567 in sleep mode, reducing the current consumption to 7 mA at ambient.

A series 5.1 nH inductor can be connected to the VCCx pins with the V_{CC} decoupling capacitor connected to the V_{CC} bus side (see Figure 18). This inductor with the internal capacitance of the amplifier results in a two pole low-pass network and reduces the amplifier V_{CC} noise.

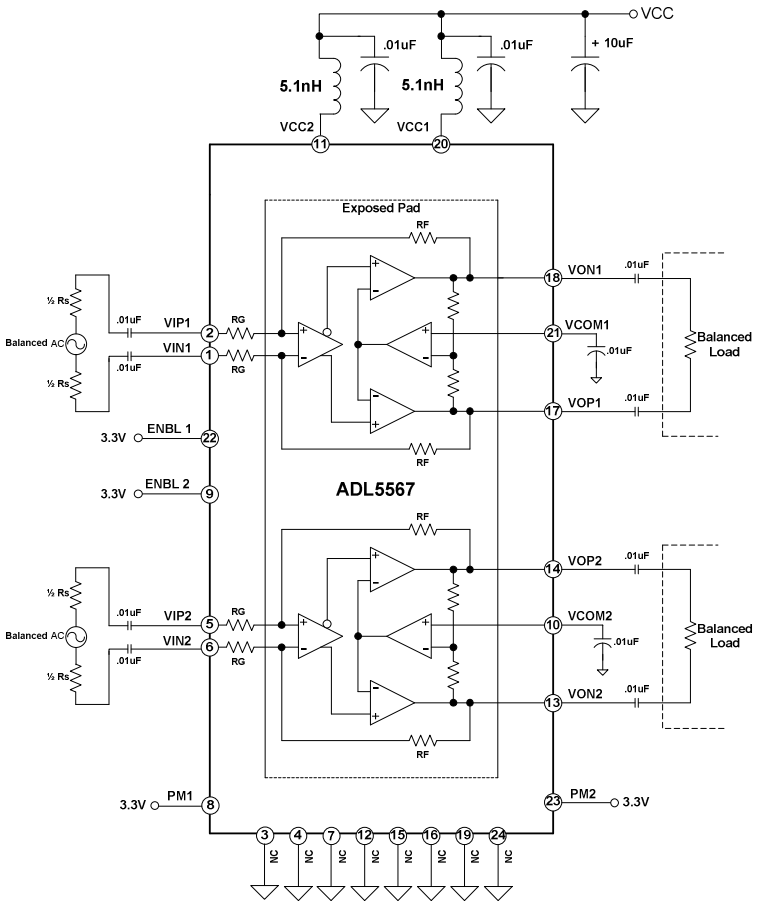


Figure 19. Basic Connections

INPUT AND OUTPUT INTERFACING

The ADL5567 can be configured as a differential-input-to-differential-output driver, as shown in Figure 20. The 50 Ω resistors, R1 and R2, combined with the ETC1-1-13 balun transformer, provide a 50 Ω input match for the 100 Ω input impedance . The input and output 0.1 µF capacitors isolate the $V_{CC}/2$ bias from the source and balanced load. The load should equal 200 Ω to provide the expected ac performance (see the Specifications section).

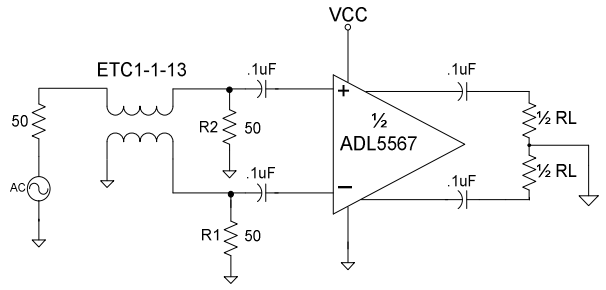


Figure 20. Differential-Input-to-Differential-Output Configuration

The differential gain of the ADL5567 is dependent on the source impedance and load, as shown in Figure 21

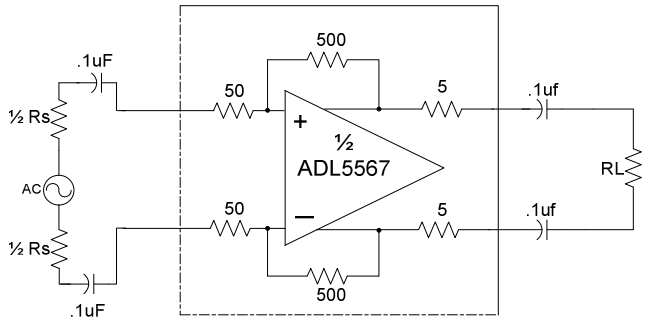


Figure 21. Differential Input Loading Circuit

The differential gain can be determined by

$$A_V = \frac{500}{50} \times \frac{R_L}{10 + R_L} \quad (1)$$

Single-Ended Input to Differential Output

The ADL5567 can also be configured in a single-ended-input-to-differential-output driver, as shown in Figure 22. In this configuration, the gain of the part is reduced due to the application of the signal to only one side of the amplifier. The single ended circuit configuration can be accomplished in three steps referring to Figure 39 and assuming a 50 ohm Rs source. First calculate the input impedance of the amplifier Rin using the formula below.

$$\text{Rin} := \frac{\text{RG}}{1 - \left[\frac{\text{RF}}{2 \cdot (\text{RG} + \text{RF})}\right]}$$

Rin = 91.6

The next step is to calculate the termination resistor R2 (Fig 39.) using the formula below assuming a 50ohm Rs termination.

$$50 := \frac{\text{R2} \cdot \text{Rin}}{\text{R2} + \text{Rin}}$$

R2 = 109

The last step is to calculate the gain path rebalancing resistor R1 (Fig 39). Using the formula below.

$$\text{R1} := \frac{\text{Rs} \cdot \text{R2}}{\text{Rs} + \text{R2}}$$

R1=34.2

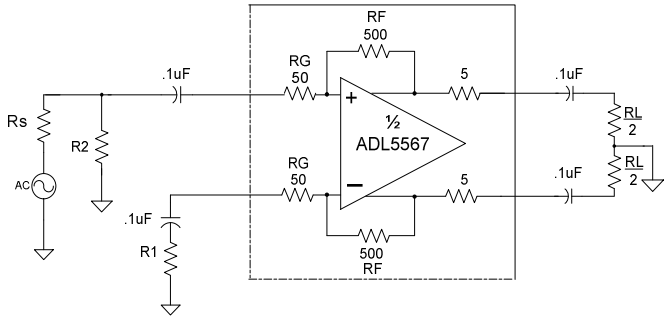


Figure 22. Single-Ended-Input-to-Differential-Output Configuration

The single-ended gain configuration of the ADL5567 is dependent on the source impedance and load, as shown in Figure 23.

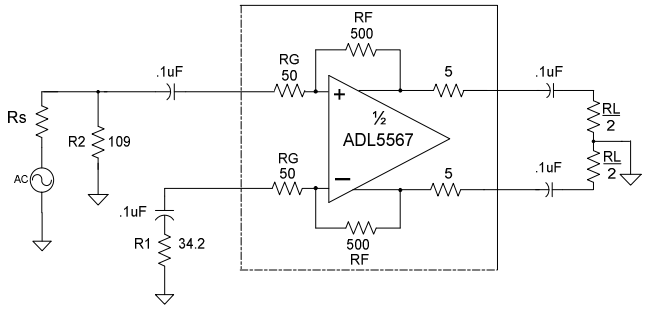


Figure 23. Single-Ended Input Loading Circuit

The single-ended gain can be determined by the following two equations:

$$R_{MATCH} = \frac{R2 \times \text{Rin}}{R2 + \text{Rin}}$$

$$A_{VI} = \frac{500}{50+\left(\frac{R_S \times R2}{R_S + R2}\right)} \times \frac{R2}{R_S + R2} \times \frac{R_{MATCH} + R_S}{R_{MATCH}} \times \frac{R_L}{10+R_L}$$

GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5567 can be reduced by adding two resistors in series with the inputs to reduce the 20 dB gain.

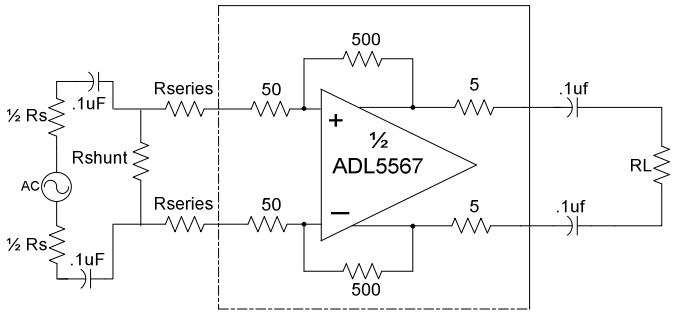


Figure 24. Gain Adjustment Using a Series Resistor Show

To find R_{SERIES} for a given A_V gain and R_L, use the following:

$$R_{SERIES} = \left[\frac{500}{\left[\frac{A_V}{\left(\frac{R_L}{10+R_L}\right)}\right]}\right] - 50 \quad (3)$$

To calculate the A_V gain for a given R_{SERIES} and R_L, use the following:

$$A_{GAIN} = \left(\frac{500}{R_{SERIES} + 50}\right) \times \left(\frac{R_L}{10 + R_L}\right) \quad (4)$$

The necessary shunt component, R_{SHUNT}, to match to the source impedance, R_S, can be expressed as

$$R_{SHUNT} = \frac{1}{\frac{1}{R_S} - \frac{1}{2R_{SERIES} + 100}} \quad (5)$$

The voltage gain for multiple shunt resistor values are summarized in Table 5. The source resistance and input impedance need careful attention when using Equation 5. The reactance of the input impedance of the ADL5567 and the ac coupling capacitors must be considered before assuming that they make a negligible contribution.

Table 5. Differential Gain Adjustment Using Series Resistor

Target Gain(dB)		R_S (Ω)	R_{SERIES} (Ω)[1]	R_{SHUNT} (Ω)[1]
0		50	426.1	52.7
1		50	374.4	53.1
2		50	328.2	53.5
3		50	287.1	54
4		50	250.4	54.5
5		50	217.7	55.1
6		50	188.6	55.8
7		50	162.7	56.6

8		50	139.5	57.5
9		50	118.9	58.6
10		50	100.5	59.9
11		50	84.2	61.4
12		50	69.6	63.2
13		50	56.6	65.3
14		50	45	67.8
15		50	34.6	70.9
16		50	25.4	74.7
17		50	17.2	79.5
18		50	9.9	85.7
19		50	3.4	93.7

[1] The resistor values are rounded to the nearest real resistor value.

LAYOUT CONSIDERATIONS

High-Q inductive drives and loads, as well as stray transmission line capacitance in combination with package parasitics, can potentially form a resonant circuit at high frequencies, resulting in excessive gain peaking or possible oscillation. If RF transmission lines connecting the input or output are used, design them such that stray capacitance at the input/output pins is minimized. In many board designs, the signal trace widths should be minimal where the driver/receiver is no more than one-eighth of the wave-length from the amplifier. This nontransmission line configuration requires that underlying and adjacent ground and low impedance planes be dropped from the signal lines.

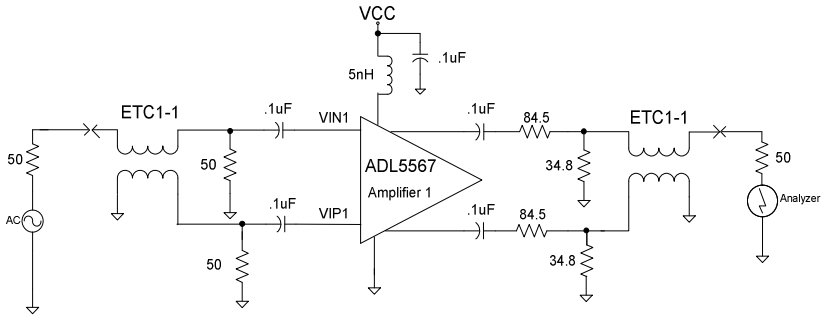


Figure 25. General-Purpose Characterization Circuit

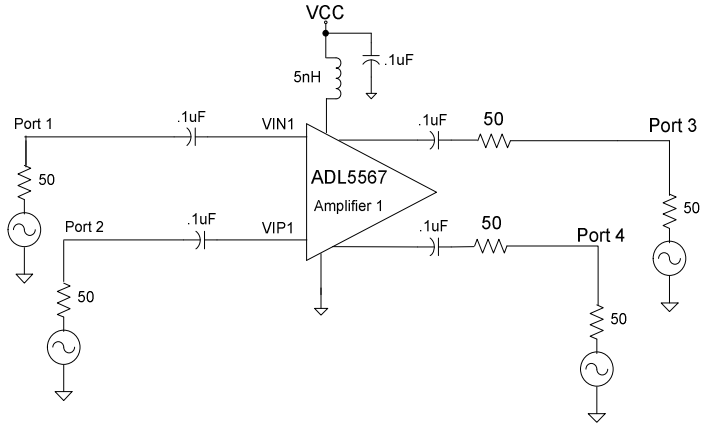


Figure 26. Differential Characterization Circuit Using Agilent E8357A Four-Port PNA

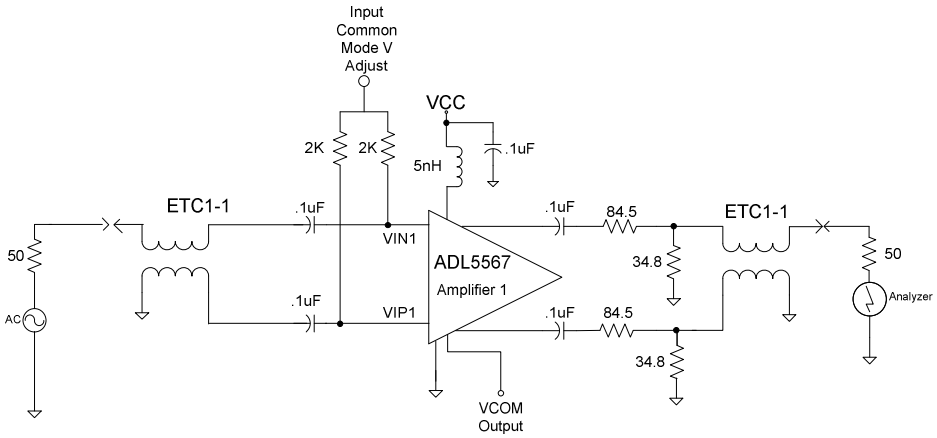


Figure 27. Distortion Measurement Circuit for Various Common-Mode Voltages

SOLDERING INFORMATION AND RECOMMENDED LAND PATTERN

Figure 28 shows the recommended land pattern for the ADL5567. The ADL5567 is contained in a 4 mm × 4 mm LFCSP package, which has an exposed ground paddle (EPAD). This paddle is internally connected to the ground of the chip. To minimize thermal impedance and ensure electrical performance, solder the paddle to the low impedance ground plane on the printed circuit board (PCB). To further reduce thermal impedance, it is recommended that the ground planes on all layers under the paddle be stitched together with vias.

For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

This land pattern, on the ADL5567 evaluation board, provides a measured thermal resistance (θ_{JA}) of 34.0°C/W. To measure θ_{JA}, the temperature at the top of the LFCSP package is found with an IR temperature gun. Thermal simulation suggests a junction temperature 1.5°C higher than the top of package temperature. With additional ambient temperature and I/O power measurements, θ_{JA} can be determined.

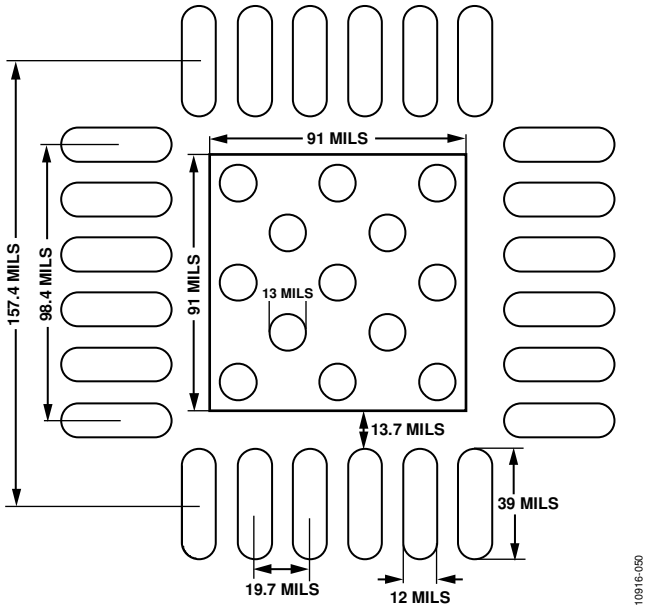


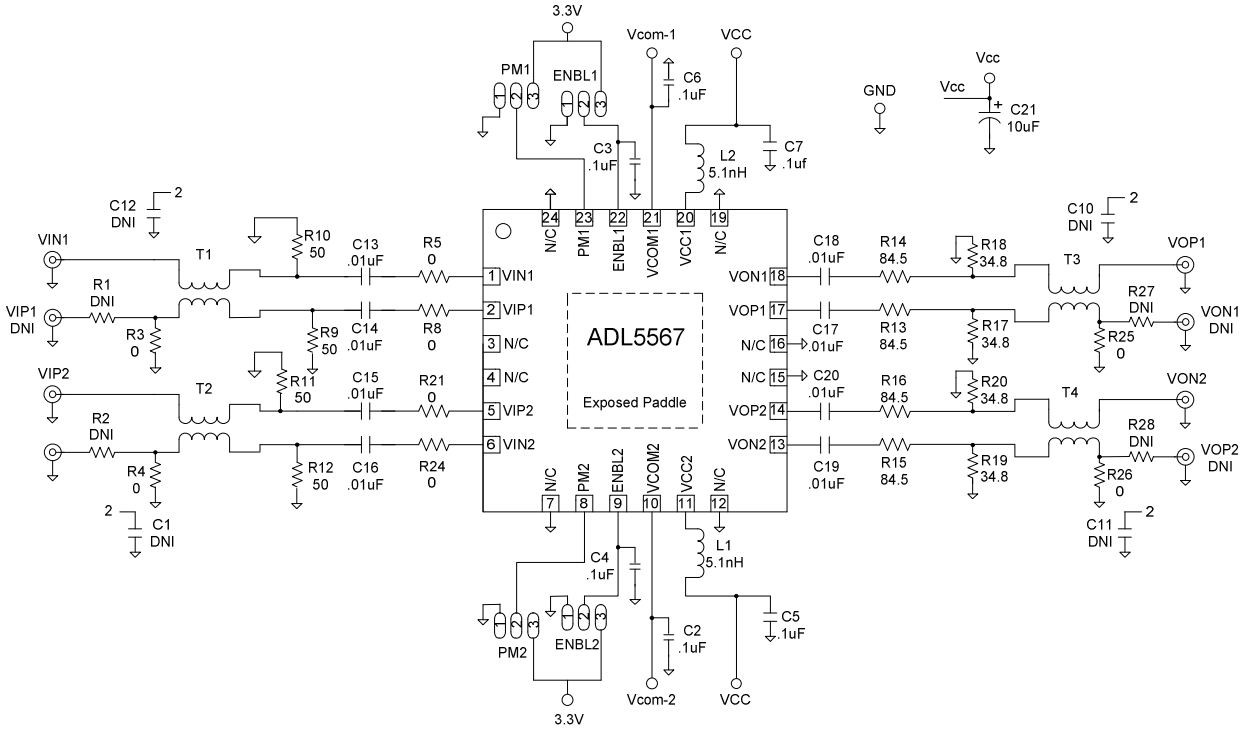
Figure 28. Recommended Land Pattern

EVALUATION BOARD

shows the schematic of the ADL5567 evaluation board. The board is powered by a single supply in the 3 V to 5 V range. The power supply is decoupled by 10 µF and 0.1 µF capacitors. Inductors, L1 and L2, decouple the ADL5567 from the power supply.

Table 6 details the various configuration options of the evaluation board. Figure 29 and Figure 30 show the component and circuit side layouts of the evaluation board.

The balanced input and output interfaces are converted to single ended with a pair of baluns (M/A-COM ETC1-1-13). The baluns at the input, T1 and T2, provide a 50 Ω single-ended-to-differential transformation. The output baluns, T3 and T4, and the matching components are configured to provide a 100 Ω to 50 Ω impedance transformation with an insertion loss of about 11 dB.



Evaluation Board Schematic

Table 6. Evaluation Board Configuration Options

Component	Description	Default Condition
V_{POS}, GND	Ground and supply test loops.	V_{POS}, GND = installed
C5, C7, C21, L1, L2	Power supply decoupling. The supply decoupling consists of a 10 µF capacitor (C21) and two 0.1µF capacitors, C5 and C7 connected between the supply lines and ground. L1 and L2 decouple the ADL5567 from the power supply.	C21 = 10 µF (Size D), C5, C7 = 0.1 µF (Size 0402) L1, L2 = 5.1 nH (Size (0603)
VIN1, VIP1, VIP2, VIN2, R1, R2, R3, R4, R5, R8, R9, R10, R11, R12, R21, R24, C13, C1, C12, C14, C15, C16, T1, T2	Input interface. The SMA labeled VIN1 is the input to amplifier 1. T1 is a 1-to-1 impedance ratio balun to transform a single-ended input into a balanced differential signal. Removing R3, installing R1 (0 Ω), and installing an SMA connector (VIP1) allows driving from a differential source. C13 and C14 provide ac coupling. C12 is an optional by pass capacitor. R9 and R10 provide a differential 50 Ω input termination. The SMA labeled VIP2 is the input to amplifier 2. T2 is a 1-to-1 impedance ratio balun to transform a single-ended input into a balanced differential signal. Removing R4, installing R2 (0 Ω), and installing an SMA connector (VIN2) allows driving from a differential source. C15 and C16 provide ac coupling. C1 is an optional by pass capacitor. R11 and R12 provide a differential 50 Ω input termination.	VIN1, VIP2 = installed VIP1, VIN2 = not installed R1, R2 = DNI, R3, R4, R5, R8, R21, R24 = 0 Ω (Size 0402) R9, R10, R11, R12 = 36 Ω (Size 0402) C13, C14, C15, C16 = 0.01 µF (Size 0402) C1,C12 = DNI T1, T2 = ETC1-1-13 (M/A-COM)
VOP1, VON1, VON2, VOP2, C10, C11, C17, C18, C19, C20,	Output interface. The SMA labeled VOP1 is the output for amplifier1. T3 is a 1-to-1 impedance ratio balun used to transform a balanced differential signal to a single-ended signal. Removing R25, installing R27 (0 Ω), and installing an SMA connector (VON1) allows differential loading. C10 is an optional bypass capacitor. C17 and C18	VOP1, VON2, = installed VON1, VOP2 = not installed R13, R14, R15, R16 = 84.5 Ω (Size 0402)

Component	Description	Default Condition
R13, R14, R15, R16, R17, R18, R19, R20, R25, R26, R27, R28, T3, T4	provide ac coupling. R13, R14, R17, and R16 are provided for generic placement of matching components. The SMA labeled VON2 is the output for amplifier2. T4 is a 1-to-1 impedance ratio balun used to transform a balanced differential signal to a single-ended signal. Removing R26, installing R28 (0 Ω), and installing an SMA connector (VOP2) allows differential loading. C11 is an optional bypass capacitor. C19 and C20 provide ac coupling. R15, R16, R19, and R20 are provided for generic placement of matching components. The evaluation board is configured to provide a 200 Ω to 50 Ω impedance transformation with an insertion loss of 11 dB.	R17, R18, R19, R20 = 34.8 Ω (Size 0402), R25, R26 = 0 Ω (Size 0402) R27, R28 = DNI (Size 0402) C10, C11 = DNI (Size 0402) C17, C18 = 0.01 µF (Size 0402) C19, C20 = 0.01 µF (Size 0402) T3, T4 = ETC1-1-13 (M/A-COM)
ENBL_1, ENBL_2, C3, C4	Device enable. ENBL_1 is the enable for amplifier1. Connecting a jumper between Pin 2 and V_{POS} enables amplifier1. C3 is a bypass capacitor. ENBL_2 is the enable for amplifier2. Connecting a jumper between pin 2 and V_{POS} enables amplifier2. C4 is a bypass capacitor.	ENBL_1, ENBL_2 = installed, C3, C4 = 0.1 µF (Size 0402)
VCOM-1, VCOM-2, C2, C6	Common-mode voltage interface. VCOM1 is the common-mode interface for Amplifier 1. A voltage applied to this pin sets the common-mode voltage of the output of Amplifier 1. VCOM2 is the common-mode interface for Amplifier 2. A voltage applied to this pin sets the common-mode voltage of the output of Amplifier 2. Typically decoupled to ground with a 0.1 µF capacitor (C2 and C6). With no reference applied, input and output common mode floats to mid supply (V_{CC}/2).	VCOM-1, VCOM-2 = installed C2, C6 = 0.1 µF (Size 0402)
PM1, PM2	Power mode control. Each amplifier has a power mode control which lowers the current in the amplifier to lower the power consumption.	PM1, PM2, = installed

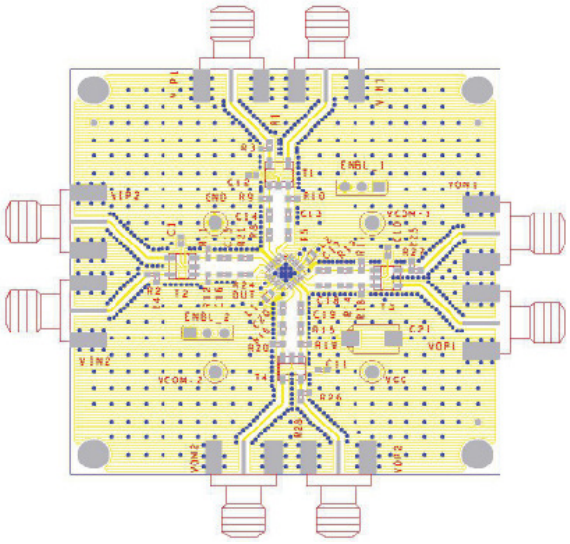


Figure 29. Layout of Evaluation Board, Component Side

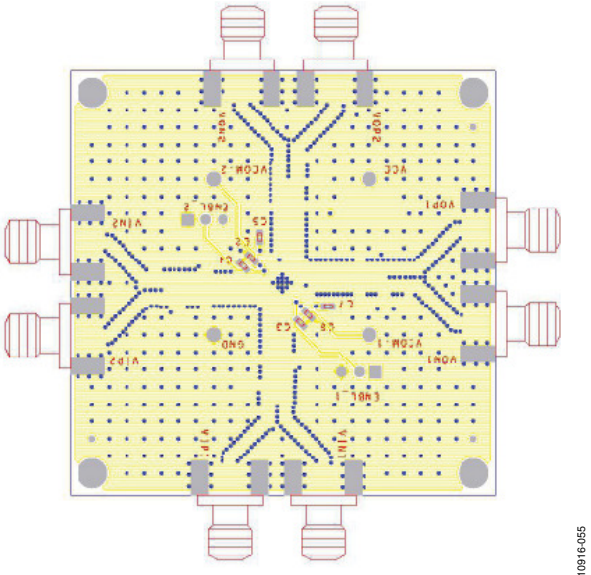
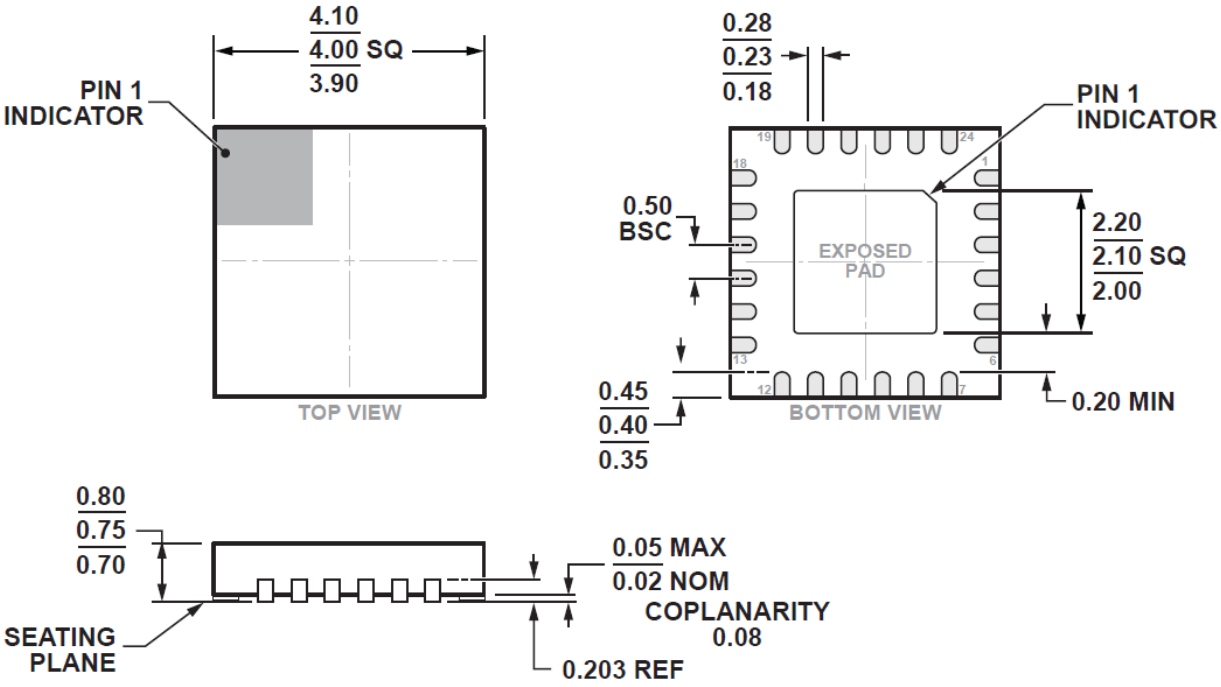


Figure 30. Layout of Evaluation Board, Circuit Side

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-6.

Figure 31. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-19)
Dimensions shown in millimeters

PR13858-0-11/15(PrB)