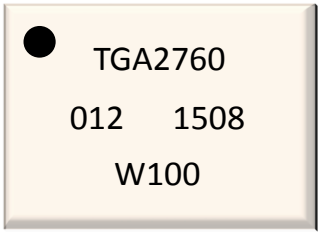
TGA2760-SM

9.5 – 12 GHz Power Amplifier

Applications

- Point-to-Point Radio



20-Lead 8.0 x 10.0 x 2 mm Package

Product Features

- Frequency Range: 9.5 – 12 GHz
- Power: +42 dBm Psat
- Gain: 33 dB
- Integrated Power Detector
- Bias: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{D3} = +28$ V, $I_{D3} = 260$ mA
- Package Dimensions: 8.0 x 10.0 x 2 mm

General Description

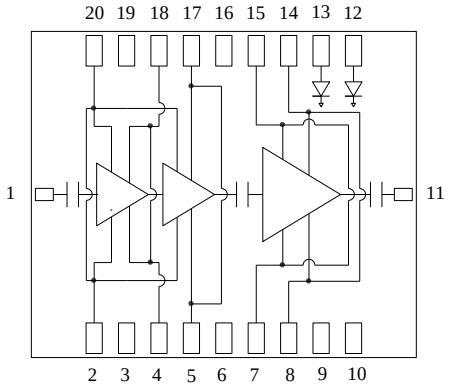
The TriQuint TGA2760-SM is a Power Amplifier with integrated power detector. The TGA2760-SM operates from 9.5 – 12 GHz and is designed using TriQuint's power GaAs pHEMT and GaN HEMT production processes.

The TGA2760-SM typically provides +42 dBm of saturated output power with small signal gain of 23 dB.

The TG2760-SM is available in a low-cost, surface mount 20 lead 8 x 10 mm laminate package and is ideally suited for Point-to-Point Radio.

Lead-free and RoHS compliant

Functional Block Diagram



Pin Configuration

Pin No.	Label
1	RF IN
2, 20	V_{G12}
4, 18	V_{D1}
5, 17	V_{D2}
3, 6, 9, 10, 16, 19	NC
7, 15	V_{G3}
8, 14	V_{D3}
11	RF OUT
12	V_{REF}
13	V_{DET}

Ordering Information

Part No.	ECCN	Description
TGA2760-SM	3A001.b.3.b.2	9.5 – 12 GHz 18 W Amp

Standard T/R size = 500 pieces on a 7" reel

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V_{D1}, V_{D2}	+9 V
Drain Voltage, V_{D3}	+32 V
Drain Current, $I_{D1} + I_{D2}$	3850 mA
Drain Current, I_{D3}	2000 mA
Power Dissipation, Driver Stages, P_{DISS}	14.8 W
Power Dissipation, Final Stage, P_{DISS}	28.8 W
RF Input Power, CW, 50 Ω, T = 25 °C	+29 dBm
GaAs Channel Temperature, T_{CH}	250 °C
GaN Channel Temperature, T_{CH}	275 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	−40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temp. Range	−40	+25	+85	°C
V_{D1}, V_{D2}		+7		V
V_{D3}		+28		V
$I_{D1} + I_{D2}$		1000		mA
I_{D3}		260		mA
V_{G12}		−0.7		V
V_{G3}		−2.6		V
$I_{D1} + I_{D2}$ drive (at +40 dBm Pout)		1031		mA
I_{D3} drive (at +40 dBm Pout)		1060		mA

Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3-} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

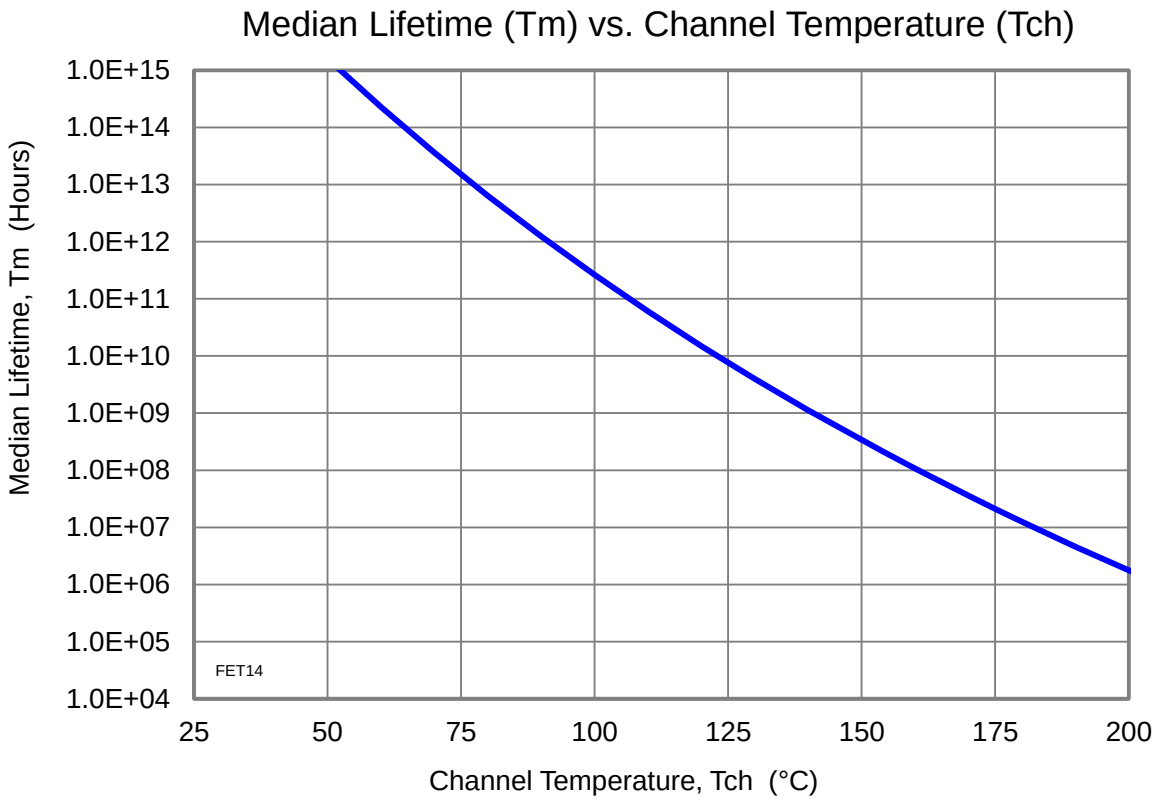
Parameter	Conditions	Min	Typ	Max	Units
RF Frequency Range		9.5		12.0	GHz
Small Signal Gain			33		dB
Input Return Loss, IRL			8		dB
Output Return Loss, ORL			8		dB
Output Power at Pin = +12 dBm			+42		dBm
Output Third Order Intercept, TOI at +35 dBm / Tone			+52		dBm
Power Added Efficiency			36		%
Gain Temperature Coefficient			−0.05		dB / °C
Power Temperature Coefficient			−0.01		dBm / °C

Notes:

1.

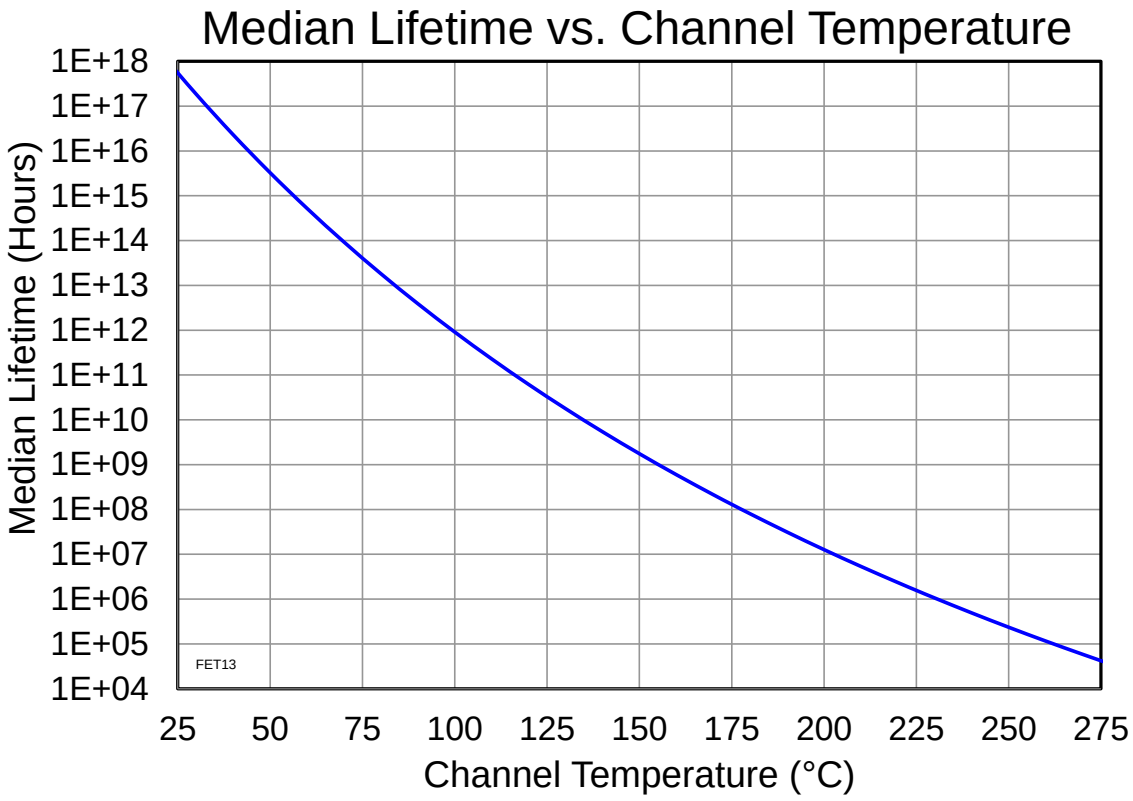
Thermal and Reliability Information (Driver Stages)

Parameter	Conditions	Rating
Thermal Resistance, θ_{JC}, measured to back of package	T_{BASE} = +85 °C	θ_{JC_DRIVER} = 8.2 °C/W
Channel Temperature (T_{CH}), and Median Lifetime (T_M)	T_{BASE} = 85 °C, $V_{D\ DRIVER}$ = +7 V, I_{D_DRIVER} = 1000 mA, P_{DISS_DRIVER} = 7.0 W	$T_{CH\ DRIVER}$ = 142 °C T_{M_DRIVER} = 8.77E+8 Hours
Channel Temperature (T_{CH}), and Median Lifetime (T_M) at +40 dBm Pout	T_{BASE} = +85 °C, $V_{D\ DRIVER}$ = +7 V, I_{D_DRIVER} = 1031 mA, P_{DISS_DRIVER} = 7.2 W	$T_{CH\ DRIVER}$ = 144 °C T_{M_DRIVER} = 6.88E+8 Hours



Thermal and Reliability Information (Final Stage)

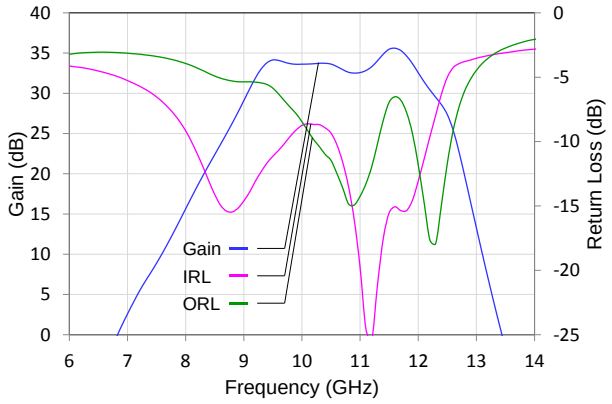
Parameter	Conditions	Rating
Thermal Resistance, θ_{JC}, measured to back of package	T_{BASE} = +85 °C	θ_{JC_FINAL} = 5.1 °C/W
Channel Temperature (Tch), and Median Lifetime (Tm)	$V_{D\ FINAL}$ = 28 V, $I_{D\ FINAL}$ = 260 mA P_{DISS_FINAL} = 7.3 W	$T_{CH\ FINAL}$ = 122 °C T_{M_FINAL} = 4.79E+10 Hours



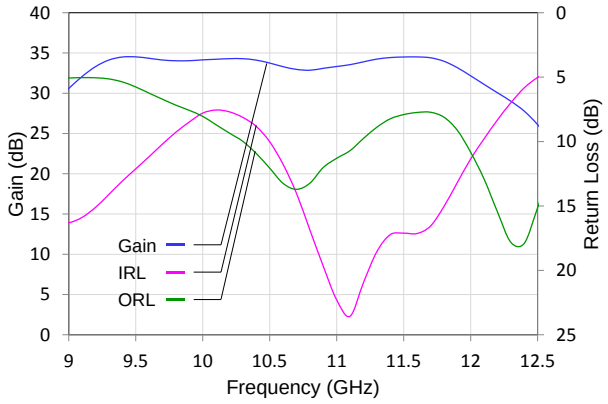
Typical Performance

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

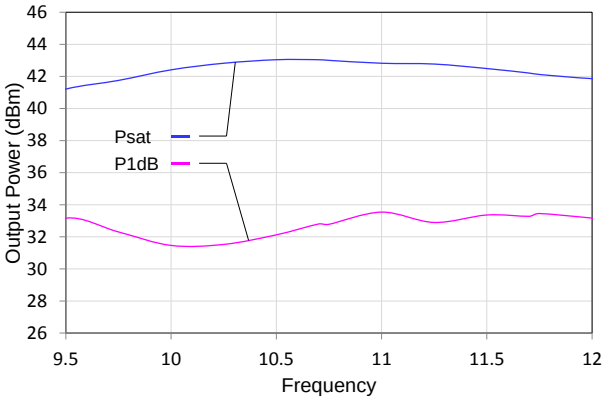
S-Parameter vs. Frequency



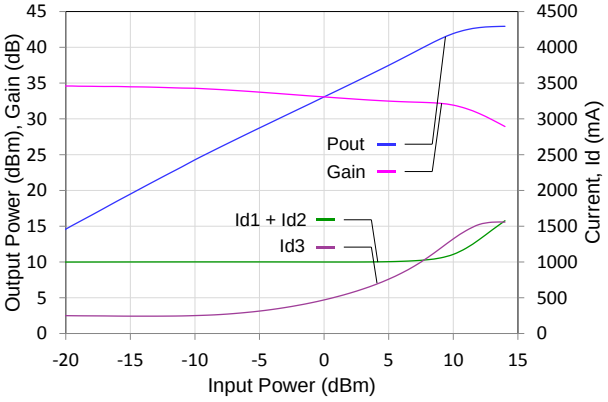
S-Parameter vs. Frequency



Output Power vs. Frequency

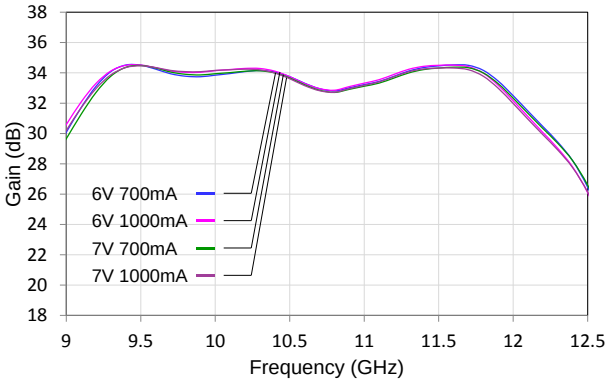


Pout, Gain, Id vs. Pin @ 10.5 GHz



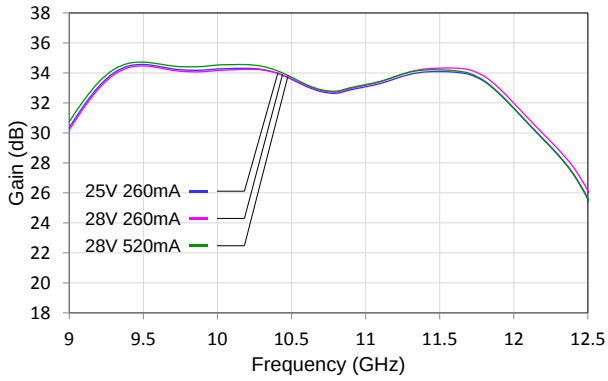
Gain vs. Frequency vs. Bias (Vd1 and Vd2)

Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



Gain vs. Frequency vs. Bias (Vd3)

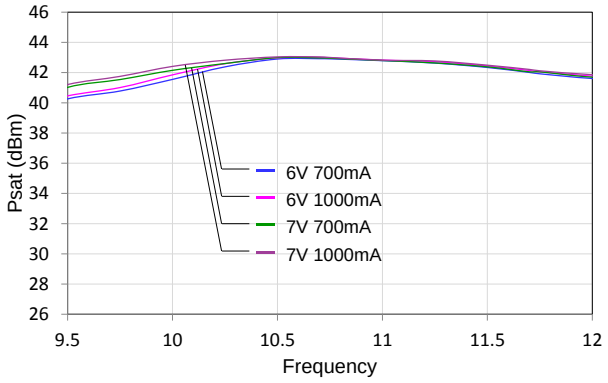
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



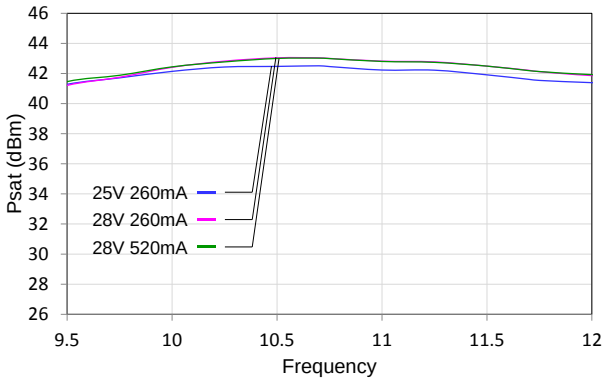
Typical Performance

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3-} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

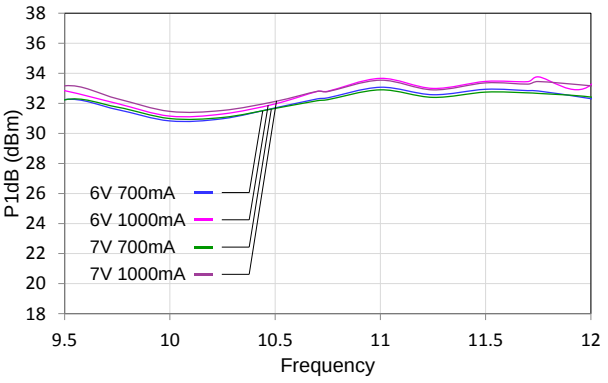
Psat vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



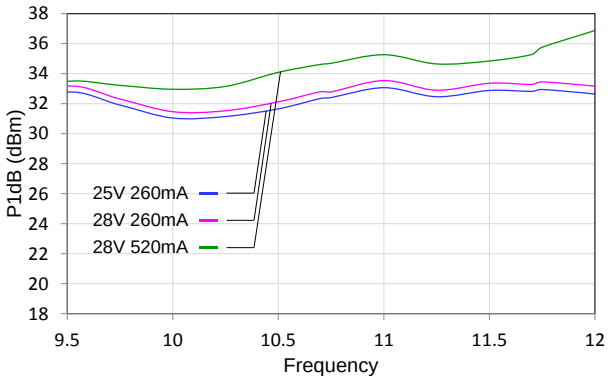
Psat vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



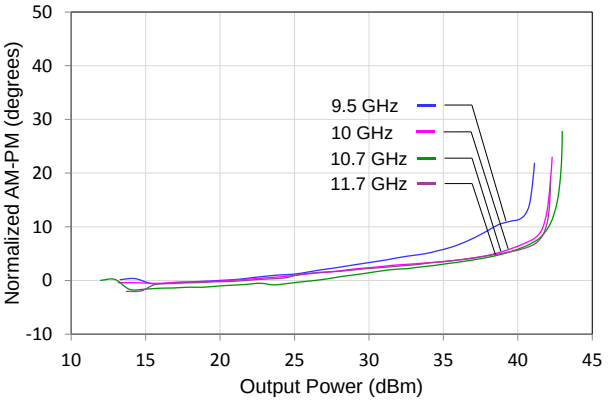
P1dB vs. Frequency vs. Bias (Vd1 and Vd2)
Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



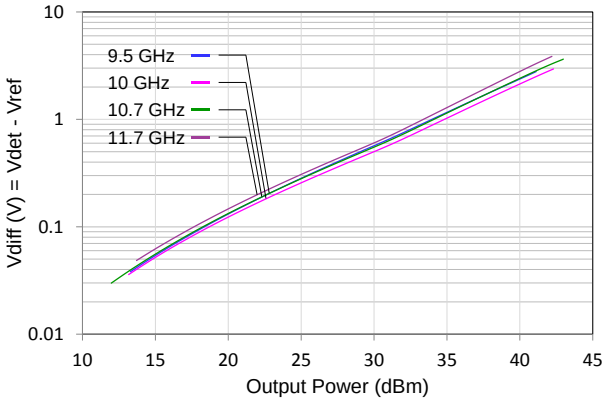
P1dB vs. Frequency vs. Bias (Vd3)
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



AM-PM vs. Pout vs. Frequency



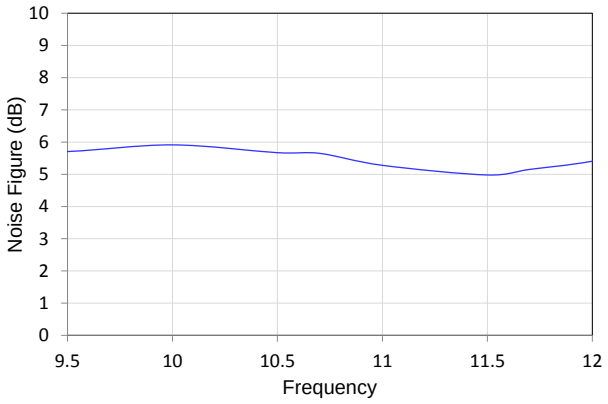
Power Detector vs. Pout vs. Frequency



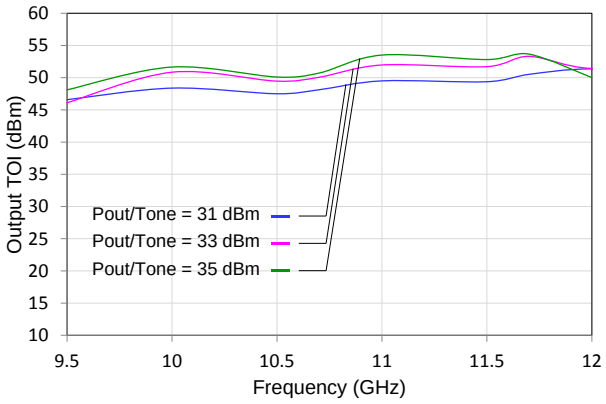
Typical Performance

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, $V_{D3-} = +28$ V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

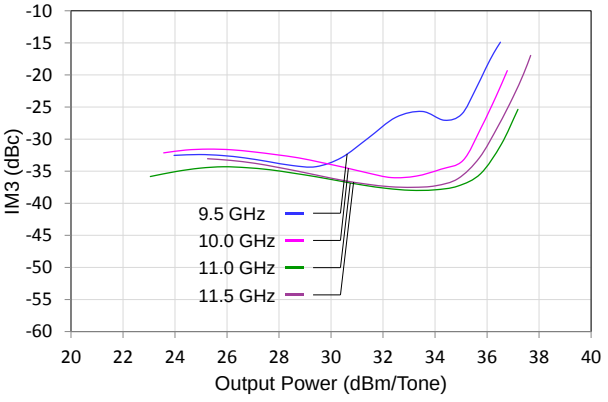
Noise Figure vs. Frequency



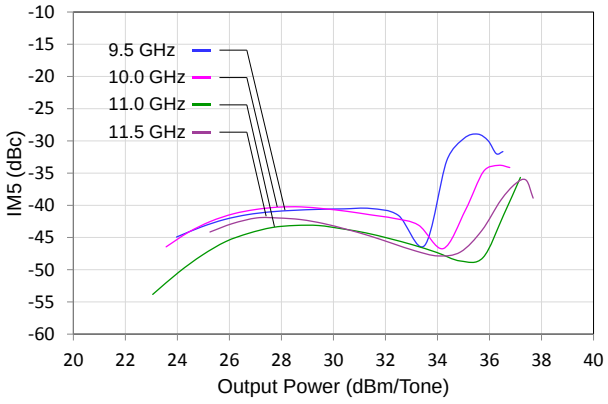
TOI vs. Frequency vs. Pout/Tone



IM3 vs. Pout/Tone vs. Frequency

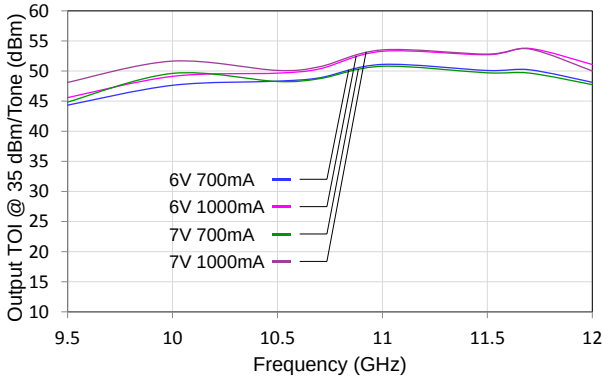


IM5 vs. Pout/Tone vs. Frequency



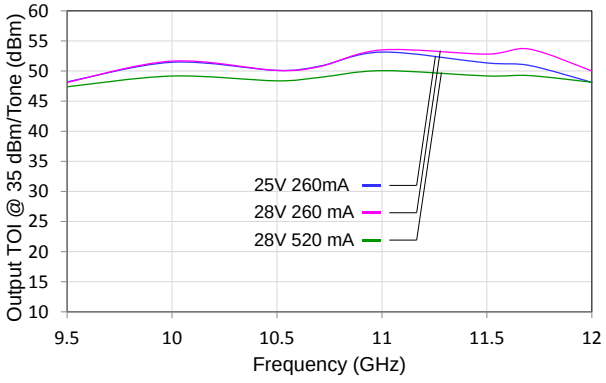
TOI vs. Frequency vs. Bias (Vd1 and Vd2)

Vd3 = 28 V, Id3 = 260 mA, Vg3 = -2.6 V Typical



TOI vs. Frequency vs. Bias (Vd3)

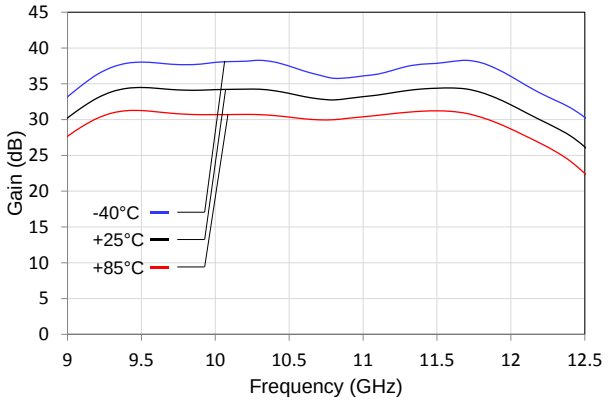
Vd1 = Vd2 = 7 V, Id1 + Id2 = 1000 mA, Vg12 = -0.7 V Typical



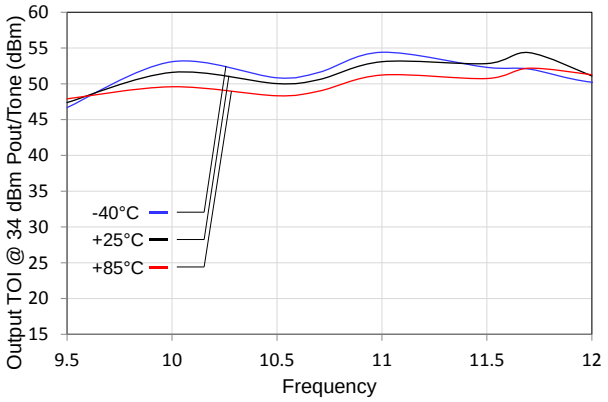
Typical Performance

Test conditions unless otherwise noted: $V_{D1} = V_{D2} = +7$ V, $I_{D1} + I_{D2} = 1000$ mA, $V_{G1} = V_{G2} = -0.7$ V, V_{D3}- = +28 V, $I_{D3} = 260$ mA, $V_{G3} = -2.6$ V, Temp = +25 °C, $Z_0 = 50\ \Omega$

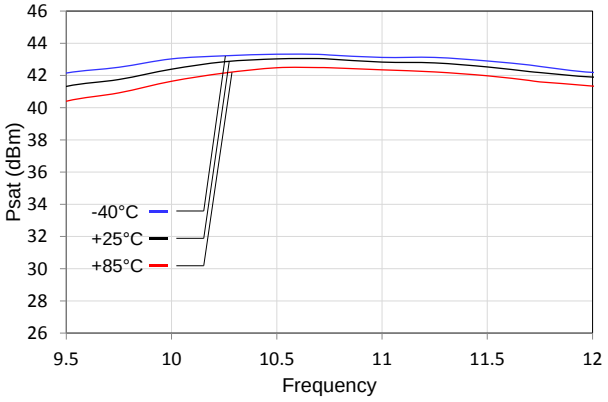
Gain vs. Frequency vs. Temperature



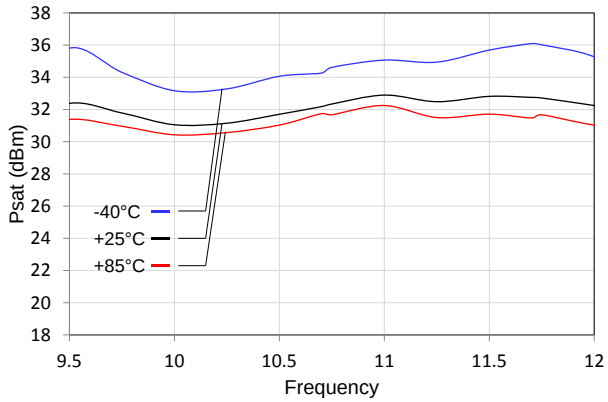
TOI vs. Frequency vs. Temperature



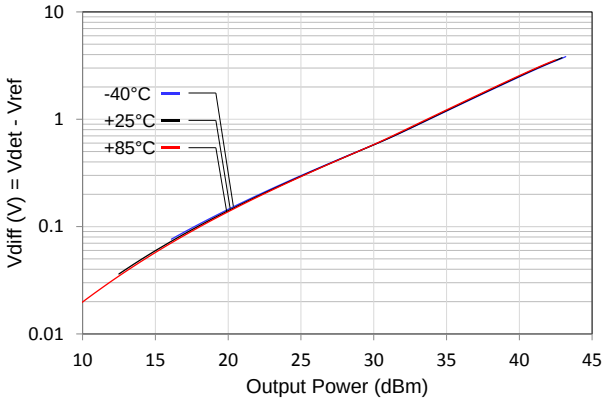
Psat vs. Frequency vs. Tempurature



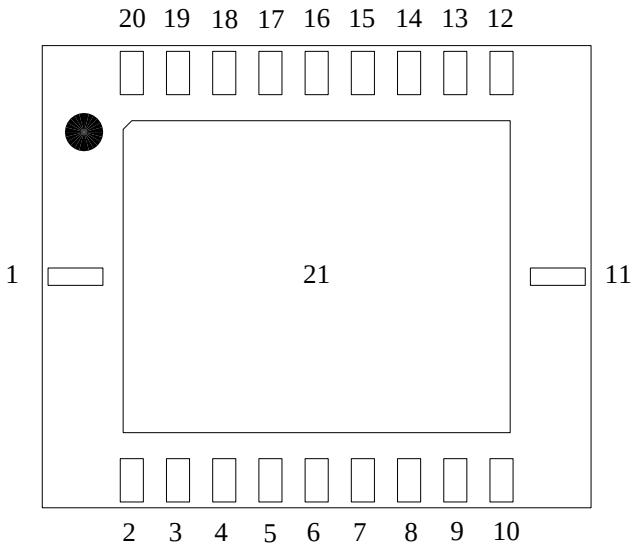
P1dB vs. Frequency vs. Tempurature



Power Detector vs. Pout vs. Temperature



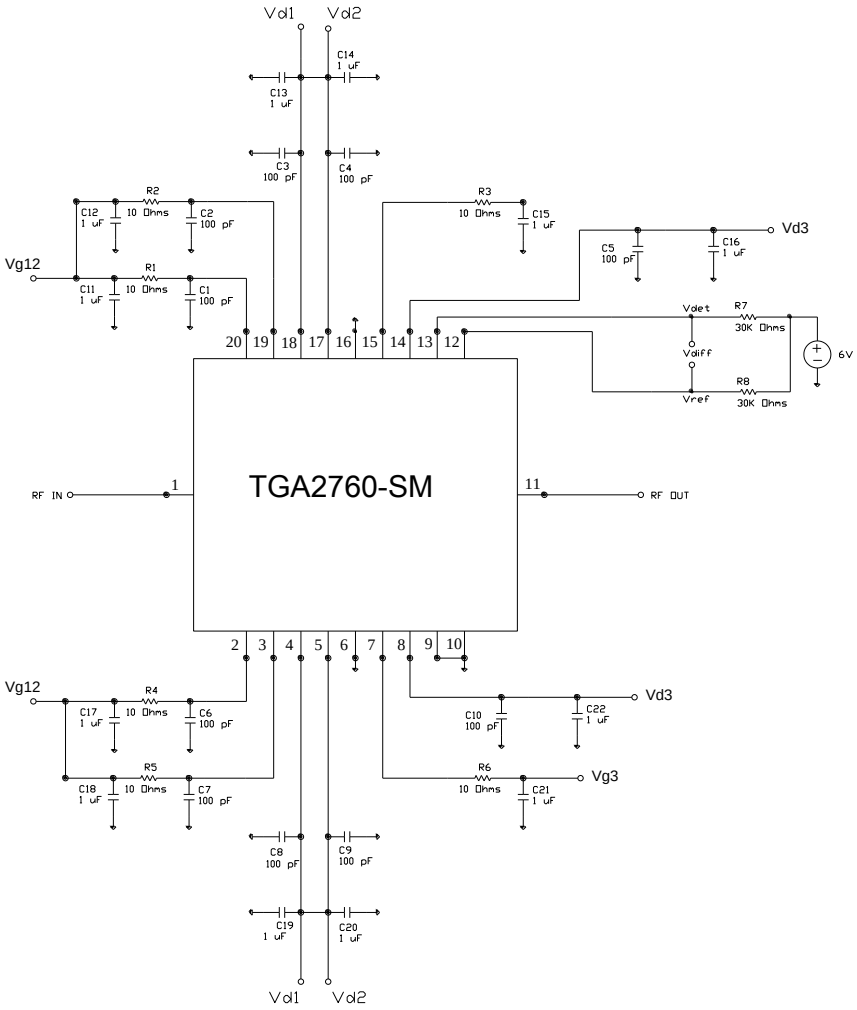
Pin Configuration and Description



Top View

Pin No.	Label	Description
1	RF IN	RF Input, matched to 50 Ω, AC Coupled.
2, 20	V_{G12}	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left open; see Application Circuit on page 11 as an example.
3, 6, 9, 10, 16, 19	NC	No internal connection; can be grounded on PCB.
4, 18	V_{D1}	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
5, 17	V_{D2}	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
7, 15	V_{G3}	Gate voltage. Bias network is required; can be biased from either pin, and non-biased pin can be left opened; see Application Circuit on page 11 as an example.
8, 14	V_{D3}	Drain voltage. Bias network is required; see Application Circuit on page 11 as an example.
11	RF OUT	RF Output, matched to 50 ohms, AC Coupled.
12	V_{REF}	Reference diode output voltage.
13	V_{DET}	Detector diode output voltage. Varies with RF output power.
21	GND	Backside Paddle. Multiple vias should be employed to minimize inductance and thermal resistance; see Mounting Configuration on page 14 for suggested footprint.

Application Circuit



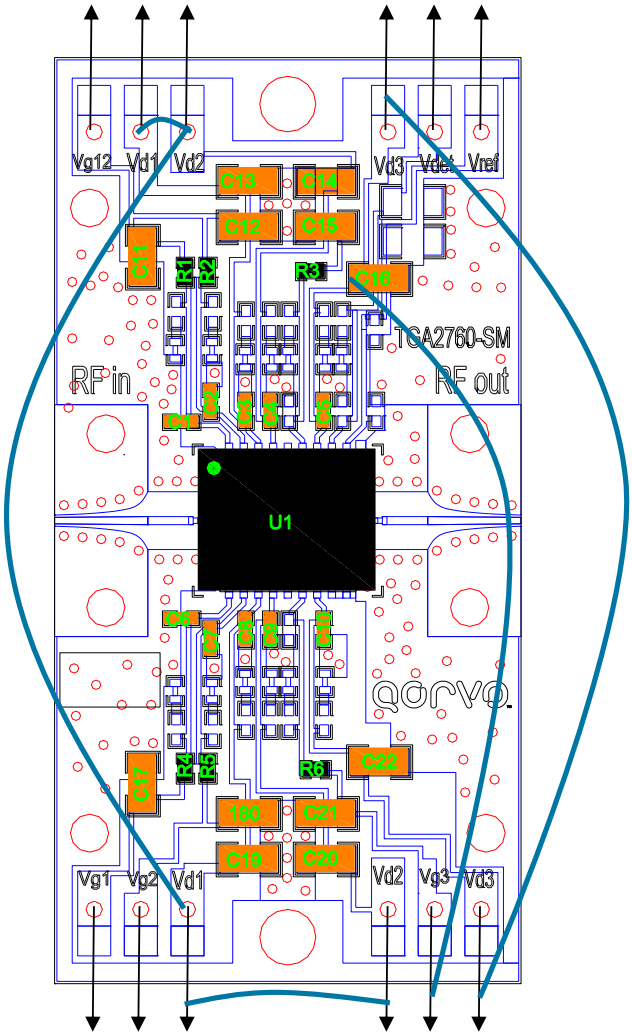
V_{G12} can be biased from either side, and the non-biased side can be left open.
V_{D1}, V_{D2}, V_{D3}, V_{G3} must be biased from both sides.
R7, R8 are external resistors, not built on board.

Bias-up Procedure	Bias-down Procedure
V_{G12} set to −1.5 V	Turn off RF signal
V_{G3} set to −3.5 V	Reduce V_{G12} to −1.5 V. Ensure I_D ~ 0 mA
V_{D1}, V_{D2} set to +7 V	Reduce V_{G3} to −3.5 V. Ensure I_D ~ 0 mA
V_{D3} sets to +28 V	Turn V_{D1}, V_{D2}, V_{D3} to 0 V
Adjust V_{G12} more positive until quiescent I_D is 1000 mA. This will be ~ V_G = −1 V typical	Turn V_{G12}, V_{G3} to 0 V
Adjust V_{G3} more positive until quiescent I_D is 260 mA. This will be ~ V_G = −2.6 V typical	
Apply RF signal	

Application Circuit

PC Board Layout

Board material is RO4003 0.008" thickness with ½ oz copper cladding.
For further technical information, refer to the TGA2760-SM Product Information page.



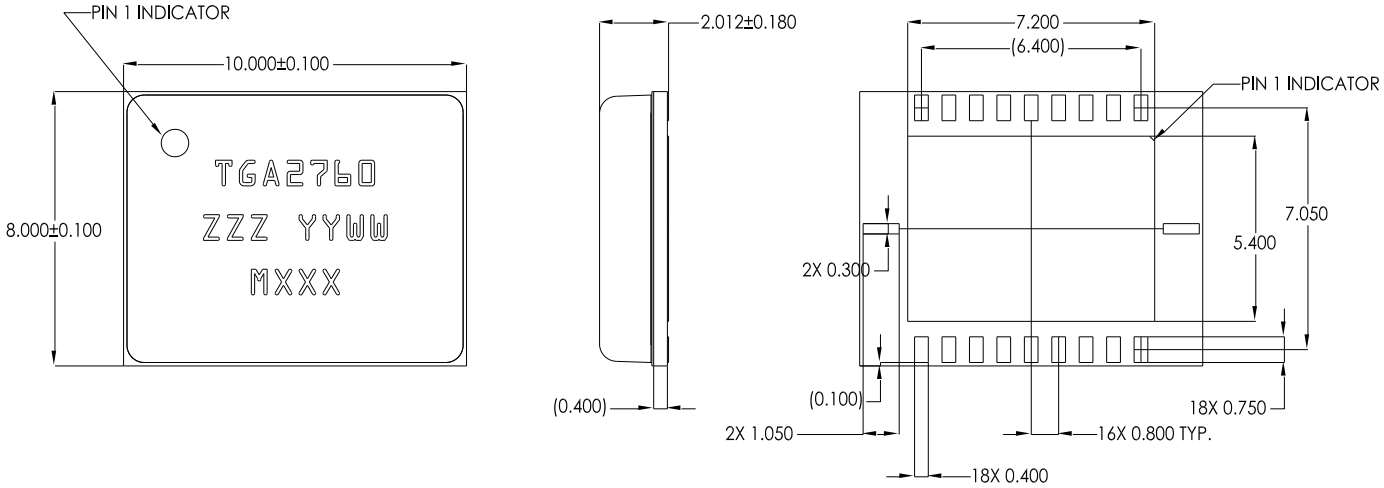
Bill of Material

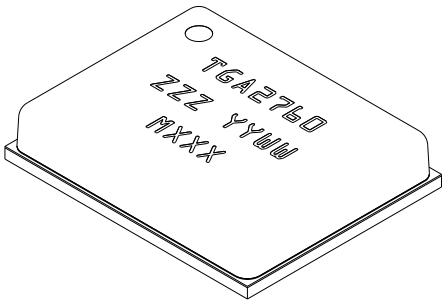
Ref Des	Value	Description	Manufacturer	Part Number
C1 – C10	100 pF	Cap, 0402, +50 V, 5%, COG	various	
C11 – C22	1 µF	Cap, 0603, +50 V, 5%, X5R	various	
R1 – R6	10 Ω	Res, 0402, 1/16W, 5%, SMD	various	
U1		9.5 – 12 GHz Power Amplifier	Triquint	TGA2760-SM

Mechanical Information

Package Marking and Dimensions

All dimensions are in millimeters.



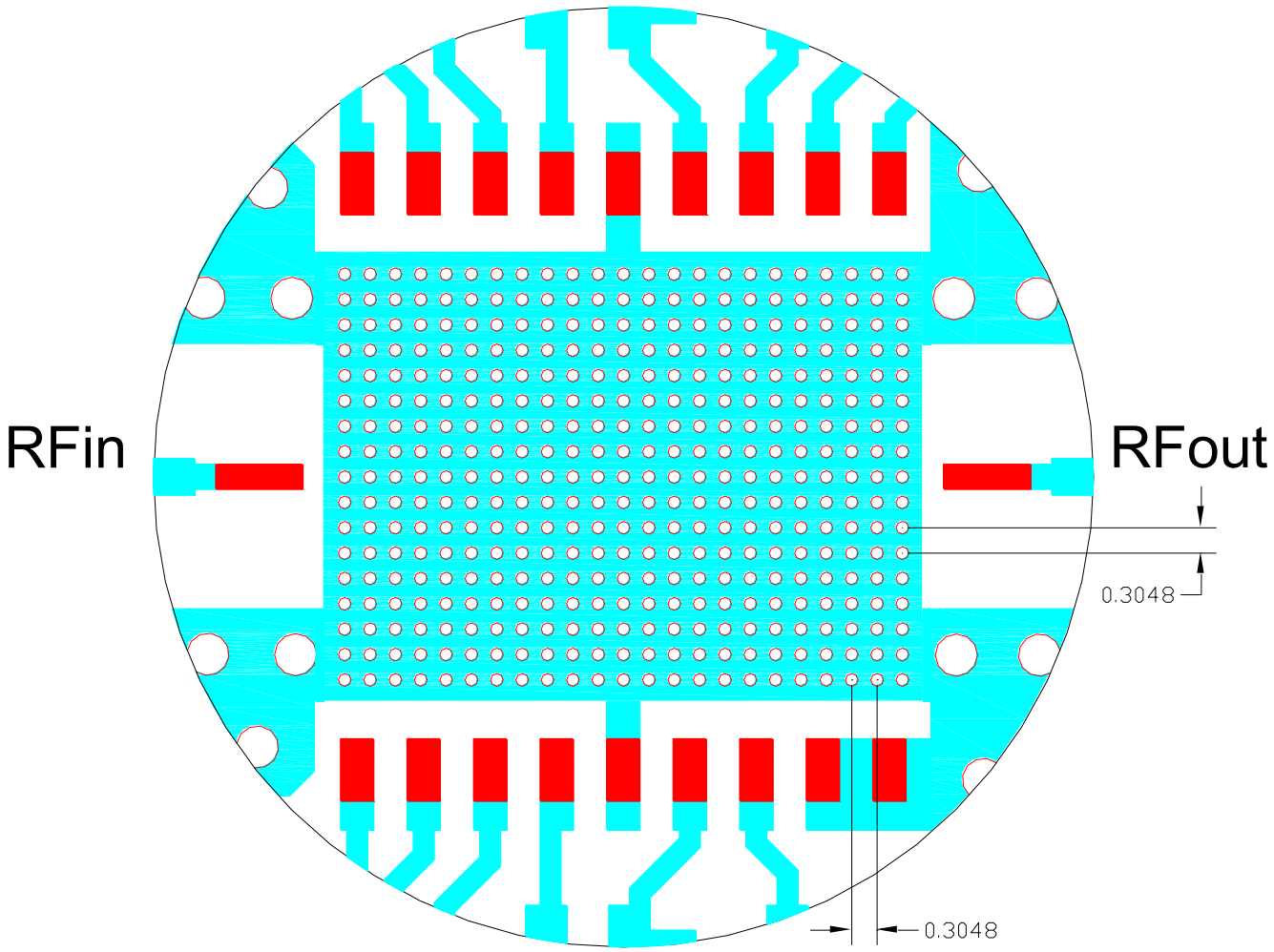


The TGA2760-SM will be marked with the “2760” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the year the part was manufactured, the “WW” is the work week, the “ZZZ” is a unique serial number, and MXXX represents assembly lot number.

This package is lead-free/RoHS-compliant with an embedded heat spreader, and the plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245 °C reflow temperature) soldering processes.

Mechanical Information

PCB Mounting Pattern



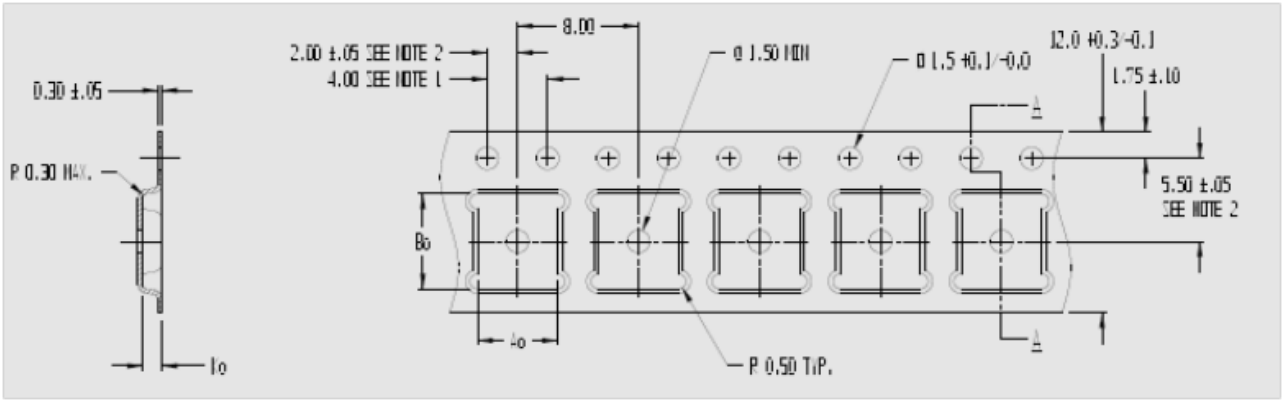
Notes:

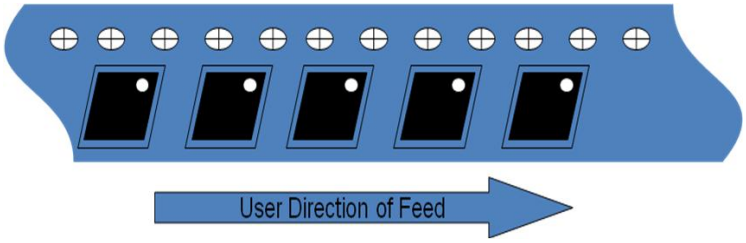
1. The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
2. Ground vias are critical for the proper performance of this device. Vias should have a final plated thru diameter of .1524 mm (.006”).
3. For best thermal performance, vias under the ground paddle should be copper filled.

Tape and Reel Information

Standard T/R size = 500 pieces on a 7” reel.

Material		Cavity (mm)				Distance Between Centerline (mm)		Carrier Tape (mm)	Cover Carrier (mm)
Vendor	Vendor P/N	Length (A0)	Width (B0)	Depth (K0)	Pitch (P1)	Length direction (P2)	Width Direction (F)	Width (W)	Width (W)
Tek-Pak	QFN0500X0500 F-L500	9.8	8.3	1.2	12.0	2.00	5.50	12.0	24.0





Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Charge Device Model (CDM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

MSL Rating: TBD
Test: 260 °C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with lead-free soldering processes, 260 °C maximum reflow temperature.

Package lead plating: NiAu.

The use of no-clean solder to avoid washing after soldering is recommended.

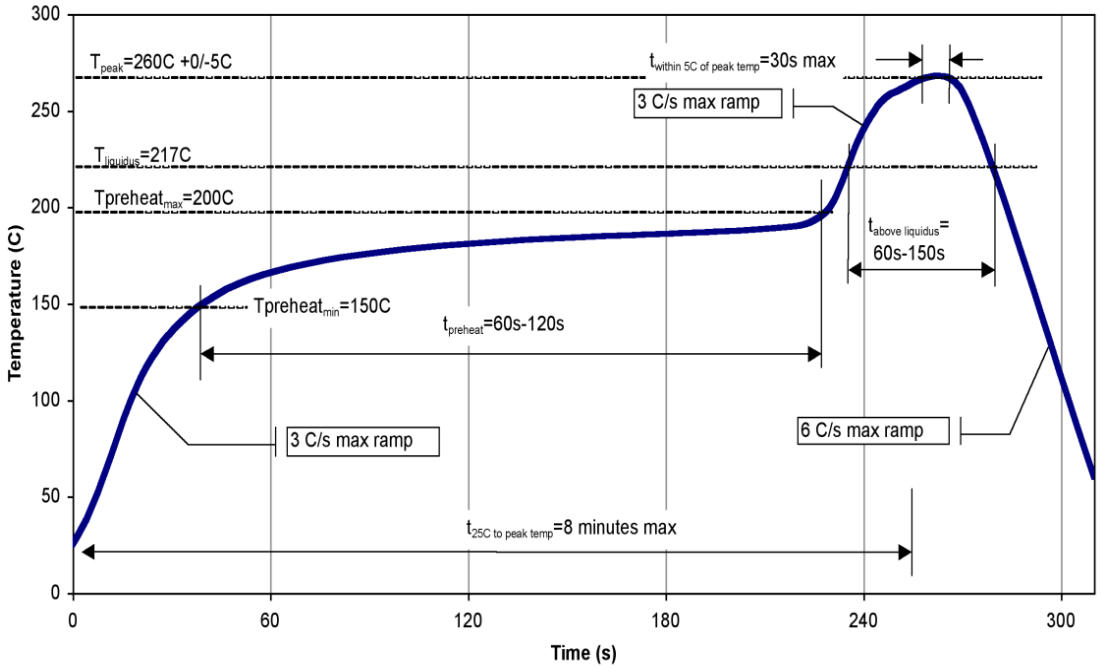
RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Recommended Solder Temperature Profile



Contact Information

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Web: www.qorvo.com

For technical questions and application information: **Email:** info-networks@tqs.com

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