MULTI SPIDER
ORG4572
GNSS RECEIVER MODULE

DATASHEET

INDEX

TABLE INDEX

FIGURE INDEX

1. SCOPE

This document describes the features and specifications of the ORG4572 GNSS receiver module.

2. DISCLAIMER

All trademarks are properties of their respective owners.

Performance characteristics listed in this document do not constitute a warranty or guarantee of product performance. OriginGPS assumes no liability or responsibility for any claims or damages arising out of the use of this document, or from the use of integrated circuits based on this document.

OriginGPS assumes no liability or responsibility for unintentional inaccuracies or omissions in this document.

OriginGPS reserves the right to make changes in its products, specifications and other information at any time without notice.

OriginGPS navigation products are not recommended to use in life saving or life sustaining applications.

3. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.

4. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.

5. CONTACT INFORMATION

Support - info@origingps.com or Online Form

Marketing and sales - marketing@origingps.com

Web – www.origingps.com

6. RELATED DOCUMENTATION

№	DESCRIPTION	DOCUMENT NAME	ISSUED BY
1	Datasheet of the ORG4572 Evaluation Kit	ORG4572-EVK-DS	OriginGPS
2	Software User Manual	ORG4572-SW	OriginGPS
3	NMEA Protocol Reference Manual	ORG4572-NMEA	OriginGPS
4	One Socket Protocol Reference Manual	ORG4572-OSP	OriginGPS
5	Host Interface Application Note	ORG4572-IF-APNT	OriginGPS
6	Low Power Modes Application Note	ORG4572-LP-APNT	OriginGPS
7	MEMS Sensors Interface Application Note	ORG4572-MEMS-APNT	OriginGPS
8	Jammer Detector and Remover Application Note	ORG4572-JDR-APNT	OriginGPS
9	Client Generated Extended Ephemeris App. Note	ORG4572-CGEE-APNT	OriginGPS
10	Server Generated Extended Ephemeris App. Note	ORG4572-SGEE-APNT	OriginGPS
11	Ephemeris Push Application Note	ORG4572-EP-APNT	OriginGPS

TABLE 1 – RELATED DOCUMENTATION

7. REVISION HISTORY

REVISION	DATE	CHANGE DESCRIPTION
A00	November 23, 2013	First release

TABLE 2 – REVISION HISTORY

8. GLOSSARY

A-GNSS Assisted **GNSS**
BPF Band **P**ass **F**ilter
CE European Community conformity mark
CGEE™ Client **G**enerated **E**xtended **E**phemeris
COMPASS PRC GNSS (same as **BDS B**ei**D**ou-2 Navigation Satellite **S**ystem)
CMOS Complementary **M**etal-**O**xide **S**emiconductor
EMC Electro-**M**agnetic **C**ompatibility
ESD Electro-**S**tatic **D**ischarge
EVB Evaluation **B**oard
EVK Evaluation **K**it
FCC Federal **C**ommunications **C**ommission
GALILEO EU GNSS
GLONASS Global **Na**vigation **S**atellite **S**ystem
GNSS Global **N**avigation **S**atellite **S**ystem
GPS Global **P**ositioning **S**ystem
IC Integrated **C**ircuit
I^2C Inter-**I**ntegrated **C**ircuit
ISO International **O**rganization for **S**tandardization
EGNOS European **G**eostationary **N**avigation **O**verlay **S**ervice
LDO Low **D**ropo**o**ut regulator
LGA Land **G**rid **A**rray
LNA Low **N**oise **A**mplifier
MSAS Multi-functional **S**atellite **A**ugmentation **S**ystem
MSL Moisture **S**ensitivity **L**evel
NMEA National **M**arine **E**lectronics **A**ssociation
NFZ™ Noise-**F**ree **Z**ones **S**ystem
MEMS Micro**E**lectro**M**echanical **S**ystems
PCB Printed **C**ircuit **B**oard
PPS Pulse **P**er **S**econd
QZSS Quasi-**Z**enith **S**atellite **S**ystem
RF Radio **F**requiency
REACH Registration, **E**valuation, **A**uthorisation and Restriction of **Ch**emical substances
RHCP Right-**H**and **C**ircular **P**olarized
RoHS Restriction of **H**azardous **S**ubstances directive
ROM Read-**O**nly **M**emory
RTC Real-**T**ime **C**lock
SAW Surface **A**coustic **W**ave
SBAS Satellite-**B**ased **A**ugmentation **S**ystems
SGEE™ Server **G**enerated **E**xtended **E**phemeris
SIP System **I**n **P**ackage
SMD Surface **M**ounted **D**evice
SMT Surface-**M**ount **T**echnology
SOC System **O**n **C**hip
SPI Serial **P**eripheral **I**nterface
TCXO Temperature-**C**ompensated Crystal **O**scillator
TTL Transistor-**T**ransistor **L**ogic
TTFF Time **T**o **F**irst **F**ix
UART Universal **A**synchronous **R**eceiver/**T**ransmitter
WAAS Wide **A**rea **A**ugmentation **S**ystem

9. ABOUT SPIDER FAMILY

OriginGPS GNSS receiver modules have been designed to address markets where size, weight, stand-alone operation, highest level of integration, power consumption and design flexibility - all are very important.

OriginGPS' Spider family breaks size barrier, offering the industry's smallest fully-integrated, highly-sensitive GPS / GNSS modules.

Spider family features OriginGPS' proprietary NFZ™ technology for high sensitivity and noise immunity even under marginal signal condition, commonly found in urban canyons, under dense foliage or when the receiver's position in space rapidly changes.

Spider family enables the shortest TTM (Time-To-Market) with minimal design risks.

Just connect an antenna and power supply on a 2-layer PCB.

10. ABOUT MULTI SPIDER MODULE

Multi Spider is a complete SiP featuring miniature LGA SMT footprint designed to commit unique integration features for high volume cost sensitive applications.

Designed to support ultra-compact applications such as smart watches, wearable devices, trackers and digital cameras, ORG4572module is a miniature multi-channel GPS/ GLONASS with SBAS, QZSS and other regional overlay systems receiver that continuously tracks all satellites in view, providing real-time positioning data in industry's standard NMEA format.

ORG4572 module offers superior sensitivity and outstanding performance, achieving rapid TTFF in less than one second, accuracy of approximately one meter, and tracking sensitivity of -165dBm.

Sized only 7mm x 7mm the ORG4572 GNSS module is pin and footprint compatible with OriginGPS' popular ORG4472 GPS module.

ORG4572 module integrates LNA, SAW filter, TCXO, RTC crystal and RF shield with market-leading SiRFstarV™ GNSS SoC.

ORG4572 module is capable to decode extremely weak satellite signals simultaneously from GPS and GLONASS thereby offering best-in-class positioning availability, unparalleled accuracy and extremely fast fixes under challenging signal conditions, such as in built-up urban areas, dense foliage or even indoor.

Internal GNSS SoC incorporating high-performance microprocessor and sophisticated GNSS firmware keeps positioning payload off the host allowing integration in embedded solutions even with low computing resources.

Innovative architecture can detect changes in context, temperature, and satellite signals to achieve a state of near continuous availability by maintaining and opportunistically updating its internal fine time, frequency, and ephemeris data while consuming mere microwatts of battery power.

11. ABOUT ORIGINGPS

OriginGPS is a world leading designer, manufacturer and supplier of miniature positioning modules, antenna modules and antenna solutions.

OriginGPS modules introduce unparalleled sensitivity and noise immunity by incorporating Noise Free Zone system (NFZ™) proprietary technology for faster position fix and navigation stability even under challenging satellite signal conditions.

Founded in 2006, OriginGPS is specializing in development of unique technologies that miniaturize RF modules, thereby addressing the market need for smaller wireless solutions.

12. DESCRIPTION

12.1. FEATURES

- Autonomous operation
- Pin compatible with ORG4472 GPS module
- OriginGPS Noise Free Zone System (NFZ™) technology
- Fully integrating:
  GNSS LNA, GNSS SAW Filter, TCXO, RTC Crystal, RF Shield, GNSS SoC, Power Management Unit
- Active or Passive antenna support
- GPS L1 1575.42 frequency, C/A code
- GLONASS L1 FDMA 1598-1606MHz frequency band, SP signal
- SBAS (WAAS, EGNOS, MSAS) and QZSS support
- Concurrent tracking of multiple constellations
- 52 channels
- Ultra-high Sensitivity down to -165dBm enabling Indoor Tracking
- TTFF of < 1s in 50% of trials under Hot Start conditions
- Low Power Consumption of < 15mW in ATP™ mode
- High Accuracy of < 1.5m in 50% of trials
- High update rate of 5Hz, 1Hz by default
- Autonomous A-GNSS by Client Generated Extended Ephemeris (CGEE™) for non-networked devices
- Predictive A-GNSS by Server Generated Extended Ephemeris (SGEE™) for connected devices
- Ephemeris Push™ for storing and loading broadcast ephemeris
- Host controlled power saving mode
- Self-managed low power modes - ATP™, PTF™, APM™ and SiRFAware™ MPM
- Almanac Based Positioning (ABP™)
- Multipath and cross-correlation mitigation
- Active Jammer Detector and Remover
- Smart Data Logging to external memory
- Fast Time Synchronization for rapid single satellite time solution
- ARM7® microprocessor system
- Selectable UART, SPI or I^2C host interface
- NMEA protocol by default, switchable into One Socket Protocol (OSP™).
- Programmable baud rate and messages rate
- 1PPS output
- Smart sensors auxiliary I^2C interface
- Flash memory auxiliary SPI interface
- Antenna input matched 50Ω
- Single voltage supply
- Miniature LGA footprint of 7mm x 7mm
- Surface Mount Device (SMD)
- Optimized for automatic assembly and reflow equipment
- Operating from -40°C to +85°C
- FCC, CE, VCCI certified
- RoHS II/REACH compliant

12.2. ARCHITECTURE

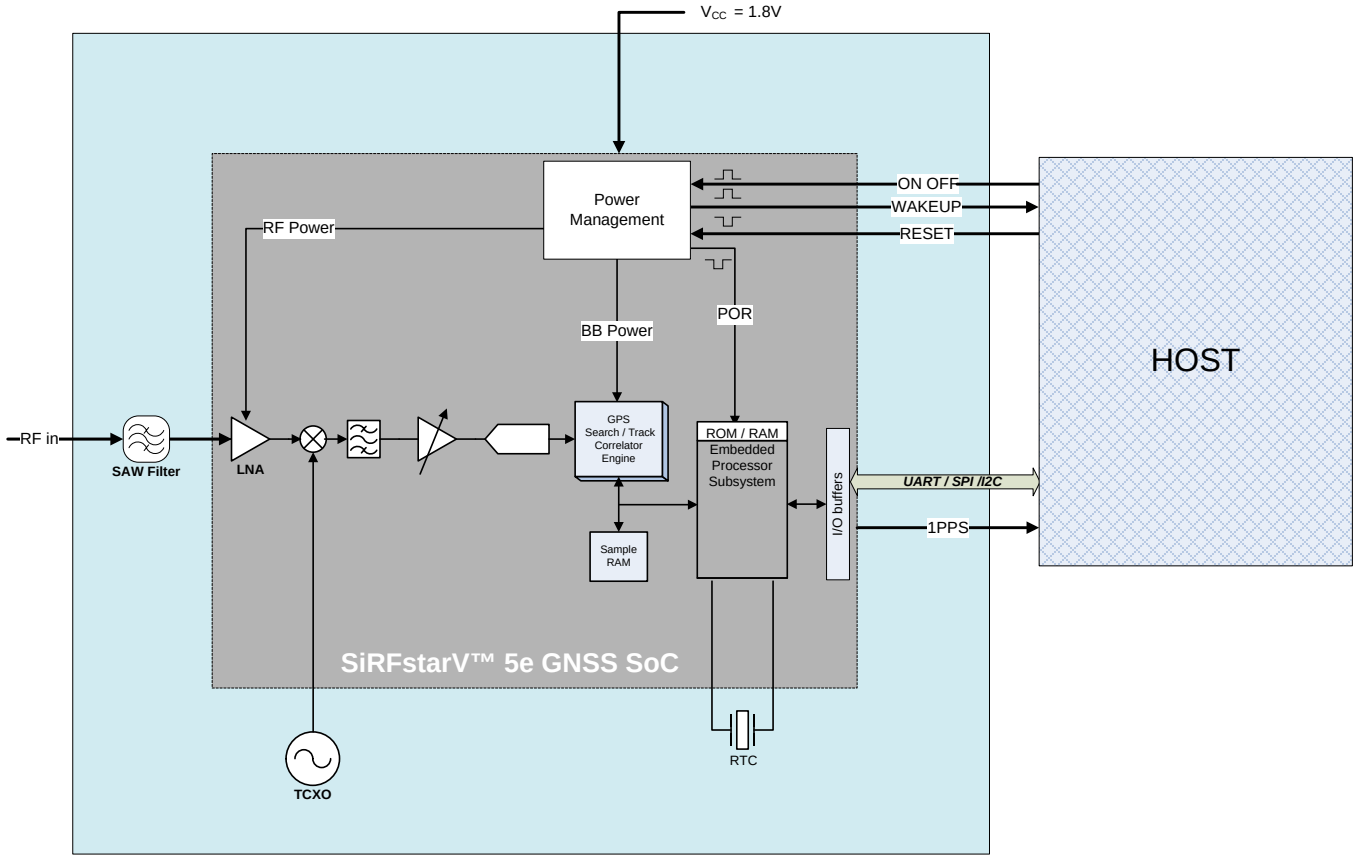


FIGURE 1 – ORG4572 ARCHITECTURE

- **GNSS SAW Filter**
  Band-Pass SAW filter eliminates out-of-band signals that may interfere to GNSS reception.
  GNSS SAW filter is optimized for low insertion-loss in GNSS band and low return-loss outside it.
- **GNSS LNA**
  The integrated LNA amplifies the GNSS signal to meet RF down converter input threshold.
  Noise Figure optimized design was implemented to provide maximum sensitivity.
- **TCXO**
  Highly stable 26 MHz oscillator controls the down conversion process in RF block of the GNSS SoC.
  Characteristics of this component are important factors for higher sensitivity, shorter TTFF and better navigation stability.
- **RTC crystal**
  Tuning fork quartz crystal with very tight specifications is necessary for maintaining Hot Start and Warm Start capabilities of the module.
- **RF Shield**
  RF enclosure avoids external interference from compromising sensitive circuitry inside the module.
  RF shield also blocks module's internal high frequency emissions from being radiated.
- **SiRFstarV™ 5e GNSS SoC**
  CSR 5e is a 5-th generation SiRFstar™ product.
  It is a hybrid positioning processor that combines GPS, GLONASS, SBAS and MEMS sensor data to provide a high performance navigation solution.
  SiRFstarV™ 5e is a full SoC built on a low-power RF CMOS single-die, incorporating GNSS RF, GNSS baseband, integrated navigation solution software and ARM® processor.

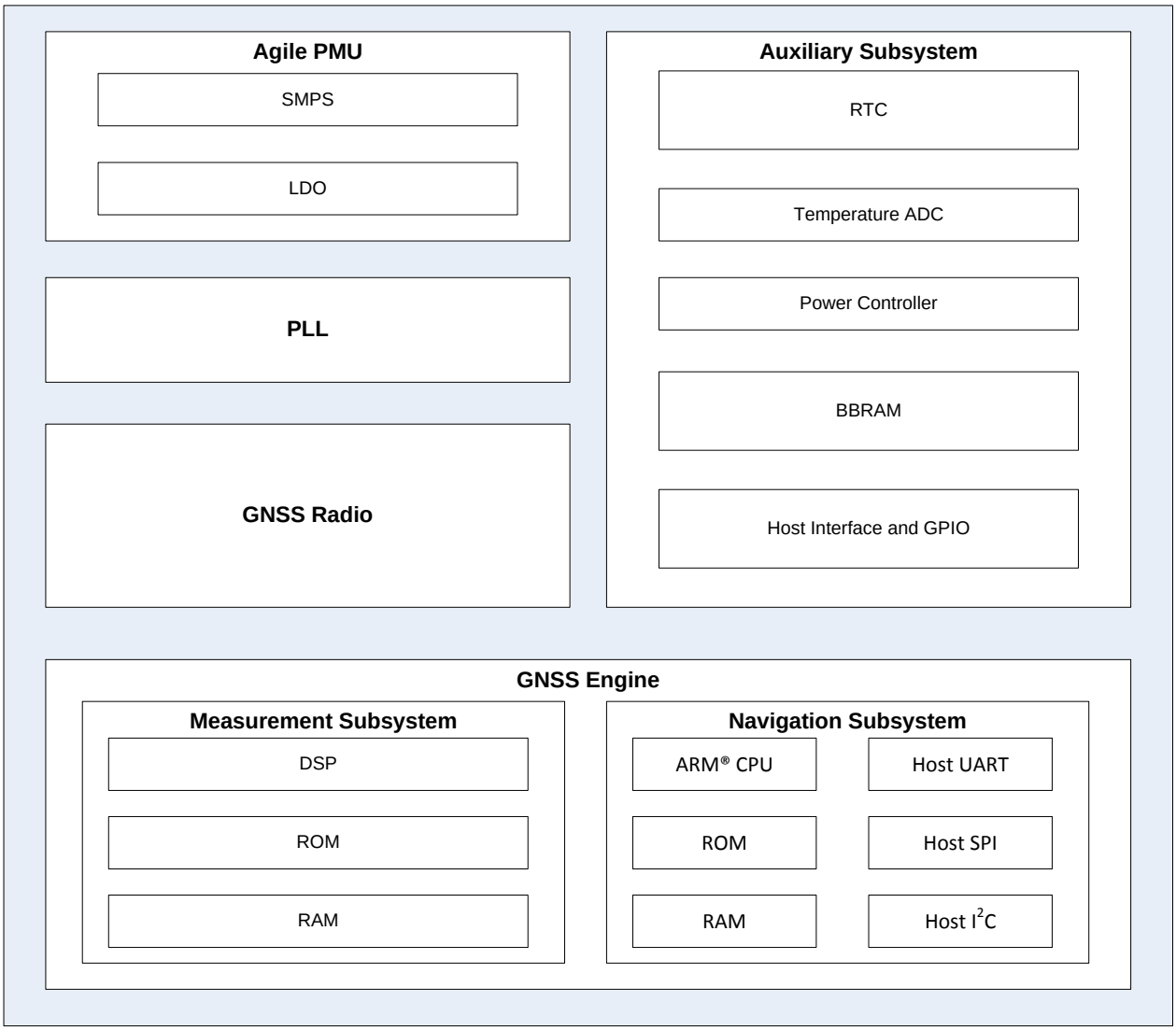


FIGURE 2 – SiRFstarV™ 5e GNSS SoC BLOCK DIAGRAM

SiRFstarV™ 5e SoC includes the following units:

- GNSS radio subsystem containing single input dual receive paths for concurrent GPS and GLONASS, harmonic-reject double balanced mixer, fractional-N synthesizer, integrated self-calibrating filters, IF VGA with AGC, high-sample rate ADCs with adaptive dynamic range.
- Measurement subsystem including DSP core for GNSS signals acquisition and tracking, interference scanner and detector, wideband and narrowband interference removers, multipath and cross-correlation detectors, dedicated DSP code ROM and DSP cache RAM.
  Measurement subsystem interfaces GNSS radio subsystem.
- Navigation subsystem comprising ARM7® microprocessor system for position, velocity and time solution, program ROM, data RAM, cache and patch RAM, MEMS sensor driver, SPI flash driver, host interface UART, SPI and I^2C drivers.
  Navigation subsystem interfaces measurement subsystem.
- Auxiliary subsystem containing RTC block and health monitor, temperature sensor for reference clock compensation, battery-backed SRAM for satellite data storage, voltage supervisor with POR, PLL controller, GPIO controller, 48-bit RTC timer and alarms, CPU watchdog monitor.
  Auxiliary subsystem interfaces navigation subsystem, PLL and PMU subsystems.
- PMU subsystem containing voltage regulators for RF and baseband domains.

13. ELECTRICAL SPECIFICATIONS

13.1. ABSOLUTE MAXIMUM RATINGS

Stresses exceeding Absolute Maximum Ratings may damage the device.

PARAMETER			SYMBOL	MIN	MAX	UNIT
Power Supply Voltage			V_{CC}	-0.30	+2.20	V
Power Supply Current[1]			I_{CC}		150	mA
RF Input Voltage			V_{RF}	-25	+25	V
I/O Voltage			V_{IO}	-0.30	+3.65	V
I/O Source/Sink Current			I_{IO}	-4	+4	mA
ESD Rating	I/O pads	HBM[2] method	$V_{IO(ESD)}$	-2000	+2000	V
		CDM[3] method		-400	+400	V
	RF input pad	HBM[2] method	$V_{RF(ESD)}$	-500	+500	V
		CDM[3] method		-100	+100	V
RF Input Power	f_{IN} = 1560MHz÷1630MHz		P_{RF}		+10	dBm
	f_{IN} <1560MHz, >1630MHz				+25	dBm
Power Dissipation			P_D		350	mW
Operating Temperature			T_{AMB}	-45	+90	°C
Storage Temperature			T_{ST}	-55	+150	°C
Lead Temperature[4]			T_{LEAD}		+260	°C

TABLE 3 – ABSOLUTE MAXIMUM RATINGS

Notes:

1. Inrush current of up to 150mA for about 20µs duration.
2. Human Body Model (HBM) contact discharge per ANSI/ESDA/JEDEC JS-001.
3. Charged Device Model (CDM) contact discharge per JEDEC EIA/JESD22-C101.
4. Lead temperature at 1mm from case for 10s duration.

13.2. RECOMMENDED OPERATING CONDITIONS

Exposure to stresses above the Recommended Operating Conditions may affect device reliability.

PARAMETER	SYMBOL	MODE / PAD	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power supply voltage	V_{CC}	V_{CC}		+1.71	+1.80	+1.89	V
Power Supply Current[1]	I_{CC}	Acquisition	GPS		40		mA
			GPS + GLONASS		50		mA
		Tracking	GPS		36		mA
			GPS + GLONASS		47		mA
		ATP™ Tracking[2]			8		mA
		CPU only[3]			15		mA
		Standby[3]				100	µA
		MPM™[4]			0.5		mA
		Hibernate				50	µA
Input Voltage Low State	V_{IL}	GPIO		-0.30		+0.40	V
Input Voltage High State	V_{IH}			$0.70 \cdot V_{CC}$		+3.60	V
Output Voltage Low State	V_{OL}		I_{OL} = 2mA			+0.40	V
Output Voltage High State	V_{OH}		I_{OH} = -2mA	$0.75 \cdot V_{CC}$			V
Input Capacitance	C_{IN}				5		pF
Internal Pull-up Resistor	R_{PU}			0.11	1.00	2.75	MΩ
Internal Pull-down Resistor	R_{PD}			0.11	1.00	2.80	MΩ
Input Leakage Current	$I_{IN(leak)}$		V_{IN} = 1.8V or 0V	-10		+10	µA
Output Leakage Current	$I_{OUT(leak)}$		V_{OUT} = 1.8V or 0V	-10		+10	µA
Input Impedance	Z_{IN}	RF Input	f_{IN} = 1575.5MHz		50		Ω
Input Return Loss	R_{LIN}				-7		dB
Input Power Range	P_{IN}		GPS or GLONASS	-165		-110	dBm
Input Frequency Range	f_{IN}			1560		1620	MHz
Operating Temperature	T_{AMB}			-40	+25	+85	°C
Storage Temperature	T_{ST}			-55	+25	+125	°C
Relative Humidity	RH		T_{AMB}	5		95	%

TABLE 4 – RECOMMENDED OPERATING CONDITIONS

Notes:

1. Typical I_{CC} values are under signal conditions of -130dBm and ambient temperature of +25°C.
2. Adaptive Trickle Power (ATP™) mode 100:1.
3. Transitional states of ATP™ power saving mode.
4. Average current during SiRFAware™ Micro Power Mode (MPM™).

14. PERFORMANCE

14.1. ACQUISITION TIME

TTFF (Time To First Fix) – is the period of time from the module's power-up till position estimation.

14.1.1. HOT START

Hot Start results either from a software reset after a period of continuous navigation or a return from a short idle period that was preceded by a period of continuous navigation.
During Hot Start all critical data (position, velocity, time, and satellite ephemeris) is valid to the specified accuracy and available in RAM.

14.1.2. WARM START

Warm Start typically results from user-supplied position and time initialization data or continuous RTC operation with an accurate last known position available in RAM.
In this state position and time data are present and valid, but satellite ephemeris data validity has expired.

14.1.3. COLD START

Cold Start occurs when satellite ephemeris data, position and time data are unknown.

14.1.4. AIDED START

Aided Start is a method of effectively reducing TTFF by making every start Hot or Warm.

OPERATION[1]	MODE	VALUE	UNIT
Hot Start		< 1	s
Aided Start		< 10	s
Warm Start	GPS + GLONASS	< 26	s
	GPS	< 32	s
Cold Start	GPS + GLONASS	< 27	s
	GPS	< 35	s
Signal Reacquisition		< 1	s

TABLE 5 – ACQUISITION TIME

14.2. SENSITIVITY

OPERATION	MODE	VALUE	UNIT
Tracking	GPS	-165	dBm
	GLONASS	-165	dBm
Navigation	GPS	-162	dBm
	GLONASS	-158	dBm
Cold Start	GPS	-146	dBm

TABLE 6 – SENSITIVITY

Notes:

1. Module is static under signal conditions of -130dBm and ambient temperature of +25°C.

14.3. ACCURACY

PARAMETER		FORMAT	MODE	VALUE	UNIT
Position[1]	Horizontal	CEP (50%)	GPS + GLONASS	< 1.5	m
			GPS + SBAS	< 2.0	m
			GPS	< 2.5	m
		2dRMS (95%)	GPS + GLONASS	< 3.0	m
			GPS + SBAS	< 4.0	m
			GPS	< 5.0	m
	Vertical	VEP (50%)	GPS + GLONASS	< 2.5	m
			GPS + SBAS	< 3.5	m
			GPS	< 4.0	m
		2dRMS (95%)	GPS + GLONASS	< 5.0	m
			GPS + SBAS	< 6.5	m
			GPS	< 7.5	m
Velocity[2]	over ground	50% of samples		< 0.01	m/s
Heading	to north	50% of samples		< 0.01	°
Time[1]		RMS jitter	1 PPS	< 40	ns

TABLE 7 – ACCURACY

14.4. DYNAMIC CONSTRAINS

PARAMETER[3]	MAXIMUM	
Velocity	515 m/s	1,000 knots
Acceleration	4g	
Altitude	18,288 m	60,000 ft.

TABLE 8 – DYNAMIC CONSTRAINS

Notes:

1. Module is 24-hrs. static under signal conditions of -130dBm and ambient temperature of +25°C.
2. Speed over ground ≤ 30m/s.
3. Standard dynamic constrains according to regulatory limitations.

15. POWER MANAGEMENT

15.1. POWER CONSUMPTION

OPERATION	MODE	VALUE	UNIT
Acquisition	GPS	72	mW
	GPS + GLONASS	90	mW
Tracking	GPS	65	mW
	GPS + GLONASS	85	mW
Low Power Tracking – ATP™ 100ms Full Power : 1s tracking		14	mW
Low Power Mode – MPM™		0.9	mW
Basic Power saving mode – 5min. Hibernate : 10s tracking		3	mW
Hibernate		0.09	mW

TABLE 9 – POWER CONSUMPTION

15.2. POWER STATES

15.2.1. FULL POWER ACQUISITION

ORG4572 module stays in Full Power Acquisition state until a reliable position solution is made. Switching to GPS-only mode turns off GLONASS RF block lowering power consumption.

15.2.2. FULL POWER TRACKING

Full Power Tracking state is entered after a reliable position solution is achieved.
During this state the processing is less intense compared to Full Power Acquisition, therefore power consumption is lower. Full Power Tracking state with navigation update rate at 5Hz consumes more power compared to default 1Hz navigation.

15.2.3. CPU ONLY

CPU Only is the transitional state of ATP™ power saving mode when the RF and DSP sections are partially powered off. This state is entered when the satellites measurements have been acquired, but navigation solution still needs to be computed.

15.2.4. STANDBY

Standby is the transitional state of ATP™ power saving mode when RF and DSP sections are completely powered off and baseband clock is stopped.

15.2.5. HIBERNATE

ORG4572 module boots into Hibernate state after power supply applied.
During this state RF, DSP and baseband sections are completely powered off leaving only RTC and Battery-Backed RAM running.
ORG4572 will perform Hot Start if stayed in Hibernate state less than 4 hours from last valid position solution.

15.3. BASIC POWER SAVING MODE

Basic power saving mode is elaborating host in straightforward way for controlling transfers between Full Power and Hibernate states.
Current profile of this mode has no hidden cycles of satellite data refresh.
Host may condition transfers by tracking duration, accuracy, satellites in-view or other parameters.

15.4. SELF MANAGED POWER SAVING MODES

ORG4572 module has several self-managed power saving modes tailored for different use cases. These modes provide several levels of power saving with degradation level of position accuracy. Initial operation in Full Power state is a prerequisite for accumulation of satellite data determining location, fine time and calibration of reference clocks.

15.4.1. ADAPTIVE TRICKLE POWER (ATP™)

ATP™ is best suited for applications that require navigation solutions at a fixed rate as well as low power consumption and an ability to track weak signals.
This power saving mode provides the most accurate position among self-managed modes.
In this mode ORG4572 module is intelligently cycled between Full Power, CPU Only and Standby states optimizing current profile for low power operation.

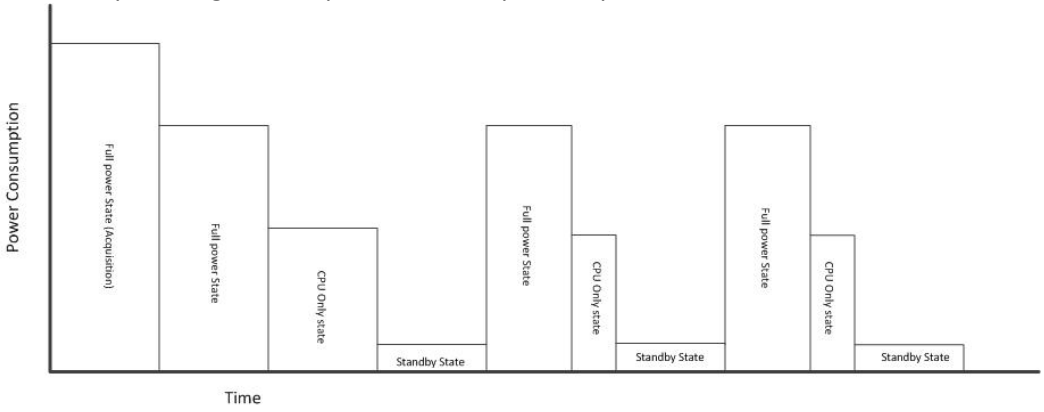


FIGURE 3 – ATP™ TIMING

15.4.2. PUSH TO FIX (PTF™)

PTF™ is best suited for applications that require infrequent navigation solutions.
In this mode ORG4572 module is mostly in Hibernate state, drawing < 50µA of current, waking up for satellite ephemeris data refresh in fixed periods of time.
PTF™ period can be anywhere between 10 seconds and 2 hours.
Host can initiate an instant position report by toggle the ON_OFF pad to wake up the module.
During fix trial ORG4572 will stay in Full Power state until good position solution is estimated or pre-configured timeout for it has expired.

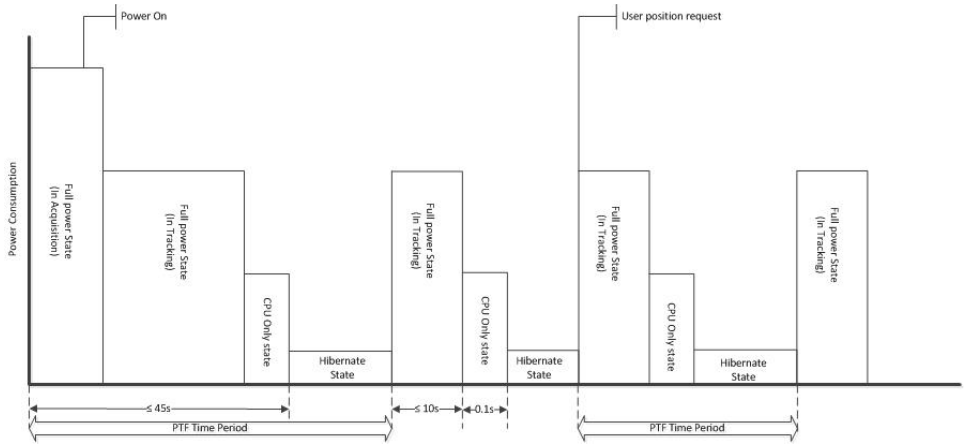
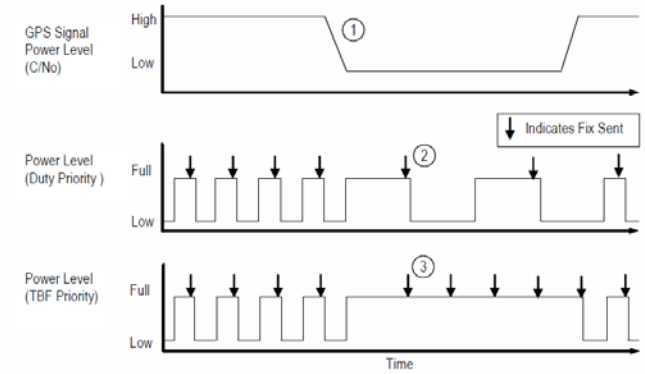


FIGURE 4 – PTF™ TIMING

15.4.3. ADVANCED POWER MANAGEMENT (APM™)

APM™ allows power savings while ensuring that the Quality of the Solution (QoS) in maintained when signals level drop.
In APM™ mode the module is intelligently cycled between Full Power and Hibernate states.
In addition to setting the position report interval, a QoS specification is available that sets allowable error estimates and selects priorities between position report interval and more power saving.
The user may select between Duty Cycle Priority for more power saving and Time Between Fixes (TBF) priority with defined or undefined maximum horizontal error.
TBF range is from 10s to 180s between fixes, Power Duty Cycle range is between 5% to 100%.
Maximum position error is configurable between 1 to 160m.
The number of APM™ fixes is configurable up to 255 or set to continuous.



1. GPS signal level drops (e.g. user walks indoors)
2. Lower signal results in longer ON time. To maintain Duty Cycle Priority, OFF time is increased.
3. Lower signal means missed fix. To maintain future TBFs, the module goes info Full Power state until signal levels improve.

FIGURE 5 – APM™ TIMING

15.4.4. SiRFAWARE™ MICRO POWER MODE (MPM™)

While in SiRFAware™ MPM the module determines how much signal processing to do and how often to do it, so that the module is always able to do a fast hot start (TTFF < 2 s) on demand.
ORG4572 will wake up (typically twice an hour) for 18-24s to collect new ephemeris data.
Ephemeris data collection operation consumes power equal to Full Power state.
Additionally, ORG4572 will wake up once every 1 to 10 minutes for 250ms to update internal navigation state and clocks calibration. Capture/Update operation consumes about 0.2mA, rest of time ORG4572 stays in Hibernate state.
Host can toggles ON_OFF to wake-up the module and initiate fix trial.
After valid fix is available, the host can turn the module back into MPM™ by re-sending the command.
Average current consumption over long period during MPM™ is about 500µA.

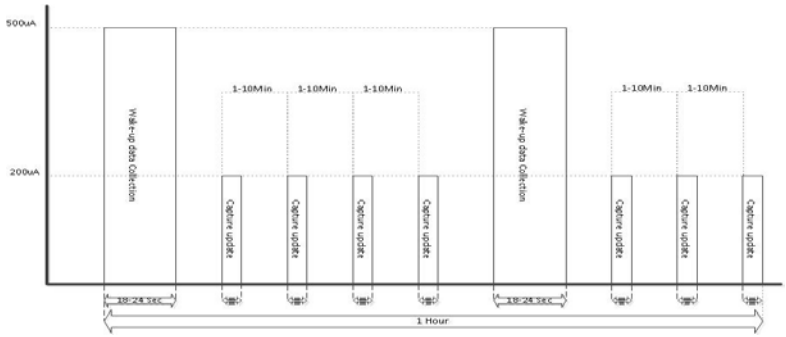


FIGURE 6 – MPM™ TIMING

16. EXTENDED FEATURES

16.1. ALMANAC BASED POSITIONING (ABP™)

With ABP™ mode enabled, the user can get shorter Cold Start TTFF as a tradeoff with the accuracy. When no sufficient ephemeris data is available to calculate an accurate solution, a coarse solution will be provided where the position is calculated based on one or more of the GPS satellites having their states derived from the almanac data.
Data source for ABP™ may be either stored factory almanac, broadcasted or pushed almanac.

16.2. ACTIVE JAMMER DETECTOR AND REMOVER

Jamming Detector is an embedded DSP block that detects interference signals in GPS L1 and GLONASS L1 bands.
Jamming Remover is another DPS block that sort-out Jamming Detector output mitigating up to 8 interference signals of Continuous Wave (CW) type up to 80dB-Hz each.

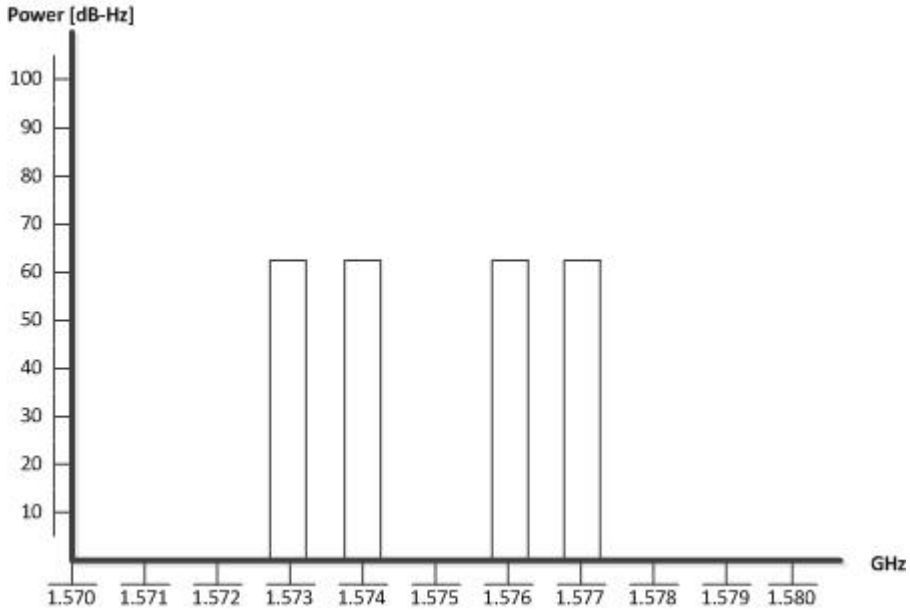


FIGURE 7 – ACTIVE JAMMER DETECTOR FREQUENCY PLOT

16.3. CLIENT GENERATED EXTENDED EPHEMERIS (CGEE™)

CGEE™ feature allows shorter TTFF by providing predicted (synthetic) ephemeris files created within a lost host system from previously received satellite ephemeris.
The prediction process requires good receipt of broadcast ephemeris data for all satellites.
EE files created this way are good for up to 3 days and then expire.
CGEE™ feature requires avoidance of power supply removal.
CGEE™ data files are stored and managed by host.

16.4. SERVER GENERATED EXTENDED EPHEMERIS

SGEE™ enables shorter TTFF by fetching EE files downloaded from OriginGPS EE distribution server.
Downloaded EE files are stored and managed by host.
There is an SOW based one-time NRE charge for set-up and access to OriginGPS EE distribution server or there is a per-unit charge for each module within SGEE™ deployment.
GPS EE files are provided with look-ahead of 7, 14 or 31 days.
GLONASS EE files are provided with look-ahead of 7 or 14 days.

17. INTERFACE

17.1. PAD ASSIGNMENT

PAD	NAME	FUNCTION			DIRECTION
1	GND	RF Ground			Power
2	RF_IN	Antenna Signal Input			Analog Input
3	GND	RF Ground			Power
4	WAKEUP	Power Status			Output
5	$\overline{\text{RESET}}$	Asynchronous Reset			Input
6	$\overline{\text{CTS}}$	Interface Select 1	UART Clear To Send	SPI Clock	Bi-directional
7	$\overline{\text{RTS}}$	Interface Select 2	UART Ready To Send	SPI Chip Select	Bi-directional
8	RX	UART Receive	SPI Data In	I^2C Data	Bi-directional
9	ON_OFF	Power State Control			Input
10	1PPS	UTC Time Mark			Output
11	TX	UART Transmit	SPI Data Out	I^2C Clock	Bi-directional
12	V_{CC}	System Power			Power
13	NC	Not Connected			
14	GND	System Ground			Power
15	GPIO1	Baud Rate Select 1	Aux I^2C Data	Aux SPI Data In	Bi-directional
16	GPIO2	Baud Rate Select 2	Aux I^2C Clock	Aux SPI Clock	Bi-directional
17	NC	Not Connected			
18	NC	Not Connected			
19	GPIO3	Aux SPI Chip Select			Output
20	GPIO4	Aux SPI Data Out			Output

TABLE 10 – PIN-OUT

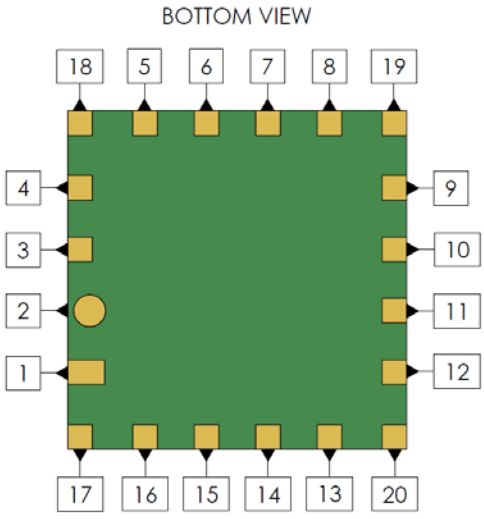


FIGURE 8 – PAD ASSIGNMENT

17.2. POWER SUPPLY

It is recommended to keep the power supply on all the time in order to maintain RTC block active and keep satellite data in RAM for fastest possible TTFF.

When V_{CC} is removed settings are reset to factory default and the receiver performs Cold Start on next power up.

17.2.1. V_{CC}

V_{CC} is 1.8V ±5% DC and must be provided from regulated power supply.

Typical I_{CC} is 50mA during acquisition.

Lower acquisition current is possible disabling GLONASS radio path by software command.

Inrush current is up to 150mA for about 20µs duration, V_{CC} can be dropped down to 1.66V.

Maximum I_{CC} current in Hibernate state is 50µA.

Output capacitors are critical when powering ORG4572 from switch-mode power supply.

Filtering is important to manage high alternating current flows on the power input connection.

An additional LC filter on ORG4572 power input may be needed to reduce system noise.

The high rate of ORG4572 input current change requires low ESR bypass capacitors.

Additional higher ESR output capacitors can provide input stability damping.

The ESR and size of the output capacitors directly define the output ripple voltage with a given inductor size. Large low ESR output capacitors are beneficial for low noise.

Voltage ripple below $50mV_{PP}$ allowed for frequencies between 100KHz to 1MHz.

Voltage ripple below $15mV_{PP}$ allowed for frequencies above 1MHz.

Higher voltage ripple may compromise ORG4572 performance.

17.2.2. GROUND

Ground pads must be connected to host PCB Ground with shortest possible traces or vias.

17.3. RF INPUT

RF input impedance is 50Ω.

Input is DC blocked ±25V.

ORG4572 module supports active or passive antenna.

In design with passive antenna attention should be paid on antenna layout.

Short trace of 50Ω controlled impedance should conduct GNSS signal from antenna to RF_IN pad.

ORG4572 is designed to track GNSS signal levels in a range down to close to the thermal noise floor.

At low signal levels, control of external noise sources is a significant factor in achieving the best performance of the receiver.

Designing with passive antenna require RF layout skills and can be challenging.

Contact OriginGPS for application specific recommendations and design review services.

DC bias voltage for active antenna can be externally applied on RF_IN trace through bias-T.

Active antenna net gain including conduction losses should not exceed 25dB.

DC bias voltage can be controlled by WAKEUP output through MOSFET or load switch.

In designs with external LNA, power enable can be controlled by ORG4572 WAKEUP output that by following module's power states assists reducing system current consumption.

17.4. CONTROL INTERFACE

17.4.1. ON_OFF

ON_OFF input is used to switch ORG4572 between different power states:

- While in Hibernate state, an ON_OFF pulse will initiate transfer into Full Power state.
- While in ATP™ mode, an ON_OFF pulse will initiate transfer into Full Power state.
- While in PTF™ mode, an ON_OFF pulse will initiate one PTF™ request.
- While in Full Power state, an ON_OFF pulse will initiate orderly shutdown into Hibernate state.

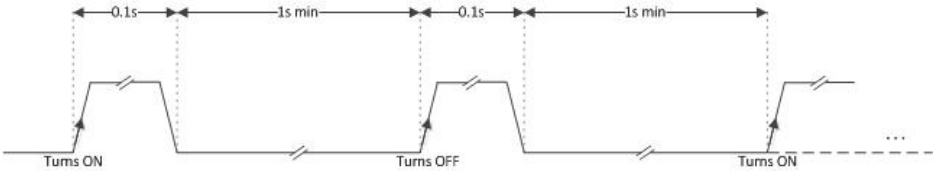


FIGURE 9 – ON_OFF TIMING

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100µs.
ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100µs.
Recommended ON_OFF Low-High-Low pulse length is 100ms.
ON_OFF pulses with less than 1s intervals are not recommended.
Multiple switch bounce pulses are recommended to be filtered out.
Pull-down resistor of 10kΩ-33kΩ is recommended to avoid accidental power mode change.
ON_OFF input is tolerable up to 3.6V.
Do not drive high permanently or pull-up this input.
This line must be connected to host.

17.4.2. WAKEUP

WAKEUP output from ORG4572 is used to indicate power state.
A low logic level indicates that the module is in one of its low-power states - Hibernate or Standby. A high logic level indicates that the module is in Full Power state.
In addition WAKEUP output can be used to control auxiliary devices.
Wakeup output is LVCMOS 1.8V compatible.
Do not connect if not in use.

17.4.3. $\overline{\text{RESET}}$

Power-on-Reset (POR) sequence is generated internally.
In addition, external reset is available through $\overline{\text{RESET}}$ pad.
Resetting ORG4572 clears the state machine of self-managed power saving modes to default.
$\overline{\text{RESET}}$ signal should be applied for at least 1µs.
$\overline{\text{RESET}}$ input is active low and has internal pull-up resistor of 1MΩ.
Do not drive this input high.
Do not connect if not in use.

17.4.4. 1PPS

Pulse-Per-Second (PPS) output provides a pulse signal for timing purposes.
PPS output starts when 3D position solution has been obtained using 5 or more GNSS satellites.
PPS output stops when 3D position solution is lost.
Pulse length (high state) is 200ms with rising edge is less than 40ns synchronized to UTC epoch.
The correspondent UTC time message is generated and put into output FIFO 300ms after the PPS signal. The exact time between PPS and UTC time message delivery depends on message rate, message queue and communication baud rate.
1PPS output is LVCMOS 1.8V compatible.
Do not connect if not in use.

17.5. DATA INTERFACE

ORG4572 module has 3 types of interface ports to connect to host - UART, SPI or I^2C – all multiplexed on a shared set of pads. At system reset host port interface lines are disabled, so no conflict occurs. Logic values on $\overline{CTS}$ and $\overline{RTS}$ are read by the module during startup and define host port type. External resistor of 10kΩ is recommended. Pull-up resistor is referenced to 1.8V.

PORT TYPE	$\overline{CTS}$	$\overline{RTS}$
UART	External pull-up	Internal pull-up
SPI (default)	Internal pull-down	Internal pull-up
I^2C	Internal pull-down	External pull-down

TABLE 11 – HOST INTERFACE SELECT

17.5.1. UART

ORG4572 has a standard UART port:

- TX used for GNSS data reports. Output logic high voltage level is LVCMOS 1.8V compatible.
- RX used for receiver control. Input logic high voltage level is 1.45V tolerable up to 3.6V.

17.5.2. UART BAUD RATE AND PROTOCOL SELECTION

Logic values on GPIO1 and GPIO2 are read by the module during startup and define UART baud rate and protocol.
External resistors of 2.2kΩ are recommended. Pull-up resistors are referenced to 1.8V.

GPIO1	GPIO2	PROTOCOL	BAUD RATE
Pull-up	Pull-up	NMEA	4,800
Pull-up	Pull-down	NMEA	9,600
Pull-down	Pull-up	NMEA	38,400
Pull-down	Pull-down	OSP	115,200

TABLE 12 – UART BAUD RATE AND PROTOCOL SELECT

17.5.3. SPI

SPI host interface features are:

- Slave SPI Mode 1, supports clock up to 6.8MHz.
- RX and TX have independent 2-byte idle patterns of '0xA7 0xB4'.
- TX and RX each have independent 1024 byte FIFO buffers.
- TX FIFO is disabled when empty and transmits its idle pattern until re-enabled.
- RX FIFO detects a software specified number of idle pattern repeats and then disables FIFO input until the idle pattern is broken.
- FIFO buffers can generate an interrupt at any fill level.
- SPI detects synchronization errors and can be reset by software.

Output is LVCMOS 1.8V compatible. Inputs are tolerable up to 3.6V.

17.5.4. I^2C

I^2C host interface features are:

- I^2C Multi-Master Mode - ORG4572 initiates clock and data, operating speed 400kbps.
- I^2C address '0x60' for RX and '0x62' for TX.
- Individual transmit and receive FIFO length of 64 bytes.

SCL and SDA are pseudo open-drain lines, therefore require external pull-up resistors of 2.2kΩ to 1.8V, or 3.3kΩ to 3.3V.

17.6. SMART SENSORS INTERFACE

MEMS sensors connected to an auxiliary I²C bus provide support for contextual awareness.
I²C bus comprises of 2 pads – GPIO1 and GPIO2, both are pseudo open-drain therefore requiring external pull-up resistors.

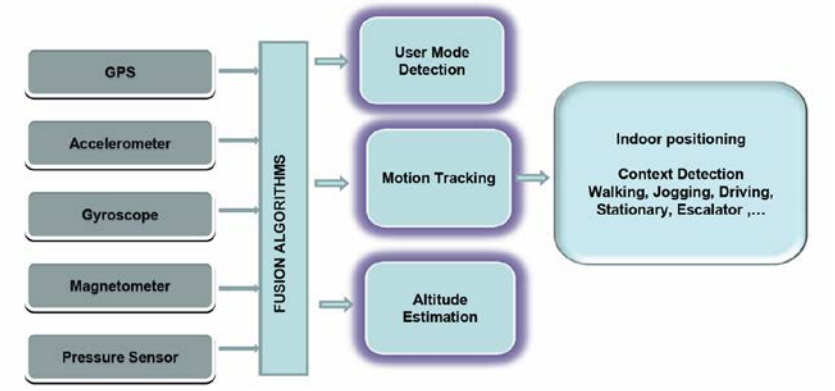


FIGURE 10 – SMART SENSORS INTERFACE

ORG4572 acts as I²C Master and sensor devices function in Slave mode at speed of 400kbps.
This provides a very low latency data pipe for the critical sensor data so that it can be used in the Navigation Library and Kalman filter to enhance navigation performance.
MEMS algorithms perform a sensor data fusion with GNSS signal measurements.
GNSS measurements can be used to calibrate MEMS sensors during periods of satellite navigation.
MEMS sensors can augment GNSS measurements, making those more accurate under degraded satellite signal conditions and challenging dynamics.
MEMS data can be output to other subsystems in the platform over host serial interface.

17.7. FLASH MEMORY INTERFACE

Flash memory connected to an auxiliary SPI bus provides storage support for smart data logger, system aiding data and firmware patch updates.
SPI bus comprises of 4 pads – GPIO1, GPIO2, GPIO3 and GPIO4.
ORG4572 acts as SPI Master while SPI flash memory functions in Slave mode.
ORG4572 supports 4Mbit and 8Mbit SPI flash memory ICs from specified manufacturers.

17.7.1. DATA LOGGER SUPPORT

ORG4572 can log data waypoints to SPI flash memory autonomously or under host control.
Features of data logger include:

- Ability to log based on time interval and/or when distance or speed thresholds are exceeded.
- Control over logging continuously or until available memory is full.
- Control over which data are logged, including time, position, altitude, speed and accuracy.
- Access to status information on how much memory remains.
- Commands to clear memory and download data.

17.7.2. AIDING DATA STORAGE SUPPORT

ORG4572 can store CGEE™ and SGEE™ aiding data to SPI flash memory:

- 4Mbit memory can support up to 7 days of SGEE™ for GPS and GLONASS satellites.
- 8Mbit memory can support up to 31 days of SGEE™ for GPS and 14 days for GLONASS.

17.7.3. PATCH UPDATE SUPPORT

Patch updates may be provided from time to time to address ROM firmware issues as a method of performance improvement.
Host controller is managing load and application of patch updates.
Patch files may be up to 128KB in size.

18. TYPICAL APPLICATION CIRCUIT

18.1. PASSIVE ANTENNA

Designing with passive antenna require RF layout skills and can be challenging.

Contact OriginGPS for application specific recommendations and design review services.

18.2. PASSIVE ANTENNA WITH EXTERNAL LNA

```
     |R1 = 10K                        | NMEA @ 4800bps. = R3,R4
UART |R2,R7,R8 = Do Not Assemble      | NMEA @ 9600bps. = R3,R6
_____|________________________________| OSP @ 115200bps. = R5,R6
SPI  |R1,R2,R7,R8 = Do Not Assemble
_____|__________________________________
I2C  |R2 = 10K
     |R1 = Do Not Assemble
     |R7,R8 = 2.2K
```

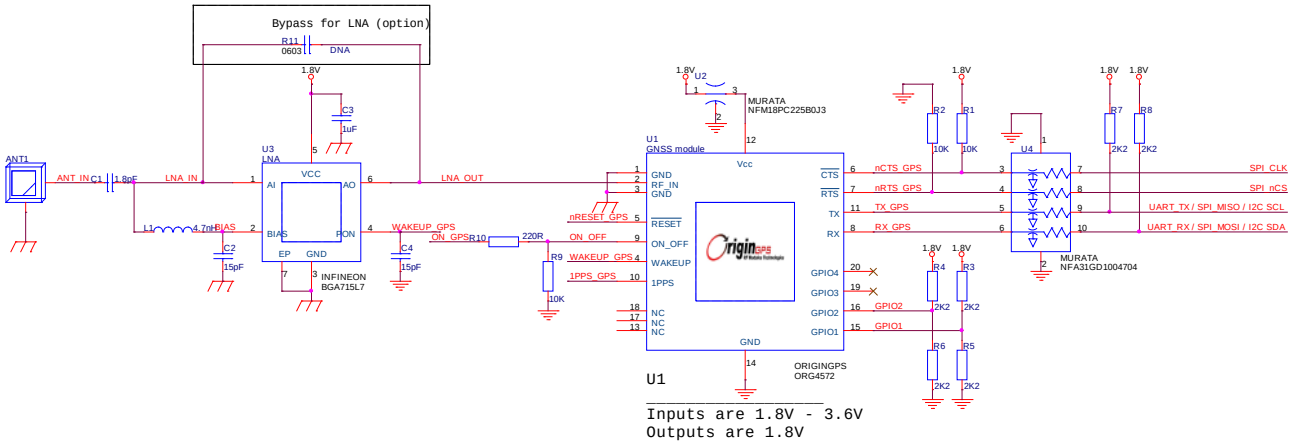


FIGURE 11 – PASSIVE ANTENNA WITH EXTERNAL LNA SCHEMATICS

18.3. ACTIVE ANTENNA

```
     |R1 = 10K                        | NMEA @ 4800bps. = R3,R4
UART |R2,R7,R8 = Do Not Assemble      | NMEA @ 9600bps. = R3,R6
_____|________________________________| OSP @ 115200bps. = R5,R6
SPI  |R1,R2,R7,R8 = Do Not Assemble
_____|__________________________________
I2C  |R2 = 10K
     |R1 = Do Not Assemble
     |R7,R8 = 2.2K
```

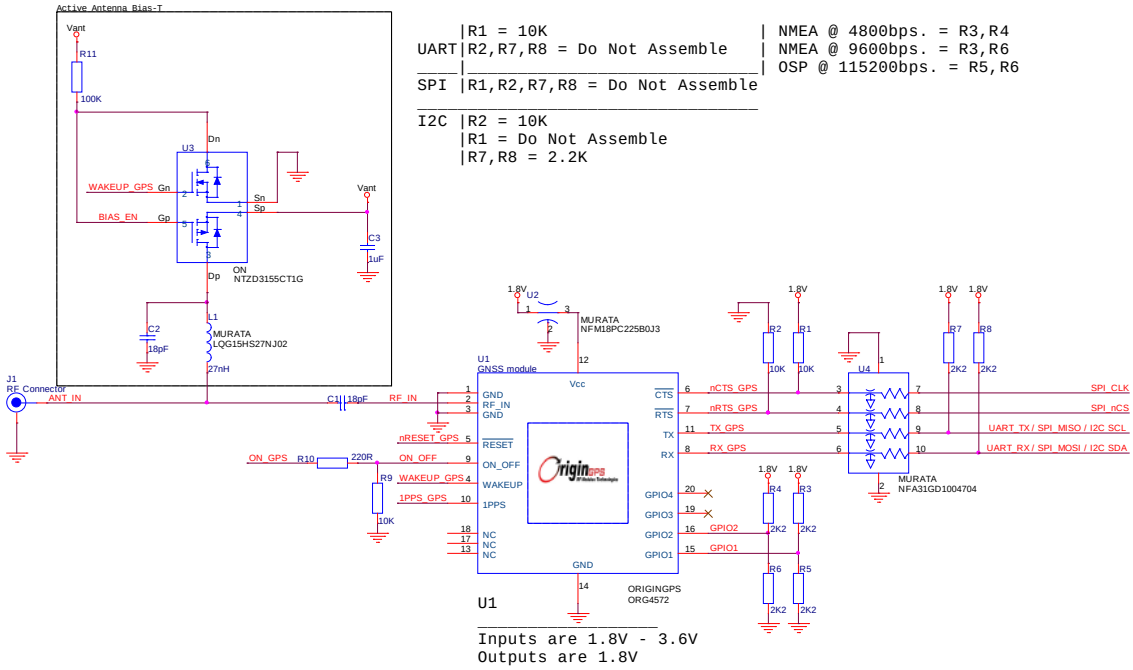


FIGURE 12 – EXTERNAL LNA SCHEMATICS

18.4. ANTENNA SWITCH

Contact OriginGPS for Application Note covering dual-antenna (on-board and external) design combining RF switch with auto-sense, DC bias and short-circuit protection.

19. RECOMMENDED PCB LAYOUT

19.1. FOOTPRINT

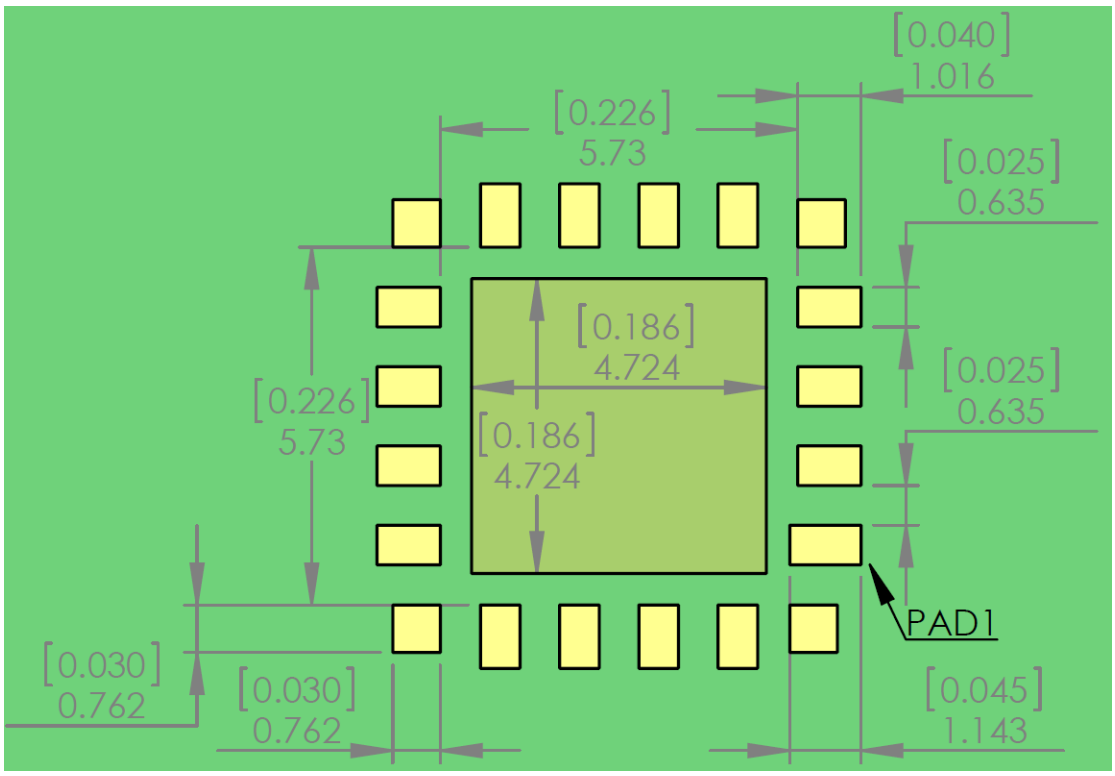


FIGURE 13 – FOOTPRINT

Ground paddle at the middle should be connected to main Ground plane by multiple vias.
Ground paddle at the middle must be solder masked.
Silk print of module's outline is highly recommended for SMT visual inspection.

TOP VIEW

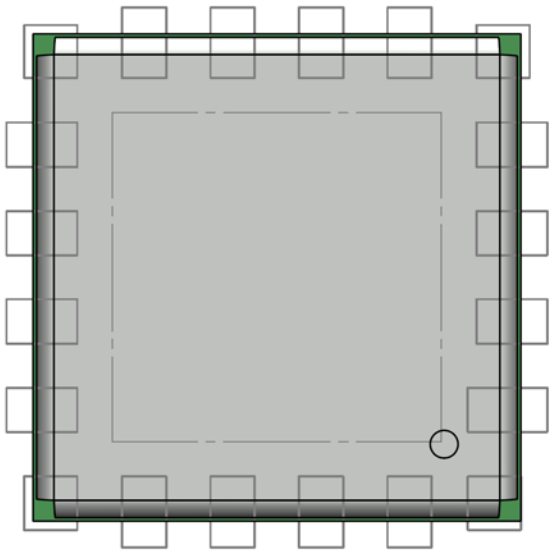


FIGURE 14 – MODULE HOSTED ON FOOTPRINT

19.2. HOST PCB

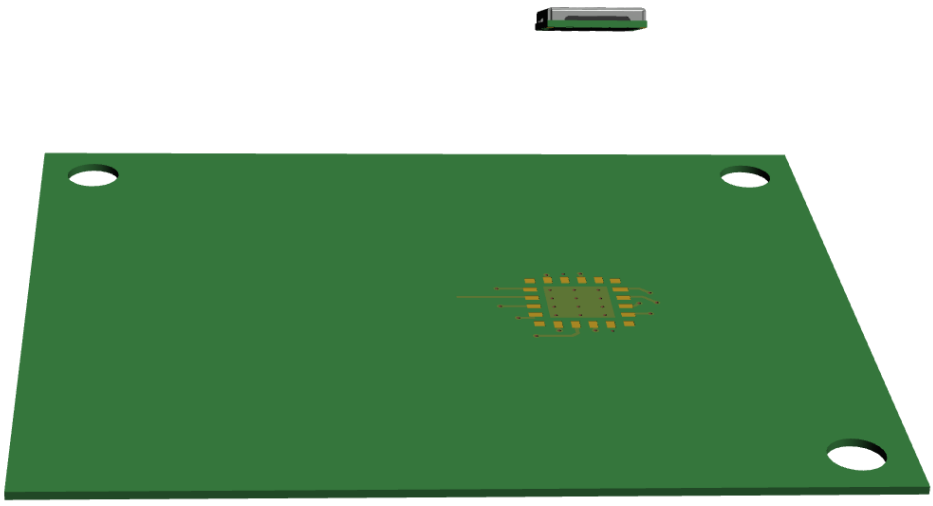


FIGURE 15 – HOST PCB

19.3. RF TRACE

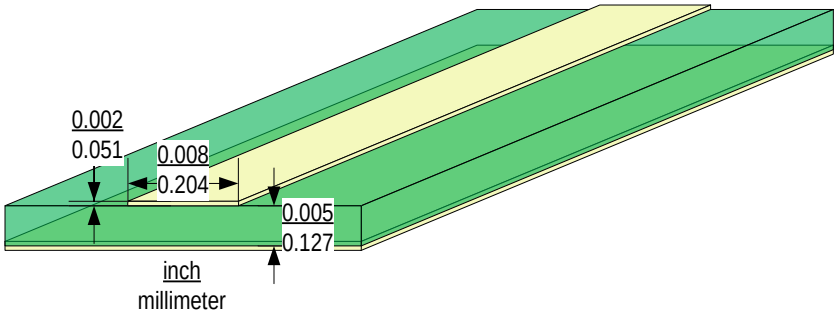


FIGURE 16 – TYPICAL MICROSTRIP PCB TRACE ON FR-4 SUBSTRATE

19.4. PCB STACK-UP

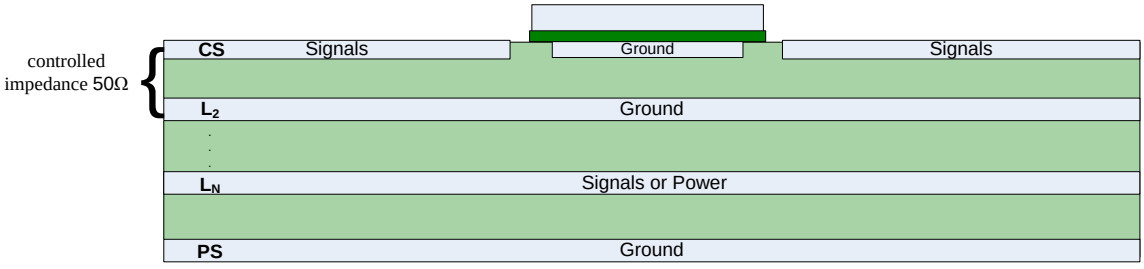


FIGURE 17 – TYPICAL PCB STACK-UP

19.5. PCB LAYOUT RESTRICTIONS

Switching and high-speed components, traces and vias must be kept away from ORG4572 module.

Signal traces to/from module should have minimum length.

Recommended minimal distance from adjacent active components is 3mm.

Ground pads must be connected to host PCB Ground with shortest possible traces or vias.

In case of tight integration constrain or co-location with adjacent high speed components like CPU or memory, high frequency components like transmitters, clock resonators or oscillators, LCD panels or CMOS image sensors, contact OriginGPS for application specific recommendations.

20. DESIGN CONSIDERATIONS

ORG4572 operate with received signal levels down to -165dBm and can be affected by high absolute levels of RF signals, moderate levels of RF interference near the GNSS bands and by low-levels of RF noise in the GNSS band.

RF interference from nearby electronic circuits or radio transmitters can contain enough energy to desensitize ORG4572. These systems may also produce levels of energy outside of GNSS band, high enough to leak through RF filters and degrade the operation of the radios in ORG4572.

This issue becomes more critical in small products, where there are industrial design constraints.

In that environment, transmitters for Wi-Fi, Bluetooth, RFID, cellular and other radios may have antennas physically close to the GNSS receiver antenna.

To prevent degraded performance of ORG4572, OriginGPS recommends performing EMI/jamming susceptibility tests for radiated and conducted noise on prototypes and assessing risks of other factors.

Antennas for GPS and GLONASS have a wider bandwidth than pure GPS antennas.

Some wideband antennas may not have a good axial ratio to block reflections of RHCP GPS and GLONASS signals. These antennas have lower rejection of multipath reflections and tend to degrade the overall performance of the receiver.

Designing with passive antenna require RF layout skills and can be challenging.

Contact OriginGPS for application specific recommendations and design review services.

21. OPERATION

When power is first applied, ORG4572 goes into a Hibernate state while integrated RTC starts and internal Finite State Machine (FSM) sequences though to “Ready-to-Start” state.
Host is not required to control external master nRESET since module’s internal reset circuitry handles detection of power application.
While in “Ready-to-Start” state, ORG4572 awaits a pulse to the ON_OFF input.
Since integrated RTC startup times are variable, host is required either to wait for a fixed interval or to monitor a short Low-High-Low pulse on WAKEUP output that indicates FSM “Ready-to-Start” state.
Another option is to repeat a pulse on the ON_OFF input every second until the module starts by either detecting a stable logic high level on WAKEUP output or neither generation of UART messages.

21.1. STARTING THE MODULE

A pulse on the ON_OFF input line when FSM is ready and in startup-ready state, Hibernate state, standby state, will command the module to start.

- While in Hibernate state, an ON_OFF pulse will initiate transfer into Full Power state.
- While in ATP™ mode, an ON_OFF pulse will initiate transfer into Full Power state.
- While in PTF™ mode, an ON_OFF pulse will initiate one PTF™ request.
- While in Full Power state, an ON_OFF pulse will initiate orderly shutdown into Hibernate state.

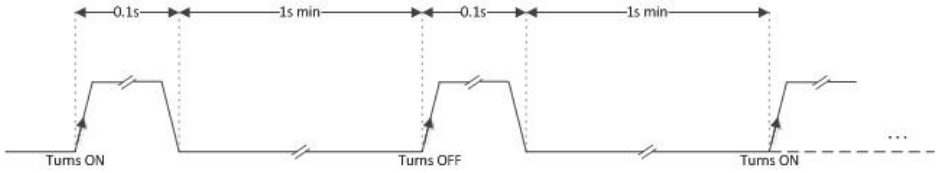


FIGURE 18 – ON_OFF TIMING

ON_OFF detector set requires a rising edge and high logic level that persists for at least 100µs.
ON_OFF detector reset requires ON_OFF asserted to low logic level for at least 100µs.
Recommended ON_OFF Low-High-Low pulse length is 100ms.
ON_OFF pulses with less than 1s intervals are not recommended.

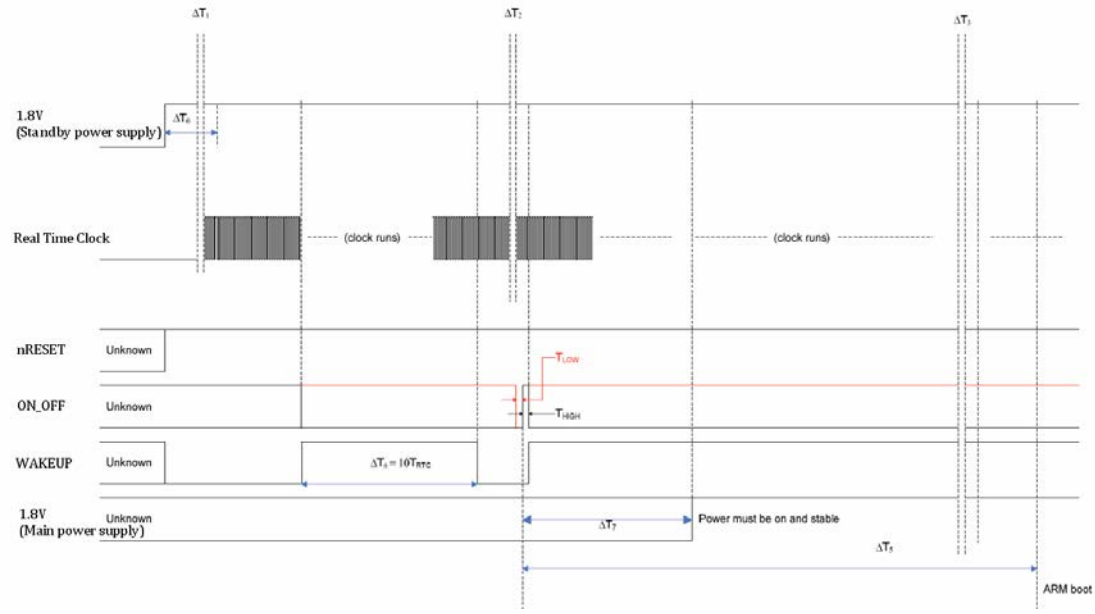


FIGURE 19 – START-UP TIMING

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
f_{RTC}	RTC frequency	25°C	-20 ppm	32768	+20 ppm	Hz
t_{RTC}	RTC tick	25°C		30.5176		µs
ΔT1	RTC startup time			300		ms
ΔT0	Power stabilization		$6 \cdot t_{RTC}+\Delta T1$	$7 \cdot t_{RTC}+\Delta T1$	$8 \cdot t_{RTC}+\Delta T1$	µs
ΔT6	WAKEUP pulse	RTC running		10		t_{RTC}
ΔT_{LOW}	ON_OFF low		3			t_{RTC}
ΔT_{HIGH}	ON_OFF high		3			t_{RTC}
ΔT3	Startup sequencing	After ON_OFF		1024		t_{RTC}
-	ON_OFF to WAKEUP high	After ON_OFF		6		t_{RTC}
ΔT5	ON_OFF to ARM start	After ON_OFF		2130		t_{RTC}
ΔT7	Main power source start[1]	WAKEUP high	0	30	300	t_{RTC}

TABLE 13 – START-UP TIMING

21.2. VERIFYING THE MODULE HAS STARTED

WAKEUP output will go high indicating ORG4572 has started.
System activity indication depends upon selected serial interface.
The first message to come out of module is “OK_TO_SEND” - ‘$PSRF150,1*3E’.

21.2.1. UART

When active, the module will output NMEA messages at the 4800bps.

21.2.2. I²C

In Multi-Master mode with no bus contention - the module will spontaneously send messages.
In Multi-Master mode with bus contention - the module will send messages after the I^2C bus contention resolution process allows it to send.

21.2.3. SPI

Since ORG4572 is SPI slave device, there is no possible indication of system “ready” through SPI interface. Host must initiate SPI connection approximately 1s after WAKEUP output goes high.

21.3. SHUTTING DOWN THE MODULE

Transferring ORG4572 from Full Power state to Hibernate state can be initiated in two ways:

- By a pulse on ON_OFF input.
- By NMEA ($PSRF117) or OSP (MID205) serial message.

Orderly shutdown process may take anywhere from 10ms to 900ms to complete, depending upon operation in progress and messages pending, and hence is dependent upon serial interface speed and controls. ORG4572 will stay in Full Power state until TX FIFO buffer is emptied.
The last message during shutdown sequence is ‘$PSRF150,0*3F’.

Notes:

1. If power provided through dual supply, assign 1.8V LDO with low quiescent current for Hibernate state and 1.8V DC-DC with high efficiency for Full Power state.

22. FIRMWARE

Power On State		Hibernate
Default Interface[1]		SPI
SPI Data Format		NMEA
UART Settings		Baud Rate is set by GPIO1 and GPIO2
UART Data Format		Protocol is set by GPIO1 and GPIO2
I^2C Settings		Multi-Master 400kbps
I^2C Data Format		NMEA
Satellite Constellation		GPS + GLONASS
NMEA Messages		$GPGGA @1 sec.
		$GNGNS @ 1 sec.
		$GNGSA @ 1 sec.
		$GPGSV @ 5 sec.
		$GLGSV @ 5 sec.
		$GNRMC @ 1 sec.
Firmware Defaults	SBAS	OFF
	ABP™	OFF
	Static Navigation	ON
	Track Smoothing	OFF
	Jammer Detector	ON
	Jammer Remover	OFF
	Fast Time Sync	OFF
	Pseudo DR Mode	ON
	Power Saving Mode	OFF
	3SV Solution Mode	ON
	MEMS Gateway	OFF
	Data Logger	OFF
	5Hz Update Rate	OFF

TABLE 14 – DEFAULT FIRMWARE SETTINGS

Notes:

1. Without external resistor straps on $\overline{CTS}$ or $\overline{RTS}$.

23. HANDLING INFORMATION

23.1. MOISTURE SENSITIVITY

ORG4572 modules are MSL 3 designated devices according to IPC/JEDEC J-STD-033B standard.
Module in sample or bulk package should be baked prior to assembly at 125°C for 48 hours.

23.2. ASSEMBLY

The module supports automatic pick-and-place assembly and reflow soldering processes.
Reflow soldering of the module on the component side of the motherboard PCB according to standard IPC/JEDEC J-STD-020D for LGA SMD.
Suggested solder paste stencil is 5 mil to ensure sufficient solder volume.

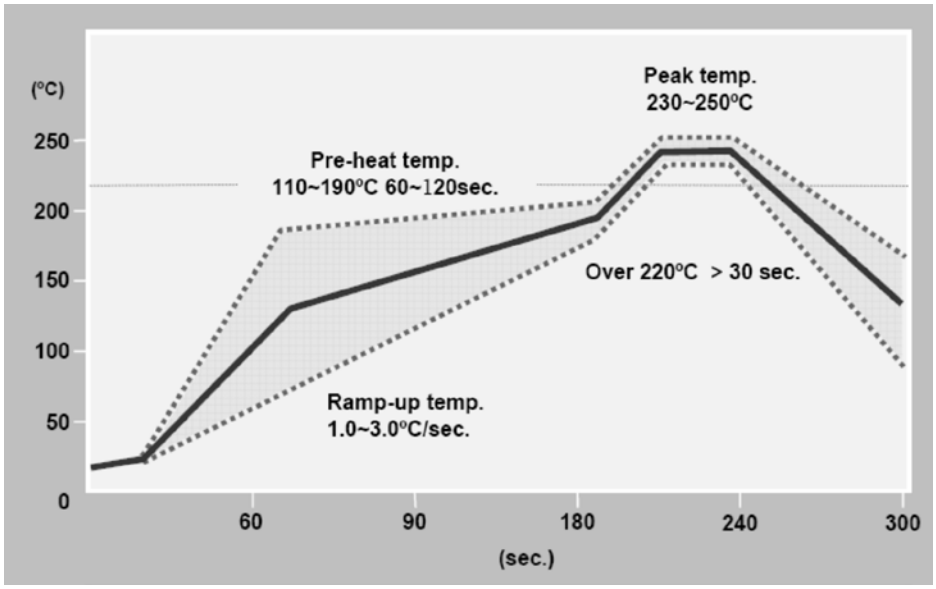


FIGURE 20 – RECOMMENDED SOLDERING PROFILE

Suggested peak reflow temperature is 250°C for 10 sec. for Pb-Free solder paste.
Absolute Maximum reflow temperature is 260°C for 10 sec.

23.3. REWORK

If localized heating is required to rework or repair the module, precautionary methods are required to avoid exposure to solder reflow temperatures that can result in permanent damage to the device.

23.4. ESD SENSITIVITY

This product is ESD sensitive device and must be handled with care.

23.5. SAFETY INFORMATION

Improper handling and use can cause permanent damage to the product.
Avoid cleaning process in ultrasonic degreaser, since ultrasonic vibrations may cause performance degradation or destruction of internal circuitry.

23.6. DISPOSAL INFORMATION

This product must not be treated as household waste.
For more detailed information about recycling electronic components contact your local waste management authority.

24. MECHANICAL SPECIFICATIONS

- ORG4572 module has miniature LGA SMD packaging sized 7mm x 7mm.
- ORG4572 built on a PCB assembly enclosed with metallic RF shield box.
- On bottom side there are 16+4 SMT pads with Cu base and ENIG plating.
- ORG4572 module supports automated pick and place assembly and reflow soldering processes.

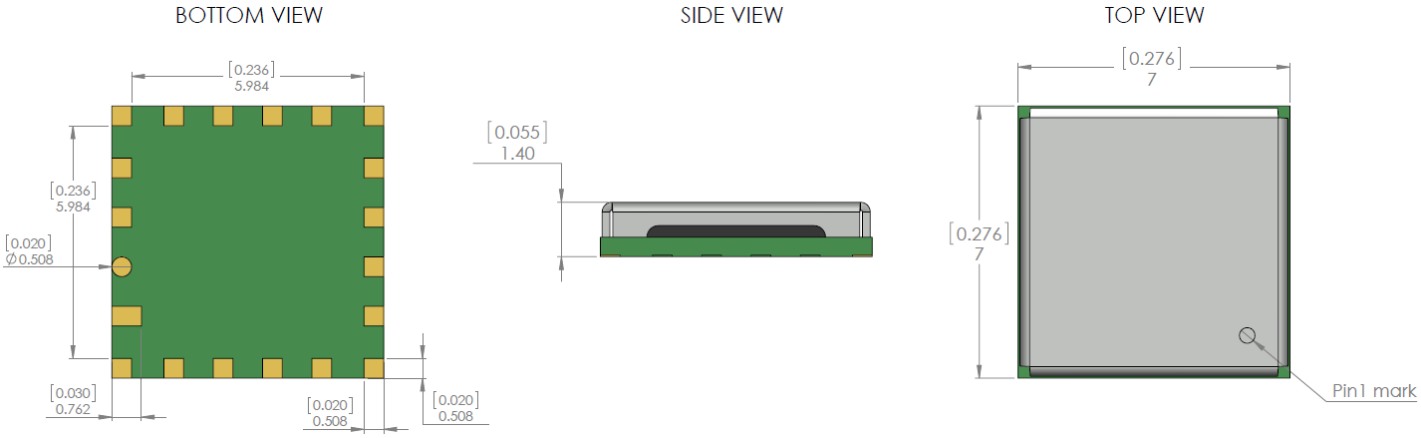


FIGURE 21 – MECHANICAL DRAWING

Dimensions	Length	Width	Height	Weight	
mm	7.00 +0.10/ -0.05	7.00 +0.10/ -0.05	1.4 +0.1/ -0.0	gr	0.2
inch	0.276 +0.004/ -0.002	0.276 +0.004/ -0.001	0.055 +0.004/ -0.0	oz	0.01

TABLE 15 – MECHANICAL SUMMARY

25. COMPLIANCE

The following standards are applied on the production of ORG4572 modules:

- IPC-6011/6012 Class2 for PCB manufacturing
- IPC-A-600 Class2 for PCB inspection
- IPC-A-610D Class2 for SMT acceptability

ORG4572 modules are manufactured in ISO 9001:2008 accredited facilities.

ORG4572 modules are manufactured in ISO 14001:2004 accredited facilities.

ORG4572 modules are manufactured in OHSAS 18001:2007 accredited facilities.

ORG4572 modules are designed, manufactured and handled in compliance with the Directive 2011/65/EU of the European Parliament and of the Council of June 2011 on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment, referred as RoHS II.

ORG4572 modules are manufactured and handled in compliance with the applicable substance bans as of Annex XVII of Regulation 1907/2006/EC on Registration, Evaluation, Authorization and Restriction of Chemicals including all amendments and candidate list issued by ECHA, referred as REACH.

ORG4572 modules comply with the following EMC standards:

- EU CE EN55022:06+A1(07), Class B
- US FCC 47CFR Part 15:09, Subpart B, Class B
- JAPAN VCCI V-3/2006.04

26. PACKAGING AND DELIVERY

26.1. APPEARANCE

ORG4572 modules are delivered in reeled tapes for automatic pick and place assembly process.

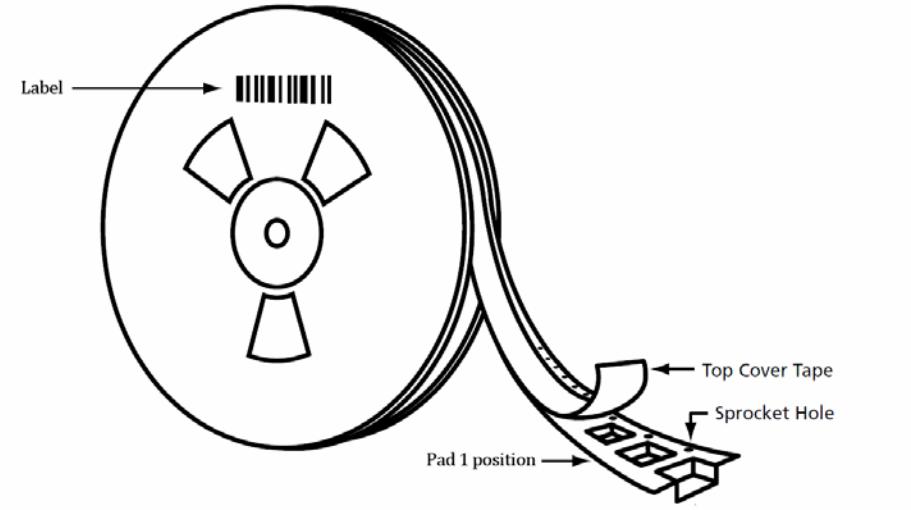


FIGURE 22 – MODULE POSITION

ORG4572 modules are packed in 2 different reel types.

SUFFIX	TR1	TR2
Quantity	500	2000

TABLE 16 – REEL QUANTITY

Reels are dry packed with humidity indicator card and desiccant bag according to IPC/JEDEC J-STD-033B standard for MSL 3 devices.

Reels are vacuum sealed inside anti-static moisture barrier bags.

Sealed reels are labeled with MSD sticker providing information about:

- MSL
- Shelf life
- Reflow soldering peak temperature
- Seal date

Sealed reels are packed inside cartons.

Reels, reel packs and cartons are labeled with sticker providing information about:

- Description
- Part number
- Lot number
- Customer PO number
- Quantity
- Date code

26.2. CARRIER TAPE

Carrier tape material - polystyrene with carbon (PS+C).

Cover tape material – polyester based film with heat activated adhesive coating layer.

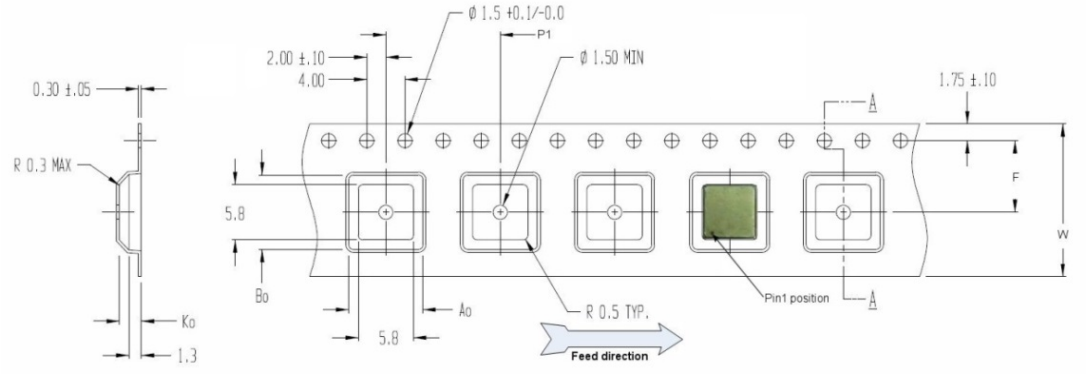


FIGURE 23 – CARRIER TAPE

	mm	inch
A_0	8.3 ± 0.1	0.327 ± 0.004
B_0	8.3 ± 0.1	0.327 ± 0.004
K_0	2.7 ± 0.1	0.106 ± 0.004
F	7.5 ± 0.1	0.295 ± 0.004
P1	12.0 ± 0.1	0.472 ± 0.004
W	16.0 ± 0.3	0.630 ± 0.012

TABLE 17 – CARRIER TAPE DIMENSIONS

26.3. REEL

Reel material - antistatic plastic.

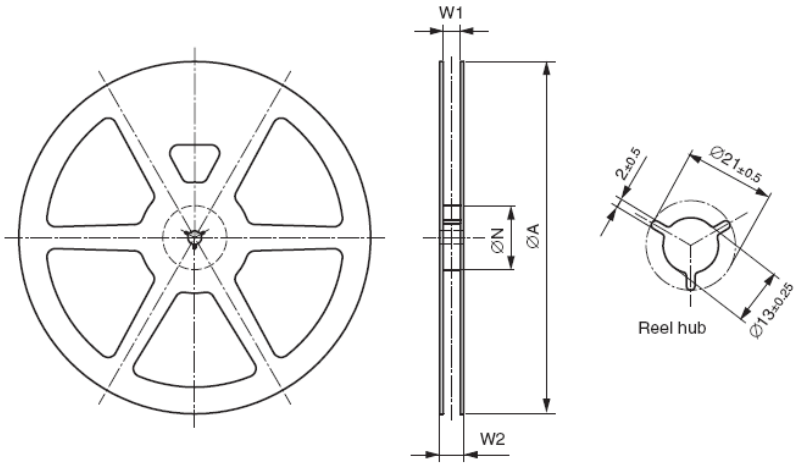


FIGURE 24 – REEL

SUFFIX	TR1		TR2	
	mm	inch	mm	inch
ØA	178.0 ± 1.0	7.00 ± 0.04	330.0 ± 2.0	13.00 ± 0.08
ØN	60.0 ± 1.0	2.36 ± 0.04	102.0 ± 2.0	4.02 ± 0.08
W1	16.7 ± 0.5	0.66 ± 0.02	16.7 ± 0.5	0.66 ± 0.02
W2	19.8 ± 0.5	0.78 ± 0.02	22.2 ± 0.5	0.87 ± 0.02

TABLE 18 – REEL DIMENSIONS

27. ORDERING INFORMATION

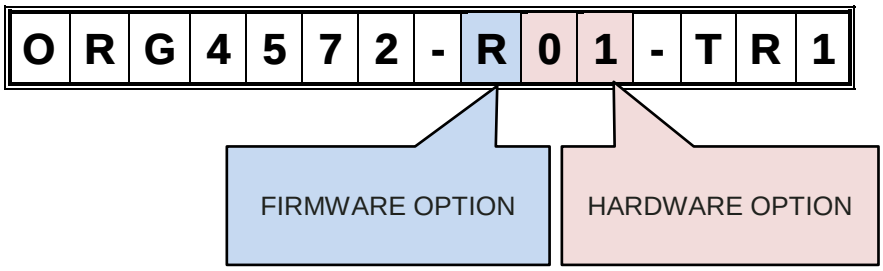


TABLE 19 – ORDERING OPTIONS

PART NUMBER	FIRMWARE VERSION	HARDWARE VARIANT	PACKAGING	SPQ
ORG4572-R01-TR1	1	01	REELED TAPE	500
ORG4572-R01-TR2	1	01	REELED TAPE	2000
ORG4572-R01-UAR	1	01	EVALUATION KIT	1

TABLE 20 – ORDERABLE DEVICES