

Product Description

Peregrine's PE97022 is a high-performance integer-N PLL capable of frequency synthesis up to 3.5 GHz. The device is designed for superior phase noise performance while providing an order of magnitude reduction in current consumption, when compared with existing commercial space PLLs.

The PE97022 features a $\div 10/11$ dual modulus prescaler, counters and a phase comparator as shown in *Figure 1*. Counter values are programmable through either a serial or parallel interface and can also be directly hardwired.

The PE97022 is optimized for commercial space applications. Single Event Latch-up (SEL) is physically impossible and Single Event Upset (SEU) is better than 10^{-9} errors per bit / day.

The PE97042 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering excellent RF performance and intrinsic radiation tolerance.

Features

- Low power - 45 mA at 3.3V
- $\div 10/11$ dual modulus prescaler
- Internal phase detector
- Serial, parallel, or direct hardwired mode
- Phase noise figure of merit: -216 dBc/Hz
- SEU $< 10^{-9}$ errors / bit-day
- 100 Krad (Si) total dose
- Pin compatible with the PE9702, packaged in a 44-lead CQFJ
(reference application note AN22 at www.psemi.com)

Figure 1. Block Diagram

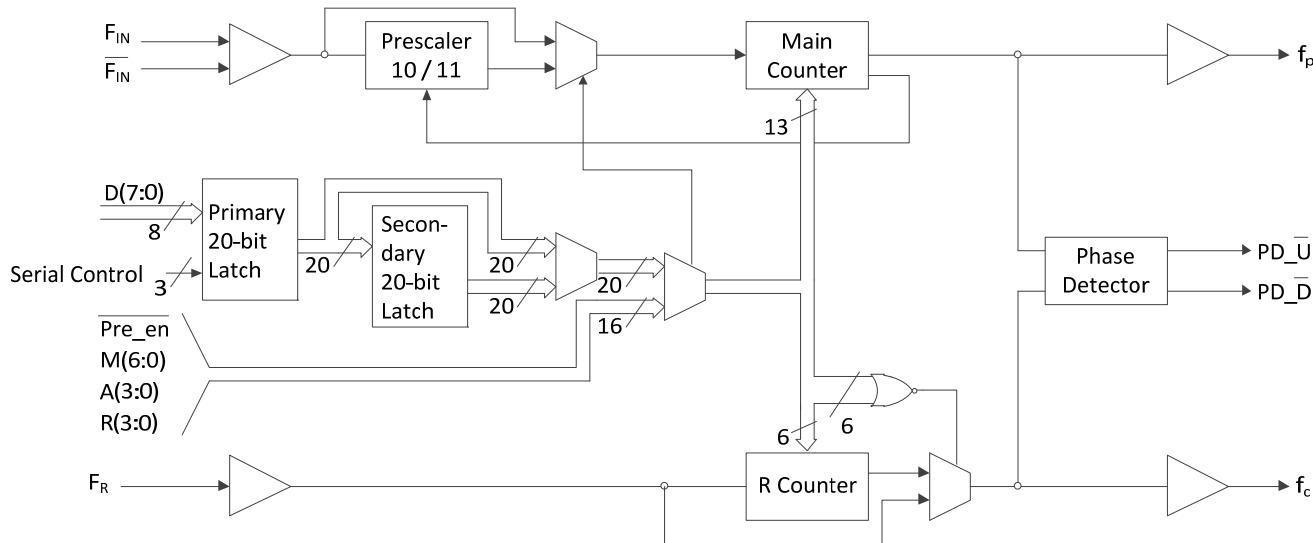
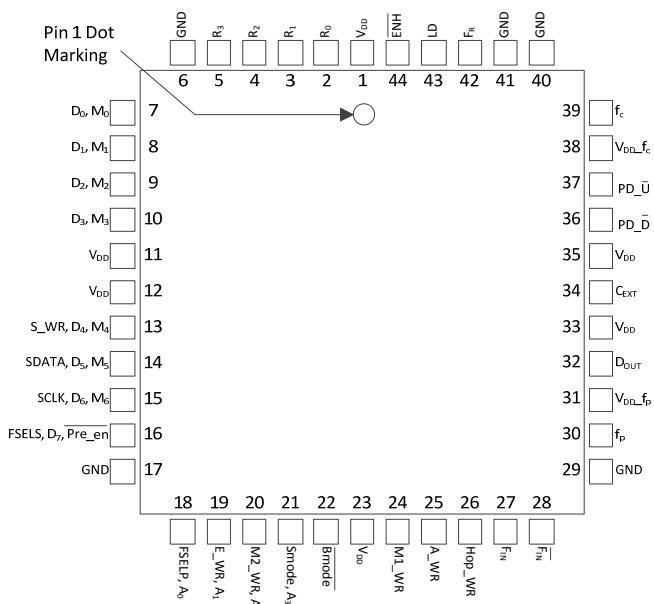
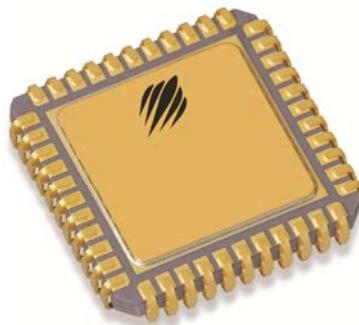


Figure 2. Pin Configurations (Top View)

Figure 3. Package Type
44-lead CQFJ

Table 1. Pin Descriptions

Pin #	Pin Name	Interface Mode	Type	Description
1	V _{DD}	ALL	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended
2	R ₀	Direct	Input	R counter bit0 (LSB)
3	R ₁	Direct	Input	R counter bit1
4	R ₂	Direct	Input	R counter bit2
5	R ₃	Direct	Input	R counter bit3
6	GND	ALL		Ground
7	D ₀	Parallel	Input	Parallel data bus bit0 (LSB)
	M ₀	Direct	Input	M counter bit0 (LSB)
8	D ₁	Parallel	Input	Parallel data bus bit1
	M ₁	Direct	Input	M counter bit1
9	D ₂	Parallel	Input	Parallel data bus bit2
	M ₂	Direct	Input	M counter bit2
10	D ₃	Parallel	Input	Parallel data bus bit3
	M ₃	Direct	Input	M counter bit3
11	V _{DD}	ALL	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended
12	V _{DD}	ALL	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended
13	S _{WR}	Serial	Input	Serial load enable input. While S _{WR} is "low", SDATA can be serially clocked. Primary register data is transferred to the secondary register on S _{WR} or Hop _{WR} rising edge
	D ₄	Parallel	Input	Parallel data bus bit4
	M ₄	Direct	Input	M counter bit4

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Interface Mode	Type	Description
14	SDATA	Serial	Input	Binary serial data input. Input data entered MSB first
	D ₅	Parallel	Input	Parallel data bus bit5
	M ₅	Direct	Input	M counter bit5
15	SCLK	Serial	Input	Serial clock input. SDATA is clocked serially into the 20-bit primary register (E_WR "low") or the 8-bit enhancement register (E_WR "high") on the rising edge of SCLK
	D ₆	Parallel	Input	Parallel data bus bit6
	M ₆	Direct	Input	M counter bit6
16	FSELS	Serial	Input	Selects contents of primary register (FSELS = 1) or secondary register (FSELS = 0) for programming of internal counters while in Serial Interface Mode
	D ₇	Parallel	Input	Parallel data bus bit7 (MSB)
	Pre_en	Direct	Input	Prescaler enable, active "low". When "high", F _{IN} bypasses the prescaler
17	GND	ALL		Ground
18	FSELP	Parallel	Input	Selects contents of primary register (FSELP=1) or secondary register (FSELP = 0) for programming of internal counters while in Parallel Interface Mode
	A ₀	Direct	Input	A counter bit0 (LSB)
19	E_WR	Serial	Input	Enhancement register write enable. While E_WR is "high", SDATA can be serially clocked into the enhancement register on the rising edge of SCLK
		Parallel	Input	Enhancement register write. D[7:0] are latched into the enhancement register on the rising edge of E_WR
	A ₁	Direct	Input	A counter bit1
20	M2_WR	Parallel	Input	M2 write. D[3:0] are latched into the primary register (R[5:4], M[8:7]) on the rising edge of M2_WR
	A ₂	Direct	Input	A counter bit2
21	Smode	Serial, Parallel	Input	Selects serial bus interface mode (Bmode = 0, Smode = 1) or Parallel Interface Mode (Bmode = 0, Smode = 0)
	A ₃	Direct	Input	A counter bit3 (MSB)
22	Bmode	ALL	Input	Selects direct interface mode (Bmode = 1)
23	V _{DD}	ALL	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended
24	M1_WR	Parallel	Input	M1 write. D[7:0] are latched into the primary register (Pre_en, M[6:0]) on the rising edge of M1_WR
25	A_WR	Parallel	Input	A write. D[7:0] are latched into the primary register (R[3:0], A[3:0]) on the rising edge of A_WR
26	Hop_WR	Serial, Parallel	Input	Hop write. The contents of the primary register are latched into the secondary register on the rising edge of Hop_WR
27	F _{IN}	ALL	Input	Prescaler input from the VCO, 3.5 GHz max frequency. A 22 pF coupling capacitor should be placed as close as possible to this pin and terminated with a 50Ω resistor to ground
28	\overline{F}_{IN}	ALL	Input	Prescaler complementary input. A 22 pF bypass capacitor should be placed as close as possible to this pin and be connected in series with a 50Ω resistor to ground
29	GND	ALL		Ground
30	f _p	ALL	Output	Monitor pin for main divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding V _{DD} pin 31

Table 1. Pin Descriptions (cont.)

Pin #	Pin Name	Interface Mode	Type	Description
31	V_{DD-f_p}	ALL	Note 1	V_{DD} for f_p . Can be left floating or connected to GND to disable the f_p output
32	D_{OUT}	Serial, Parallel	Output	Data Out. The MSEL signal and the raw prescaler output are available on D_{OUT} through enhancement register programming
33	V_{DD}	ALL	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended
34	C_{EXT}	ALL	Output	Logical “NAND” of $PD_{\bar{U}}$ and $PD_{\bar{D}}$ terminated through an on chip, 2 k Ω series resistor. Connecting C_{EXT} to an external capacitor will low pass filter the input to the inverting amplifier used for driving LD
35	V_{DD}	ALL	Note 1	Power supply input. Input may range from 2.85V to 3.45V. Bypassing recommended
36	$PD_{\bar{U}}$	ALL	Output	$PD_{\bar{D}}$ is pulse down when f_p leads f_c
37	$PD_{\bar{U}}$	ALL		$PD_{\bar{U}}$ is pulse down when f_c leads f_p
38	V_{DD-f_c}	ALL	Note 1	V_{DD} for f_c . Can be left floating or connected to GND to disable the f_c output
39	f_c	ALL	Output	Monitor pin for reference divider output. Switching activity can be disabled through enhancement register programming or by floating or grounding V_{DD} pin 38
40	GND	ALL		Ground
41	GND	ALL		Ground
42	F_R	ALL	Input	Reference frequency input
43	LD	ALL	Output	Lock detect and open drain logical inversion of C_{EXT} . When the loop is in lock, LD is high impedance, otherwise LD is a logic low (“0”)
44	\bar{ENH}	Serial, Parallel	Input	Enhancement mode. When asserted low (“0”), enhancement register bits are functional

Notes: 1. V_{DD} pins 1, 11, 12, 23, 31, 33, 35, and 38 are connected by diodes and must be supplied with the same positive voltage level. V_{DD} pins 31 and 38 are used to enable test modes and should be left floating
 2. All digital input pins have 70 k Ω pull-down resistors to ground

Table 2. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	$V_{DD} + 0.3$	V
I_I	DC into any input	-10	+10	mA
I_O	DC into any output	-10	+10	mA
T_{stg}	Storage temperature range	-65	150	°C
V_{ESD}	ESD voltage HBM ¹		1000	V

Note 1: Human Body Model (MIL-STD 883 Method 3015 C2)

Table 3. Operating Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Supply voltage	2.85	3.45	V
T_A	Operating ambient temperature range	-40	85	°C

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ratings table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Table 4. DC Characteristics @ $V_{DD} = 3.3V$, $-40^\circ C < T_A < 85^\circ C$, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	Operational supply current;	$V_{DD} = 2.85\text{--}3.45V$ Prescaler disabled Prescaler enabled		15 45	20 50	mA
Digital inputs: all except F_R , F_{IN} , $\overline{F_{IN}}$						
V_{IH}	High level input voltage	$V_{DD} = 2.85\text{--}3.45V$	$0.7 \times V_{DD}$			V
V_{IL}	Low level input voltage	$V_{DD} = 2.85\text{--}3.45V$			$0.3 \times V_{DD}$	V
I_{IH}	High level input current	$V_{IH} = V_{DD} = 3.45V$			70	μA
I_{IL}	Low level input current	$V_{IL} = 0$, $V_{DD} = 3.45V$	-1			μA
Reference divider input: f_r						
I_{IHR}	High level input current	$V_{IH} = V_{DD} = 3.45V$			100	μA
I_{ILR}	Low level input current	$V_{IL} = 0$, $V_{DD} = 3.45V$	-100			μA
Counter and phase detector outputs: f_c , f_p .						
V_{OLD}	Output voltage LOW	$I_{out} = 6\text{ mA}$			0.4	V
V_{OHD}	Output voltage HIGH	$I_{out} = -3\text{ mA}$	$V_{DD} - 0.4$			V
Lock detect outputs: C_{EXT} , LD						
V_{OLC}	Output voltage LOW, C_{EXT}	$I_{out} = 100\text{ }\mu A$			0.4	V
V_{OHC}	Output voltage HIGH, C_{EXT}	$I_{out} = -100\text{ }\mu A$	$V_{DD} - 0.4$			V
V_{OLLD}	Output voltage LOW, LD	$I_{out} = 1\text{ mA}$			0.4	V

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating specified in Table 2.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

ELDRS

UltraCMOS® devices do not include bipolar minority carrier elements and therefore do not exhibit enhanced low dose rate sensitivity.

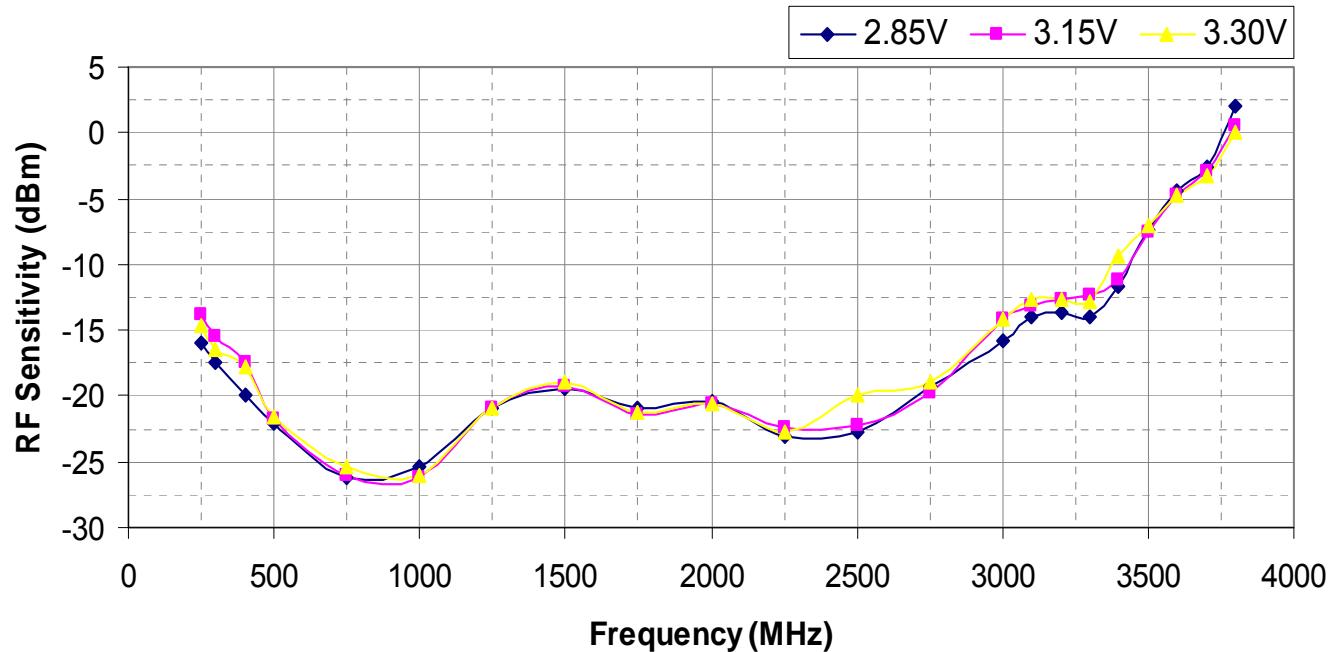
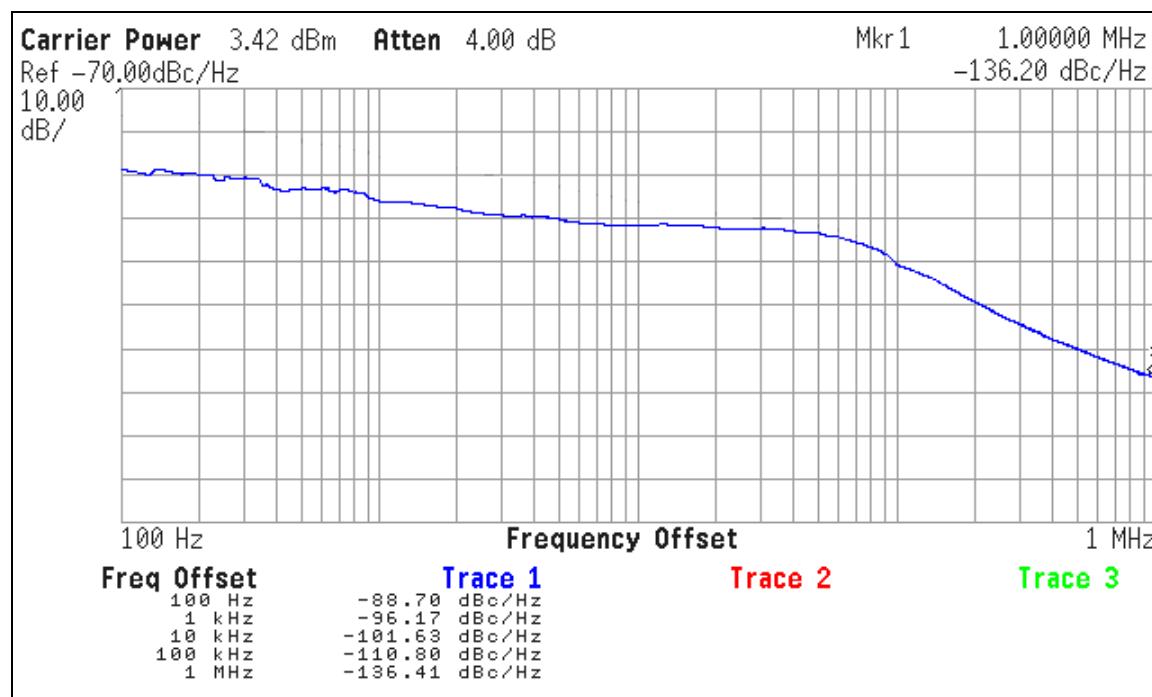
Table 5. AC Characteristics @ $V_{DD} = 3.3V$, $-40^{\circ}C < T_A < 85^{\circ}C$, unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Control interface and latches (see <i>Figures 1, 10, and 11</i>)						
f_{Clk}	Serial data clock frequency	Note 1			10	MHz
t_{ClkH}	Serial clock HIGH time		30			ns
t_{ClkL}	Serial clock LOW time		30			ns
t_{DSU}	SDATA set-up time after SCLK rising edge, D[7:0] set-up time to M1_WR, M2_WR, A_WR, E_WR rising edge		10			ns
t_{DHLD}	SDATA hold time after SCLK rising edge, D[7:0] hold time to M1_WR, M2_WR, A_WR, E_WR rising edge		10			ns
t_{PW}	S_WR, M1_WR, M2_WR, A_WR, E_WR pulse width		30			ns
t_{CWR}	SCLK rising edge to S_WR rising edge. S_WR, M1_WR, M2_WR, A_WR falling edge to Hop_WR rising edge		30			ns
t_{CE}	SCLK falling edge to E_WR transition		30			ns
t_{WRC}	S_WR falling edge to SCLK rising edge. Hop_WR falling edge to S_WR, M1_WR, M2_WR, A_WR rising edge		30			ns
t_{EC}	E_WR transition to SCLK rising edge		30			ns
t_{MDO}	MSEL data out delay after F_{IN} rising edge	$C_L = 12 \text{ pf}$			8	ns
Main divider (including prescaler) ⁴						
P_{Fin}	Input level range	External AC coupling 275 MHz \leq Freq \leq 3200 MHz	-5		5	dBm
		External AC coupling 3.2 GHz $<$ Freq \leq 3.5 GHz	0		5	dBm
Main divider (prescaler bypassed) ⁴						
F_{IN}	Operating frequency		50		300	MHz
P_{Fin}	Input level range	External AC coupling	-5		5	dBm
Reference divider						
F_R	Operating frequency	Note 3			100	MHz
P_{Fr}	Reference input power ²	Single-ended input	-2		10	dBm
Phase detector						
f_c	Comparison frequency	Note 3			50	MHz
SSB phase noise ($F_{IN} = 1.9 \text{ GHz}$, $F_R = 20 \text{ MHz}$, $f_c = 20 \text{ MHz}$, LBW = 50 kHz, $V_{DD} = 3.3V$, temp = 25°C) ⁴						
Φ_N	Phase noise	100 Hz offset		-89	-83	dBc/Hz
Φ_N	Phase noise	1 kHz offset		-95	-91	dBc/Hz
Φ_N	Phase noise	10 kHz offset		-102	-96	dBc/Hz
SSB phase noise ($F_{IN} = 1.9 \text{ GHz}$, $F_R = 20 \text{ MHz}$, $f_c = 20 \text{ MHz}$, LBW = 50 kHz, $V_{DD} = 3.0V$, temp = 25°C) ⁴						
Φ_N	Phase noise	100 Hz offset		-87	-70	dBc/Hz
Φ_N	Phase noise	1 kHz offset		-94	-81	dBc/Hz
Φ_N	Phase noise	10 kHz offset		-101	-89	dBc/Hz

Notes:

- f_{clk} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{clk} specification
- CMOS logic levels can be used to drive the reference input. If the V_{DD} of the CMOS driver matches the V_{DD} of PLL IC, then the reference input can be DC coupled. Otherwise, the reference input should be AC coupled
- Parameter is guaranteed through characterization only and is not tested
- Parameters below are not tested for die sales. These parameters are verified during the element evaluation

Figure 4. RF Sensitivity vs Frequency (typical device at temperature = 25°C)

Figure 5. Typical Phase Noise for PE97022, $V_{DD} = 3.3V$, Temp = 25°C, $F_{vco} = 1.92$ GHz, $F_{comp} = 20$ MHz, Loop Bandwidth = 50 kHz

Functional Description

The PE97022 consists of a prescaler, counters, a phase detector, and control logic. The dual modulus prescaler divides the VCO frequency by either 10 or 11, depending on the value of the modulus select. Counters R and M divide the reference and prescaler output, respectively, by integer values stored in a 20-bit register. An additional counter (A) is used in the modulus select logic. The phase-frequency detector

generates up and down frequency control signals. The control logic includes a selectable chip interface. Data can be written via serial bus, parallel bus, or hardwired directly to the pins. There are also various operational and test modes and a lock detect output.

Figure 6. Functional Block Diagram

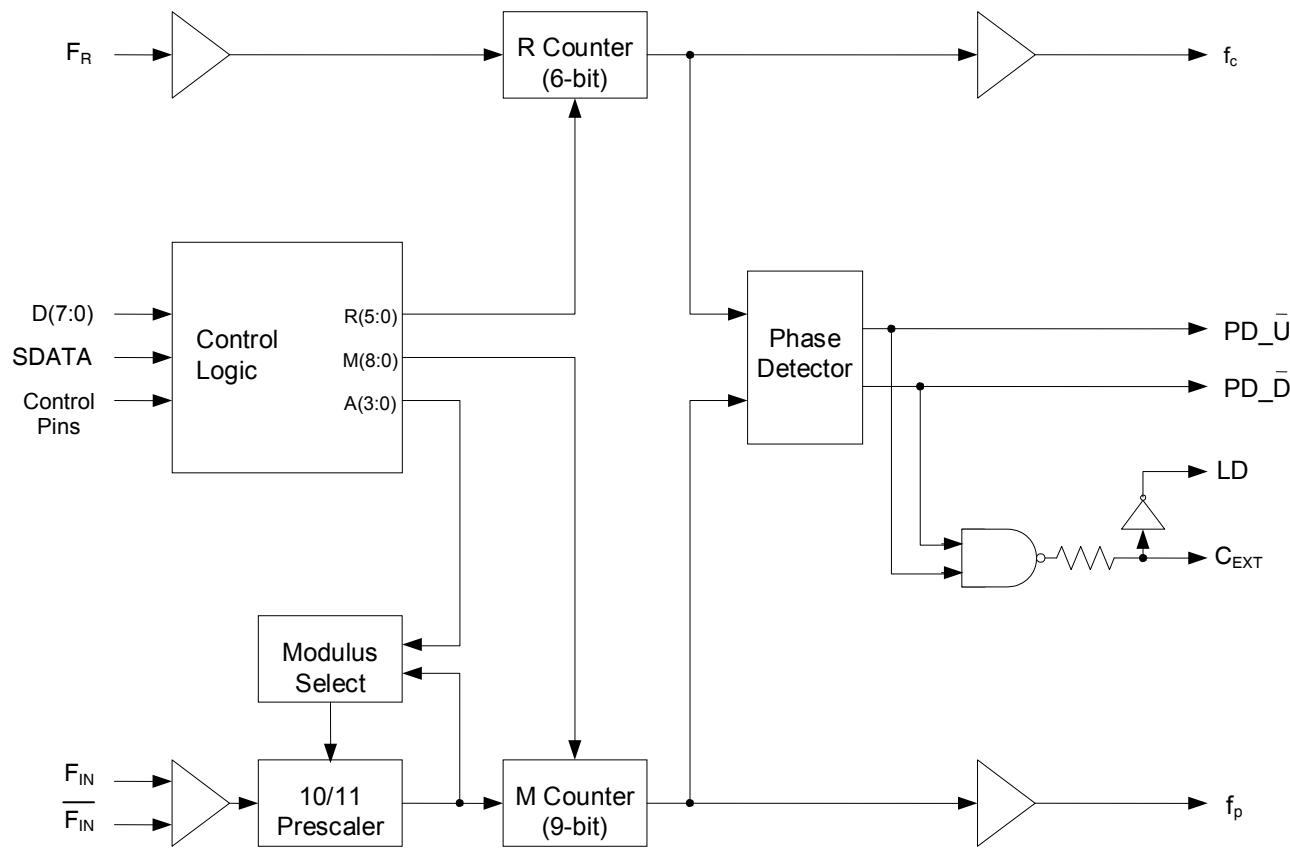


Figure 7. Equivalent Input Diagram: Reference Input

Reference Input

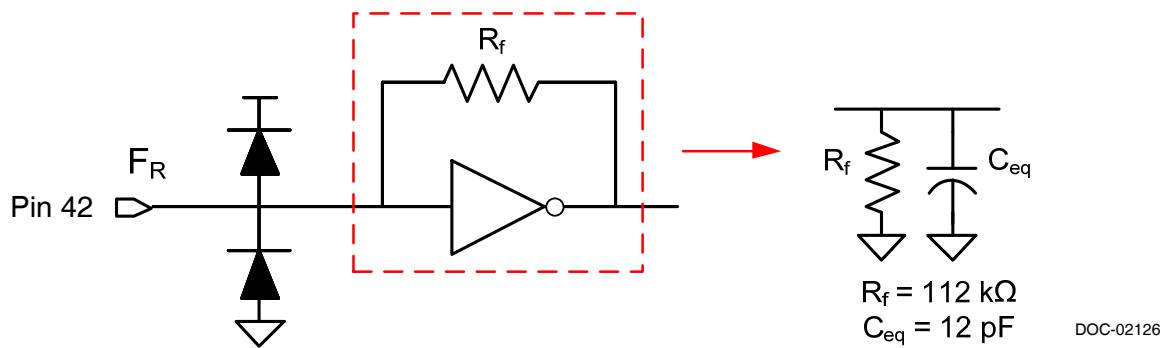


Figure 8. Equivalent Input Diagram: Main Input

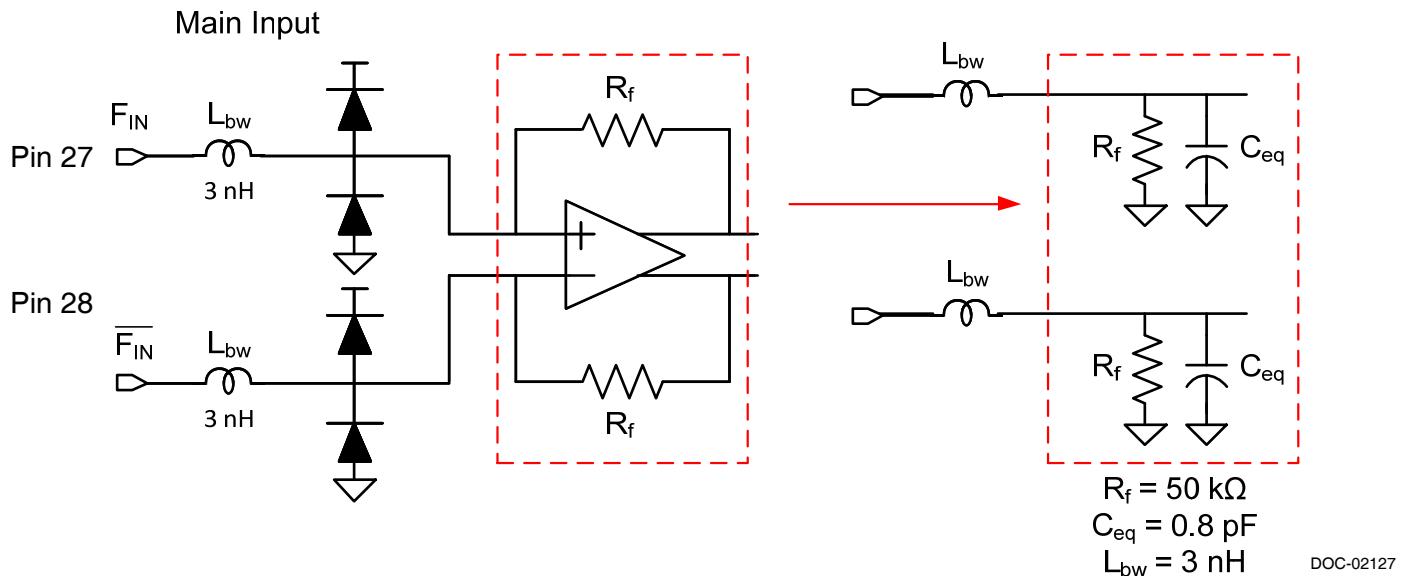
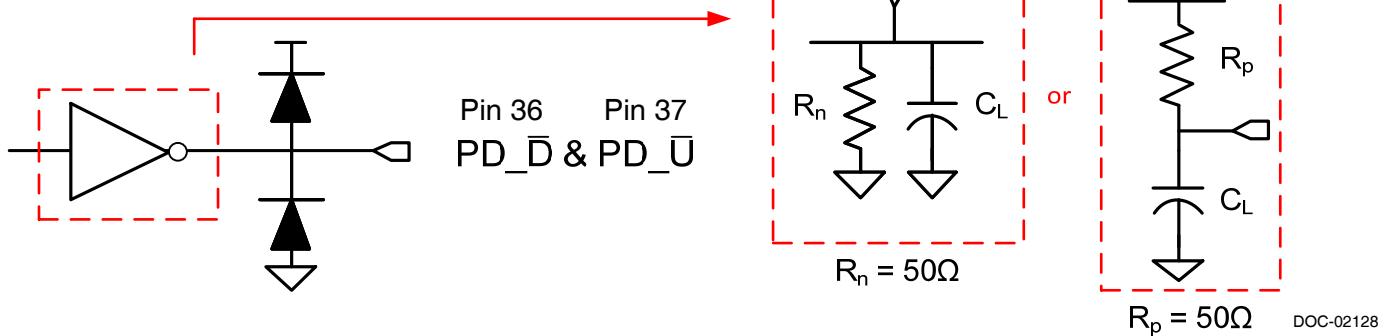


Figure 9. Equivalent Output Diagram: PD_̄D & PD_̄U Outputs

PD_̄D & PD_̄U Outputs



Main Counter Chain

Normal Operating Mode

The main counter chain divides the RF input frequency (F_{IN}) by an integer derived from the user-defined values in the M and A counters. It is composed of the 10/11 dual modulus prescaler, modulus select logic, and 9-bit M counter. Setting Pre_en “low” enables the 10/11 prescaler. Setting Pre_en “high” allows F_{IN} to bypass the prescaler and powers down the prescaler.

The output from the main counter chain (f_p) is related to the VCO frequency, F_{IN} , by the following equation:

$$f_p = F_{IN} / [10 \times (M + 1) + A] \quad (1)$$

where

$$A \leq M + 1, 1 \leq M \leq 511$$

When the loop is locked, F_{IN} is related to the reference frequency (F_R) by the following equation:

$$F_{IN} = [10 \times (M + 1) + A] \times [F_R / (R + 1)] \quad (2)$$

where

$$A \leq M + 1, 1 \leq M \leq 511$$

A consequence of the upper limit on A is that F_{IN} must be greater than or equal to $90 \times [F_R / (R + 1)]$ to obtain contiguous channels. Programming the M counter with the minimum value of “1” will result in a minimum M counter divide ratio of “2”.

In Direct Interface mode, main counter inputs M_7 and M_8 are internally forced low. In this mode, the M value is limited to $1 \leq M \leq 127$.

Prescaler Bypass Mode

Setting Pre_en “high” allows F_{IN} to bypass and power down the prescaler. In this mode, the 10/11 prescaler and A register are not active, and the input VCO frequency is divided by the M counter directly. The following equation relates F_{IN} to the reference frequency, F_R :

$$F_{IN} = (M + 1) \times [F_R / (R + 1)] \quad (3)$$

where

$$1 \leq M \leq 511$$

In Direct Interface mode, main counter inputs M_7 and M_8 are internally forced low. In this mode, the M value is limited to $1 \leq M \leq 127$.

Reference Counter

The reference counter chain divides the reference frequency (F_R) down to the phase detector comparison frequency, f_c .

The output frequency of the 6-bit R counter is related to the reference frequency by the following equation:

$$f_c = F_R / (R + 1) \quad (4)$$

where

$$0 \leq R \leq 63$$

Note that programming R with “0” will pass the reference frequency (F_R) directly to the phase detector.

In Direct Interface mode, R counter inputs R_4 and R_5 are internally forced low (“0”). In this mode, the R value is limited to $0 \leq R \leq 15$.

Register Programming

Parallel Interface Mode

Parallel Interface Mode is selected by setting the Bmode input “low” and the Smode input “low”.

Parallel input data, $D[7:0]$, are latched in a parallel fashion into one of three 8-bit primary register sections on the rising edge of M1_WR, M2_WR, or A_WR per the mapping shown in *Table 7*. The contents of the primary register are transferred into a secondary register on the rising edge of Hop_WR according to the timing diagram shown in *Figure 10*. Data is transferred to the counters as shown in *Table 6*.

The secondary register acts as a buffer to allow rapid changes to the VCO frequency. This double buffering for “ping-pong” counter control is programmed via the FSEL_P input. When FSEL_P is “high”, the primary register contents set the counter inputs. When FSEL_P is “low”, the secondary register contents are utilized.

Parallel input data, $D[7:0]$, are latched into the enhancement register on the rising edge of E_WR according to the timing diagram shown in *Figure 10*. This data provides control bits as shown in *Table 7* with bit functionality enabled by asserting the ENH input “low”.

Serial Interface Mode

Serial Interface mode is selected by setting the **Bmode** input “low” and the **Smode** input “high”. While the **E_WR** input is “low” and the **S_WR** input is “low”, serial input data (SDATA input), B_0 to B_{19} , is clocked serially into the primary register on the rising edge of SCLK, MSB (B_0) first. The contents from the primary register are transferred into the secondary register on the rising edge of either **S_WR** or **Hop_WR** according to the timing diagram shown in *Figure 11*. Data is transferred to the counters as shown in *Table 6*.

The double buffering provided by the primary and secondary registers allows for “ping-pong” counter control using the **FSELS** input. When **FSELS** is “high”, the primary register contents set the counter inputs. When **FSELS** is “low”, the secondary register contents are utilized.

While the **E_WR** input is “high” and the **S_WR** input is “low”, serial input data (SDATA input), B_0 to B_7 , is clocked serially into the enhancement register on the rising edge of SCLK, MSB (B_0) first. The enhancement register is double buffered to prevent inadvertent control changes during serial loading, with buffer capture of the serially-entered data performed on the falling edge of **E_WR** according to the timing diagram shown in *Figure 11*. After the falling edge of **E_WR**, the data provides control bits as shown in *Table 8* with bit functionality enabled by asserting the **Enh** input “low”.

Direct Interface Mode

Direct Interface mode is selected by setting the **Bmode** input “high”. Counter control bits are set directly at the pins as shown in *Table 6*. In Direct Interface mode, main counter inputs M_7 and M_8 , and R counter inputs R_4 and R_5 are internally forced low (“0”).

Table 6. Primary Register Programming

Interface Mode	ENH	Bmode	Smode	R ₅	R ₄	M ₈	M ₇	Pre_en	M ₆	M ₅	M ₄	M ₃	M ₂	M ₁	M ₀	R ₃	R ₂	R ₁	R ₀	A ₃	A ₂	A ₁	A ₀
Parallel	1	0	0	M2_WR rising edge load				M1_WR rising edge load										A_WR rising edge load					
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Serial*	1	0	1	B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇	B ₈	B ₉	B ₁₀	B ₁₁	B ₁₂	B ₁₃	B ₁₄	B ₁₅	B ₁₆	B ₁₇	B ₁₈	B ₁₉
Direct	1	1	X	0	0	0	0	Pre_en	M ₆	M ₅	M ₄	M ₃	M ₂	M ₁	M ₀	R ₃	R ₂	R ₁	R ₀	A ₃	A ₂	A ₁	A ₀

* Serial data clocked serially on SCLK rising edge while **E_WR** “low” and captured in secondary register on **S_WR** rising edge.

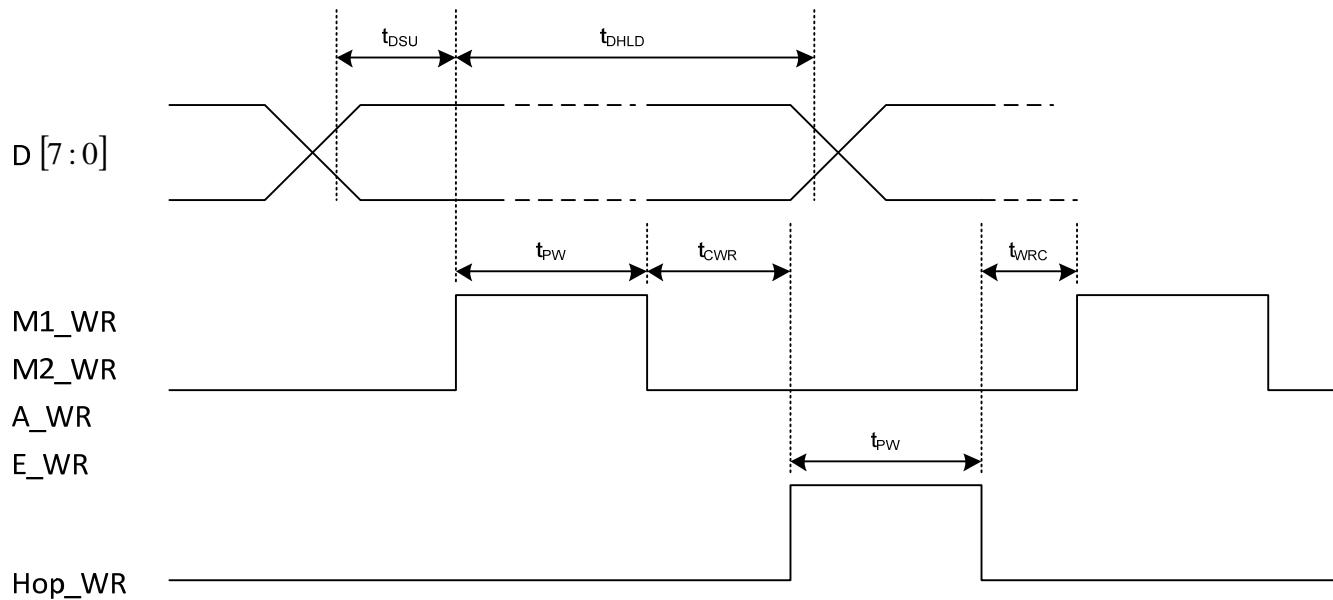
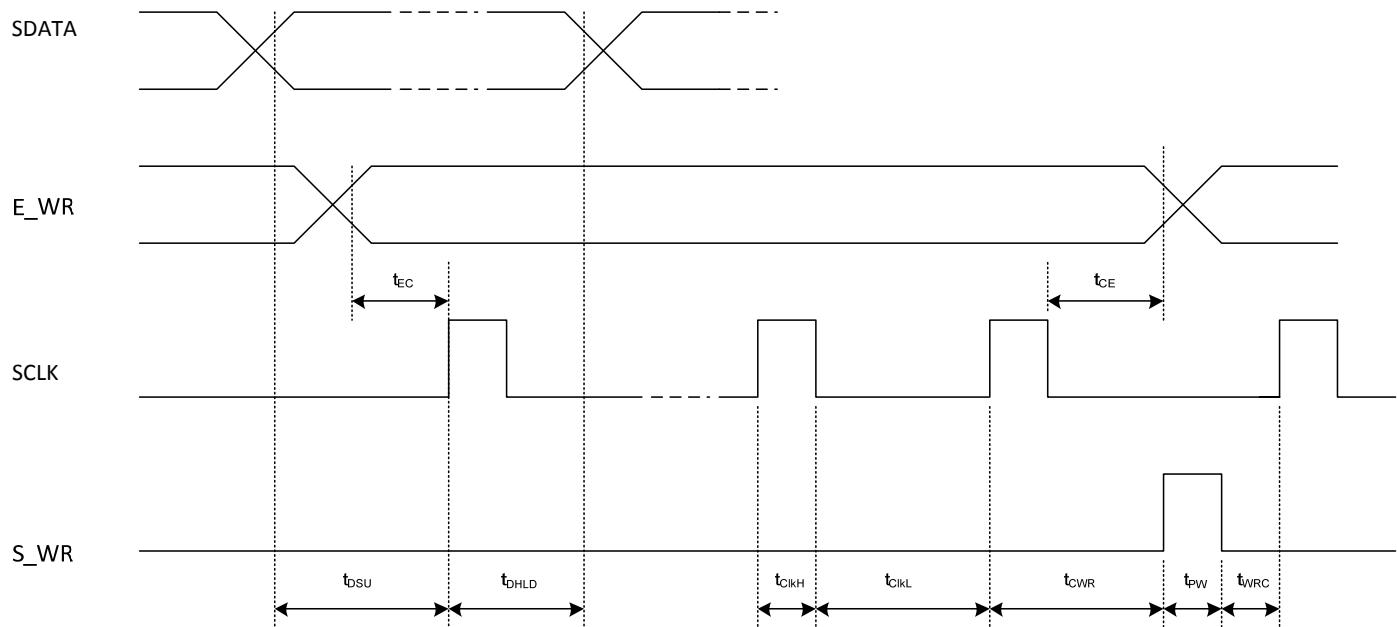


Table 7. Enhancement Register Programming

Interface Mode	ENH	Bmode	Smode	Reserved	Reserved	Reserved	Power down	Counter load	MSEL output	Prescaler output	f _c , f _p OE
E_WR rising edge load											
Parallel	0	0	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Serial*	0	0	1	B ₀	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇

* Serial data clocked serially on SCLK rising edge while **E_WR** “high” and captured in the double buffer on **E_WR** falling edge



Figure 10. Parallel Interface Mode Timing Diagram

Figure 11. Serial Interface Mode Timing Diagram


Enhancements Register

The functions of the enhancement register bits are shown below with all bits active “high”.

Table 8. Enhancement Register Bit Functionality

Bit Function		Description
Bit 0	Reserved**	
Bit 1	Reserved**	
Bit 2	Reserved**	
Bit 3	Power down	Power down of all functions except programming interface
Bit 4	Counter load	Immediate and continuous load of counter programming as directed by the <u>Bmode</u> and <u>Smode</u> inputs
Bit 5	MSEL output	Drives the internal dual modulus prescaler modulus select (MSEL) onto the Dout output
Bit 6	Prescaler output	Drives the raw internal prescaler output (fmain) onto the Dout output
Bit 7	$f_p, f_c \bar{OE}$	f_p, f_c outputs disabled

** Program to 0

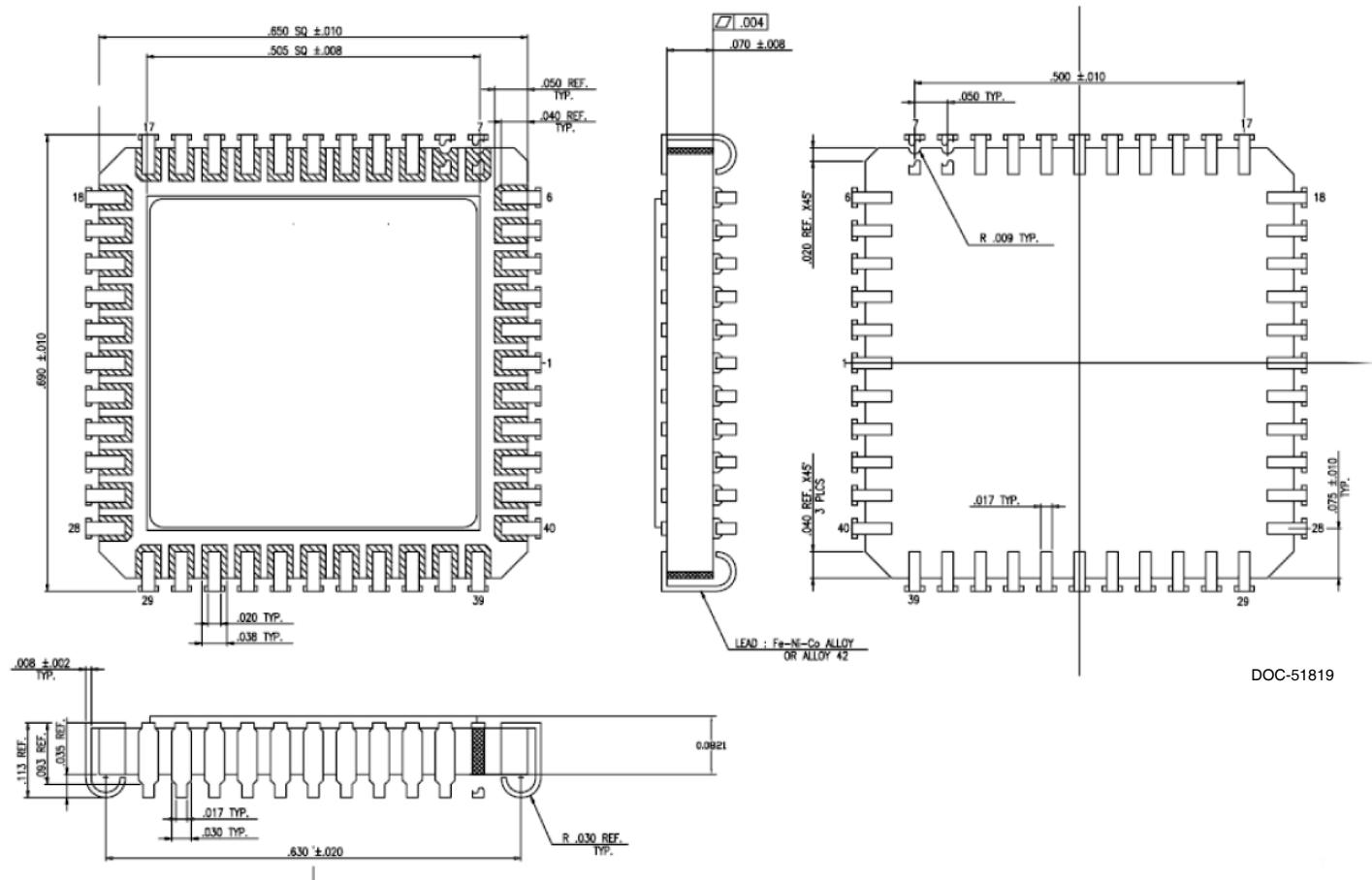
Phase Detector

The phase detector is triggered by rising edges from the main Counter (f_p) and the reference counter (f_c). It has two outputs, namely $PD_{\bar{U}}$, and $PD_{\bar{D}}$. If the divided VCO leads the divided reference in phase or frequency (f_p leads f_c), $PD_{\bar{D}}$ pulses “low”. If the divided reference leads the divided VCO in phase or frequency (f_c leads f_p), $PD_{\bar{U}}$ pulses “low”. The width of either pulse is directly proportional to phase offset between the two input signals, f_p and f_c . The phase detector gain is 430 mV / radian.

$PD_{\bar{U}}$ and $PD_{\bar{D}}$ are designed to drive an active loop filter which controls the VCO tune voltage. $PD_{\bar{U}}$ pulses result in an increase in VCO frequency and $PD_{\bar{D}}$ results in a decrease in VCO frequency.

A lock detect output, LD is also provided, via the pin C_{EXT} . C_{EXT} is the logical “NAND” of $PD_{\bar{U}}$ and $PD_{\bar{D}}$ waveforms, which is driven through a series 2 kΩ resistor. Connecting C_{EXT} to an external shunt capacitor provides integration. C_{EXT} also drives the input of an internal inverting comparator with an open drain output. Thus LD is an “AND” function of $PD_{\bar{U}}$ and $PD_{\bar{D}}$. See *Figure 6* for a schematic of this circuit.

Figure 12. Package Drawing
44-lead CQFJ



All dimensions are in inches

Figure 13. Top Marking Specifications



△ = Pin 1 indicator

97022-XX = Part number (XX will be specified by the PO and/or the assembly instructions)

YYWW = Date Code, last two digits of the year and work week

ZZZZZZZ = Lot Code (up to seven digits)

nnnnnn = Serial number of the part (up to six digits)

Table 9. Ordering Information

Order Code	Description	Package	Shipping Method
97022-01 ¹	Engineering samples	44-lead CQFJ	40 units / tray
97022-11	Flight units	44-lead CQFJ	40 units / tray
97022-99	Die production units	Die	100 units / waffle pack
97022-00	Evaluation kit		1 / box

Note 1: The PE97042-01 devices are ES (Engineering Sample) prototype units intended for use as initial evaluation units for customers of the PE97042-11 flight units. The PE97042-01 device provides the same functionality and footprint as the space qualified device, and intended for engineering evaluation only. They are tested at 25°C only and processed to a non-compliant flow (e.g. No Burn-In, etc.). These units are not suitable for qualification, production, radiation testing or flight use.

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

Advance Information: The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification: The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product. **Product Specification:** The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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