RFMD
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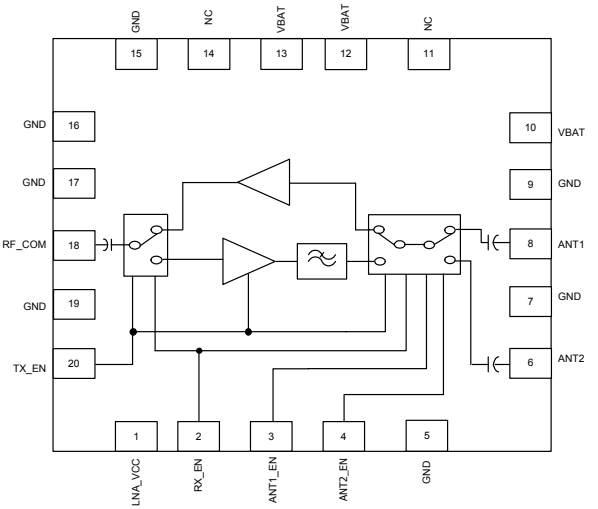
RF6575

3.0V TO 3.6V, 2.4GHz FRONT END MODULE

Package Style: QFN, 20-Pin, 3.5mmx3.5mmx0.5mm



Functional Block Diagram

Features

- TX Output Power = 22dBm
- Integrated RF Front End Module with TX/RX switch, PA, filter, LNA, and DP2T switch.
- 50Ω single-ended bidirectional Transceiver interface.

Applications

- ZigBee® 802.15.4 Based Systems for Remote Monitoring and Control
- WiFi 802.11b/g
- 2.4GHz ISM band applications
- Smart Meters for Energy Management

Product Description

The RF6575 integrates a complete solution in a single Front End Module (FEM) for WiFi and ZigBee® applications in the 2.4GHz to 2.5GHz band. This FEM integrates the PA plus harmonic filter in the transmit path. The RF6575 has an integrated LNA. Also, the RF6575 provides a single balanced TDD access for RX and TX paths along with two ports on the output for connecting a diversity solution or a test port. The device is provided in a 3.5mm x 3.5mm x 0.5, 20-pin QFN package.

Ordering Information

RF6575	3.3V Front End Module for AMR systems in the 2.4GHz to 2.5GHz Band
RF6575SQ	Standard 25 piece bag
RF6575SR	Standard 100 piece reel
RF6575TR13	Standard 2500 piece reel
RF6575PCK-410	Fully assembled evaluation board and 5 loose pieces

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	5.5	V
DC Supply Current	250	mA
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
ESD Human Body Model RF Pins	1000	V
ESD Human Body Model All Other Pins	500	V
ESD Charge Device Model All Pins	500	V
Moisture Sensitivity Level	MSL 2	
Maximum Input Power to PA	+10	dBm
Maximum Input Power to LNA	+5	dBm

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Specifications must be met across supply voltage, control voltage, and temperature ranges unless otherwise specified.
V_{BATT}	3.0	3.3	3.6	V_{DC}	
Operating Temperature Range	-40	+25	+85	°C	
Z_O		50		Ω	
Off Mode Current		1		μA	All logic low
TX Path					
Frequency	2400		2483	MHz	
Input Return Loss	12			dB	
Output Return Loss	9			dB	
Transmit Path Gain	24	28		dB	
Gain Flatness	-0.8		+0.8	dB	
Rated Output Power		22		dBm	Nominal conditions
	20			dBm	All conditions
Supply Current		200		mA	P_O=22dBm 802.15.4 OQPSK
		170		mA	P_O=20dBm 802.15.4 OQPSK
		130		mA	P_O=16dBm 802.15.4.OQPSK
Thermal Resistance		66		°C/W	V_{CC} = 3.6V, P_{OUT} = 22dBm, T_{REF} = 85°C
2nd harmonic level			-42	dBm/MHz	P_O=20dBm
3rd harmonic level			-42	dBm/MHz	P_O=20dBm
VSWR Stability and Load	4:1				
VSWR No Damage	8:1				
Gain Settling Time		1	2	uS	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RX Path					
Frequency	2400		2483	MHz	
Gain	10	13	15.5	dB	
Noise Figure		2.5	3	dB	
Current		8		mA	
IIP3		7		dBm	
Gain Flatness	-0.5		+0.5	dB	
Input Return Loss	12	15		dB	
Output Return Loss		9.5		dB	
Maximum Input Power	5			dBm	
Antenna Switch					
RF-to-Control Isolation	50			dB	
RF-to-ANT Isolation	17	20		dB	
RF-to-RF Isolation	18	20		dB	
T/R Switching Time			1	µs	
Logic Level "HIGH" Input Voltage	V_{CC}-0.3		=V_{CC}	V	
Logic Level "LOW" Input Voltage	0.0		+0.2	V	
Input Source Current at Logic "HIGH"		5	10	uA	
Switch Leakage Current at Logic "LOW"		0.5		uA	

Control Logic

Switch Control Logic	TX_EN	RX_EN	ANT1_EN	ANT2_EN
Tx, Antenna 1	High	Low	High	Low
Tx, Antenna 2	High	Low	Low	High
Rx, Antenna 1	Low	High	High	Low
Rx, Antenna 2	Low	High	Low	High
All Off	Low	Low	Low	Low

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Pin	Function	Description
1	LNA_VCC	Voltage supply for the LNA.
2	RX_EN	Enable voltage for the LNA and receive switch. See logic table for operation.
3	ANT1_EN	Control pin for Antenna 1 switch. See logic table for operation.
4	ANT2_EN	Control pin for Antenna 2 switch. See logic table for operation.
5	GND	Ground.
6	ANT2	This is a common port (antenna). It is matched to 50Ω and DC block is provided internally.
7	GND	Ground.
8	ANT1	This is a common port (antenna). It is matched to 50Ω and DC block is provided internally.
9	GND	Ground.
10	VBAT	Voltage supply for PA 2nd stage. An external 1uF capacitor might be needed for low frequency decoupling.
11	N/C	No connect.
12	VBAT	Voltage supply for PA 1st stage. An external 1uF capacitor might be needed for low frequency decoupling.
13	VBAT	Voltage supply (control circuitry). An external 1uF capacitor might be needed for low frequency decoupling.
14	N/C	No Connect.
15	GND	Ground.
16	GND	Ground.
17	GND	Ground.
18	RF_COM	Bi-directional transmit/receive port for interfacing to TXVR SOIC. It is matched to 50Ω and DC block is provided internally.
19	GND	Ground.
20	TX_EN	Enable voltage for the PA and transmit switch. See logic table for operation.

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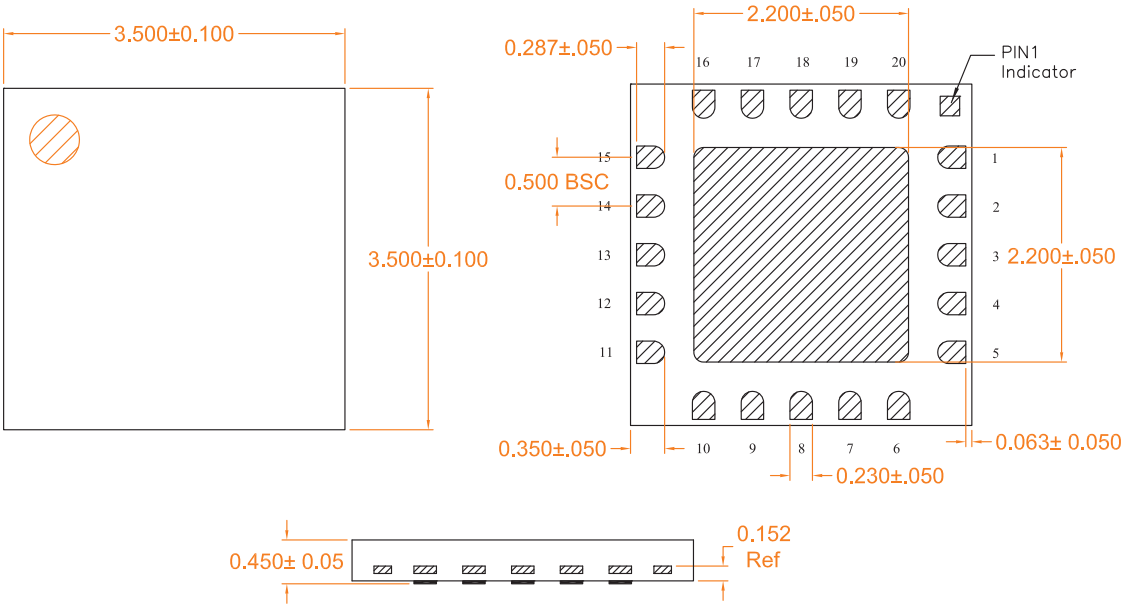
Package Drawing



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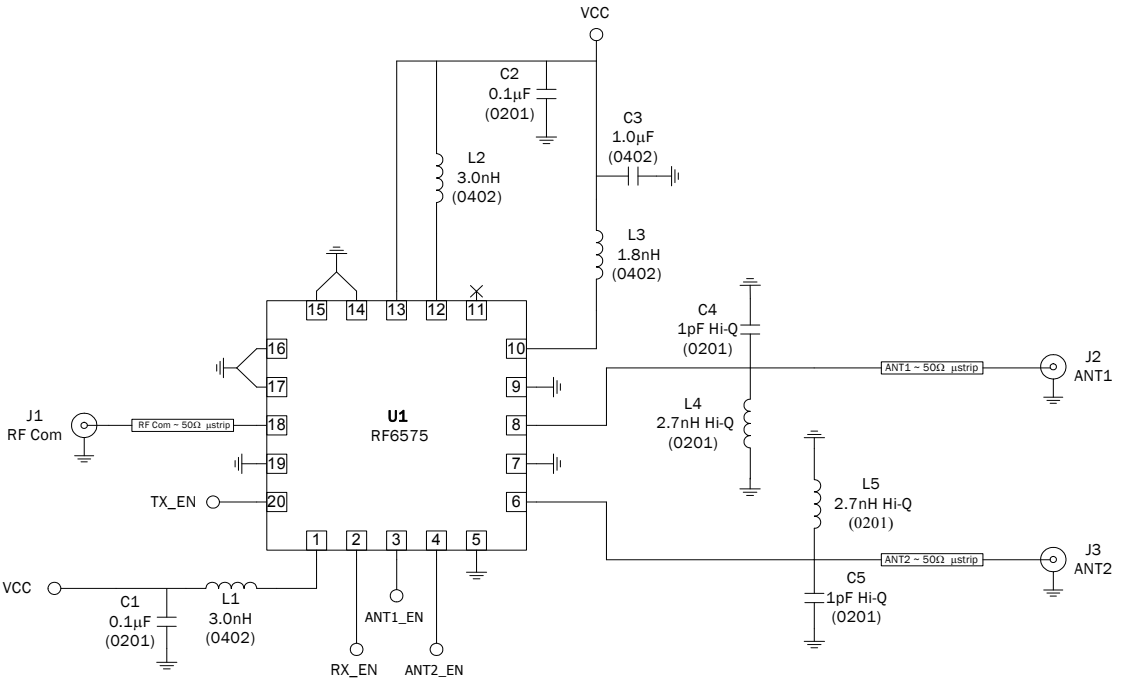
Evaluation Board Schematic



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PCB Design Requirements

PCB Surface Finish

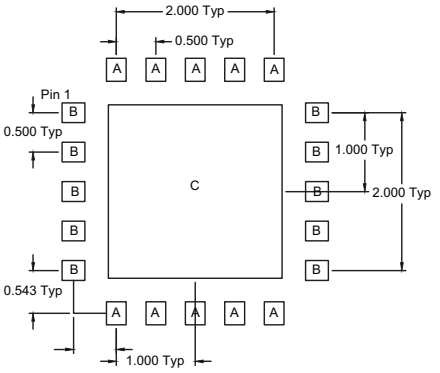
The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

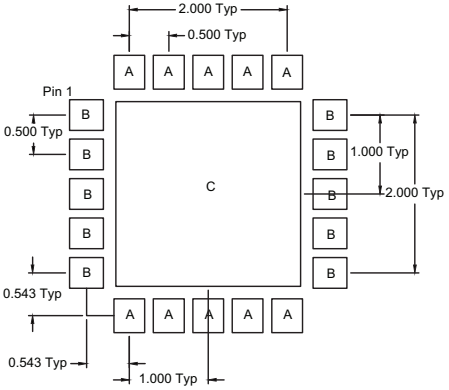
PCB Metal Land and Solder Mask Pattern

A = 0.250 x 0.290 (mm) Typ Rounded Rectangle 50%
B = 0.290 x 0.250 (mm) Typ Rounded Rectangle 50%
C = 2.200 (mm) Sq Rounded Rectangle 5%



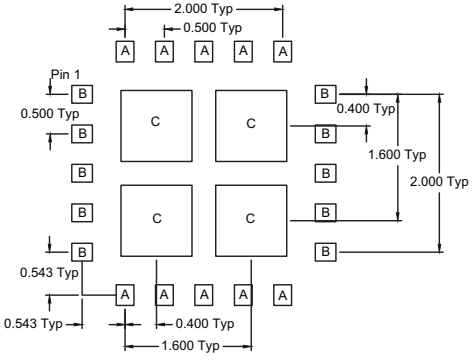
PCB METAL LAND PATTERN

A = 0.390 x 0.430 (mm) Typ Rounded Rectangle 50%
B = 0.430 x 0.390 (mm) Typ Rounded Rectangle 50%
C = 2.340 (mm) Sq Rounded Rectangle 5%



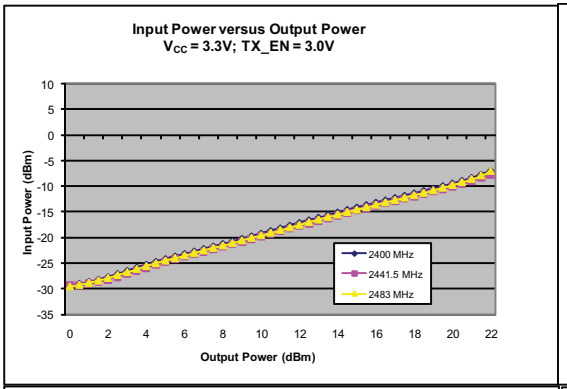
PCB SOLDER MASK PATTERN

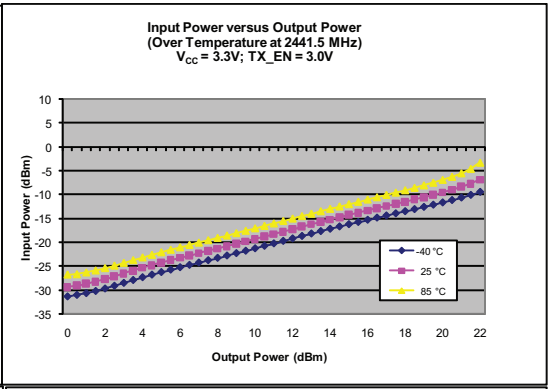
A = 0.225 x 0.261 (mm) Typ Rounded Rectangle 10%
B = 0.261 x 0.225 (mm) Typ Rounded Rectangle 10%
C = 0.900 (mm) Sq Typ Rounded Rectangle 10%

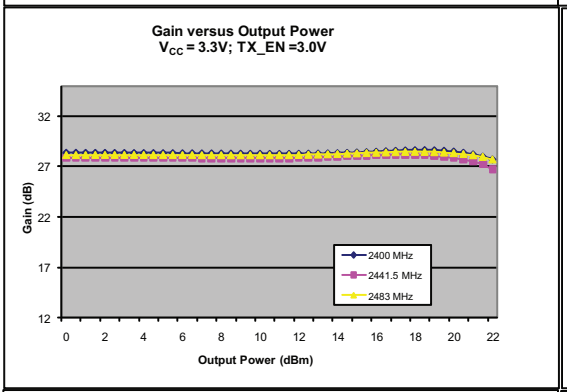


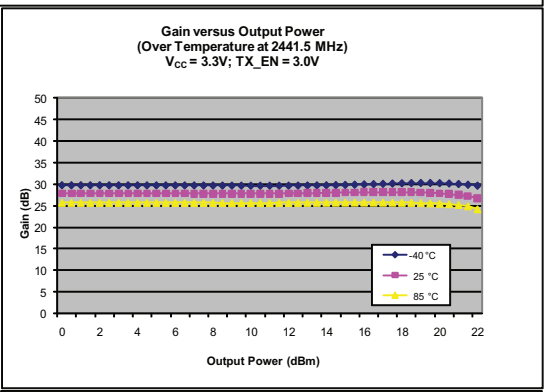
PCB STENCIL PATTERN

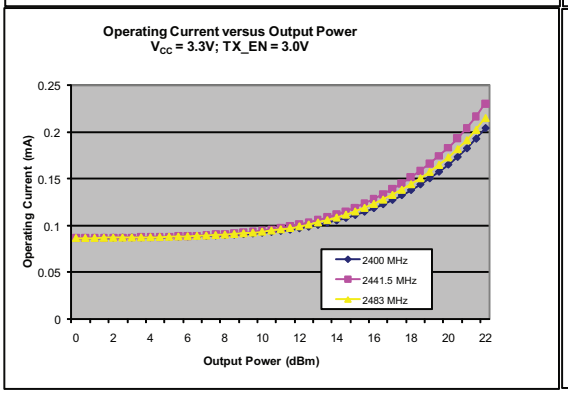
Thermal vias for center slug “C” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and this electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout

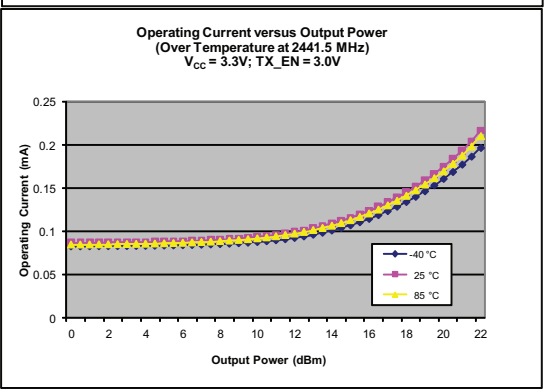












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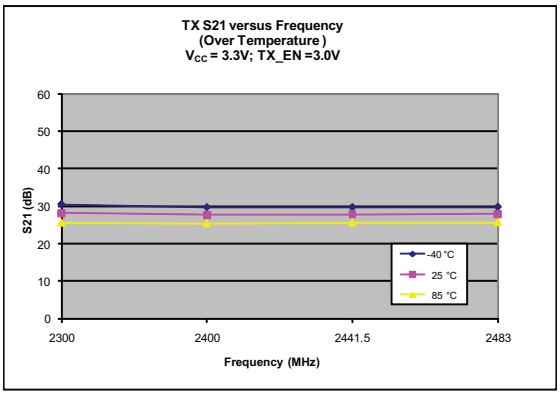
TX S21 versus Frequency
(Over Temperature)
V_{CC} = 3.3V; TX_EN =3.0V
S21 (dB)
60
50
40
30
20
10
0
2300
2400
2441.5
2483
Frequency (MHz)
-40 °C
25 °C
85 °C