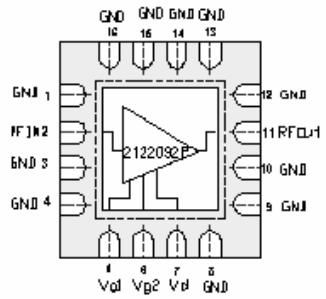
1.0 – 6 GHz Ultra Low Noise Amplifier

Features

- **Frequency Range: 1.0- 6 GHz**
- **0.7 dB mid-band Noise Figure**
- **18 dB mid band Gain**
- **13dBm Nominal P1dB**
- **Bias current : 50mA**
- **0.15-um InGaAs pHEMT Technology**
- **16-Pin QFN Plastic Package : 3mmx3mmx1mm**

Functional Diagram



Typical Applications

- **Cellular system**
- **Base stations**
- **Applications from 1 to 6GHz in Balanced configuration**
- **Communication receivers and transmitters.**

Description

AMT 2122092P is an Ultra Low Noise single stage Amplifier MMIC combining high gain and state of the art noise figure. No-off-chip components are needed, except for additional bypass capacitors in DC bias path for reliable operation. Matching network, DC Blocks and bypass capacitors are provided on-chip for simplification of assembly operation. The amplifier operates on Drain Bias of +5V and Gate biases of +2V & -0.4 V supply. The bias current can be tuned from 30 to 70 mA as per requirement with minor variation in performance. The LNA features 18dB mid-band gain and 0.7 dB mid-band noise figure (typical). The die is fabricated using reliable Low noise 0.15um InGaAs pHEMT process. This chip is available in low cost 16 pin QFN plastic package.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Positive DC Supply	10	V
RF Input Power	23	dBm
Supply current	100	mA
Operating Temperature	-55 to +85	^{o}C
Storage Temperature	-65 to +150	^{o}C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, Z_o =50 Ω

Vdd = +5V, Vg1= -0.4V, Vg2= +2V

Parameter	Min.	Typ.	Max.	Units
Frequency	1.0	-	6	GHz
RF Performance between 2.5-4 GHz unless otherwise stated:				
Gain	17	18	20	dB
Gain Flatness	-	± 0.5	± 0.7	dB
Noise Figure	0.6	0.7	0.9	dB
Input Return Loss	-5	-8	-	dB
Output Return Loss	-8	-15	-	dB
Reverse Isolation	-	-31	-	dB
Output Power (P1dB) @ 3.3 GHz	+10	+13	-	dBm
Output Third Order Intercept(IP3) [2]	-	30	-	dBm
Supply Current[3]	30	50	70	mA

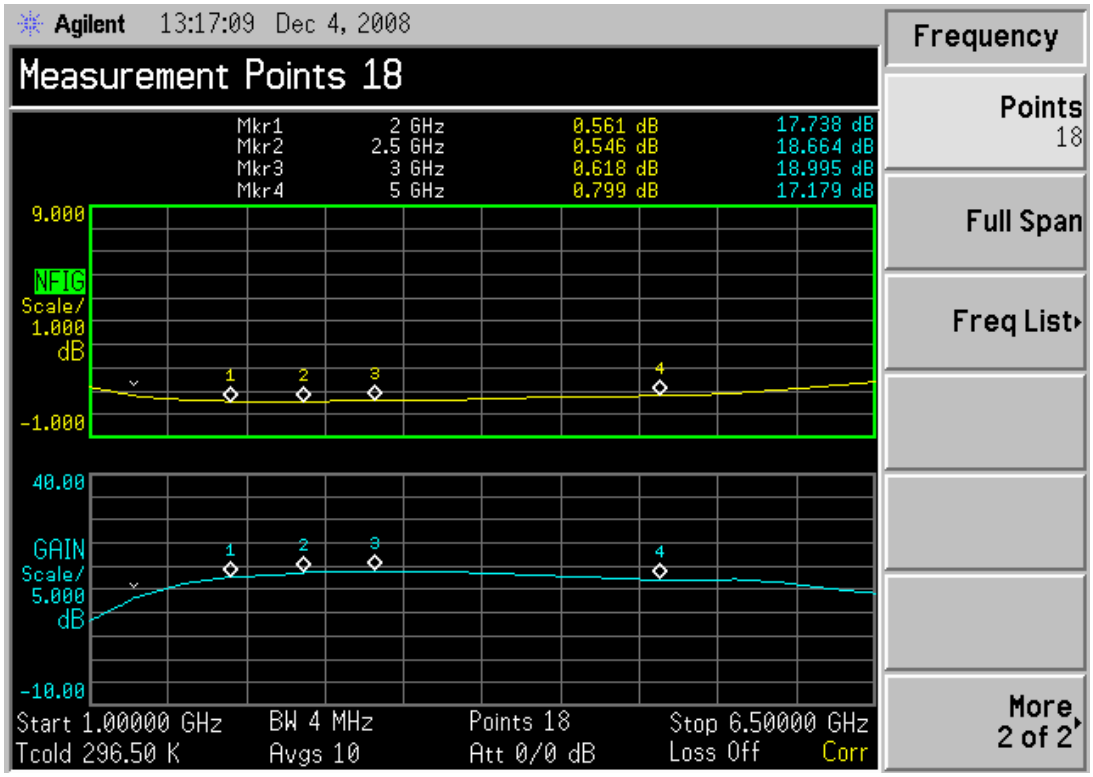
Note:

1. Electrical specifications as measured in test fixture.
2. Estimated value.
3. Supply current tunable with gate bias (Vg1) with minor variation in performance.
4. I/O Match can be improved in the required band with stub matching.

Test fixture data

Vdd =+5V ,Vg1= -0.4V, Vg2= +2V, Total Current = 50mA , T_A = 25 ^oC

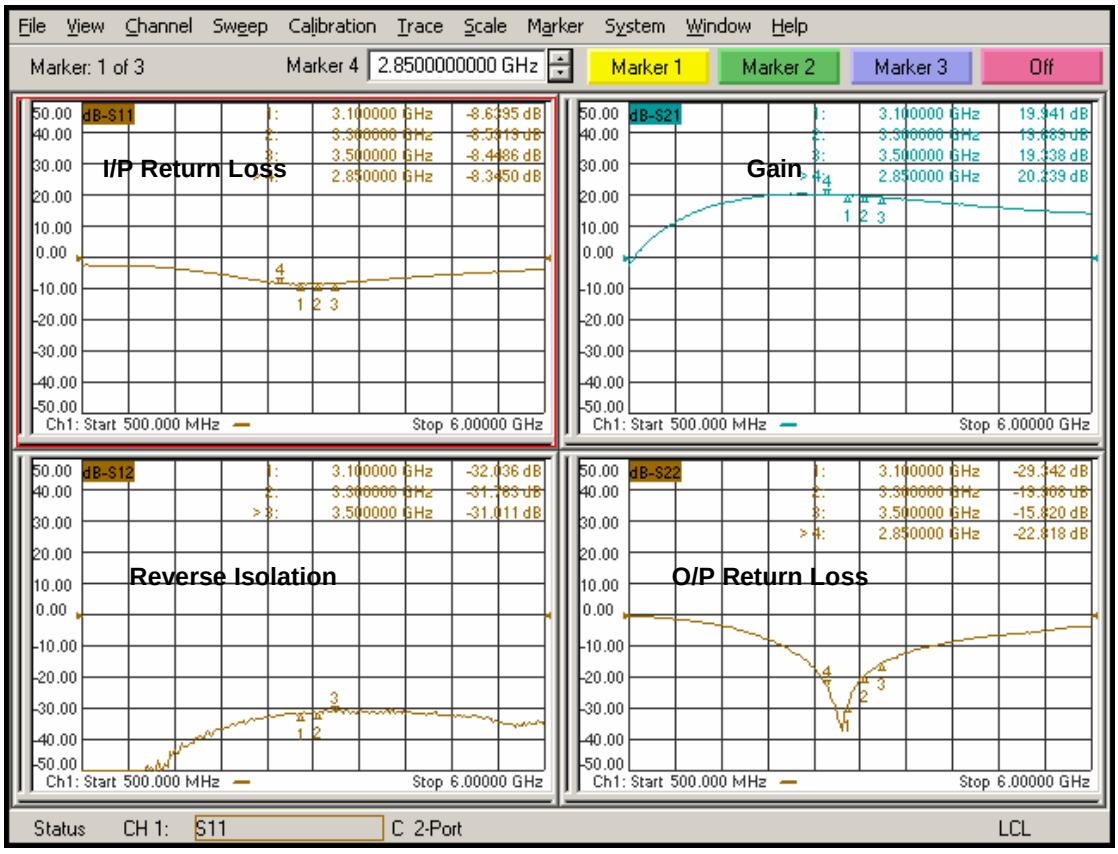
Noise Figure



Test fixture data

Vdd =+5V ,Vg1= -0.4V, Vg2= +2V, Total Current = 50mA , T_A = 25 ^oC

RF Performance



Test fixture data

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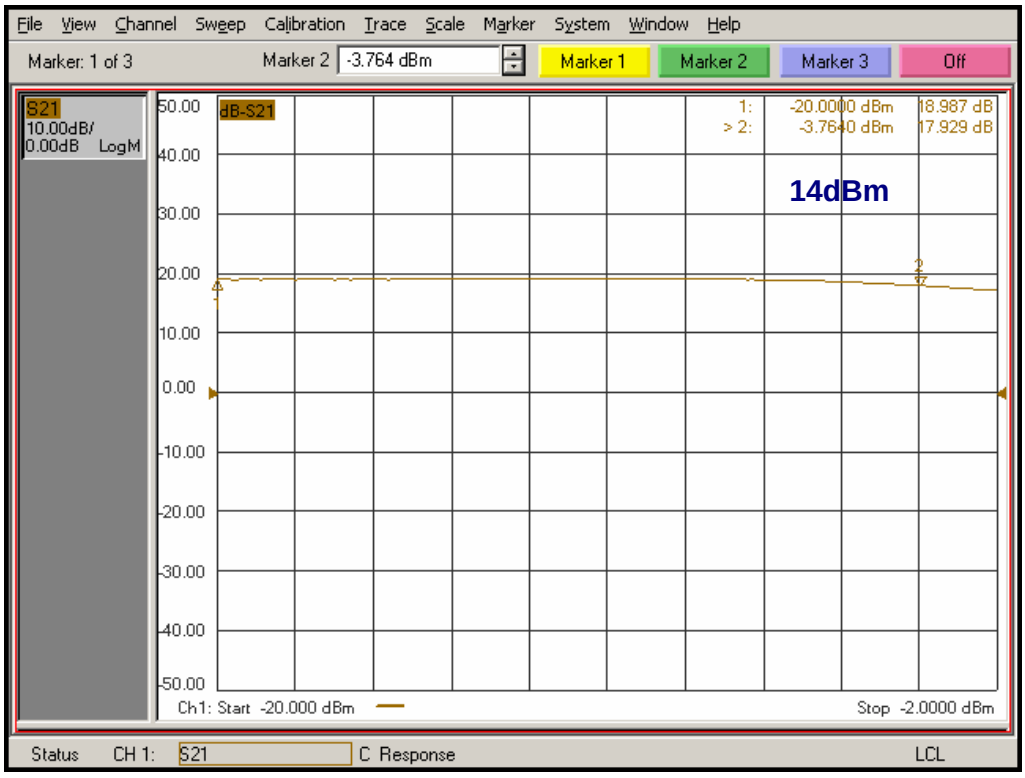
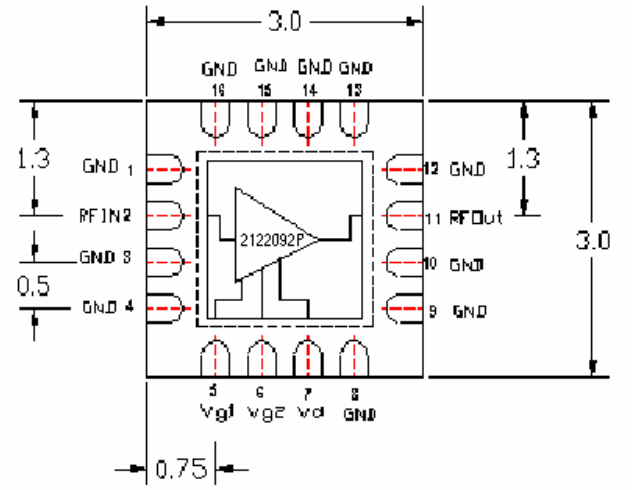
Gain compression at 3.3 GHz



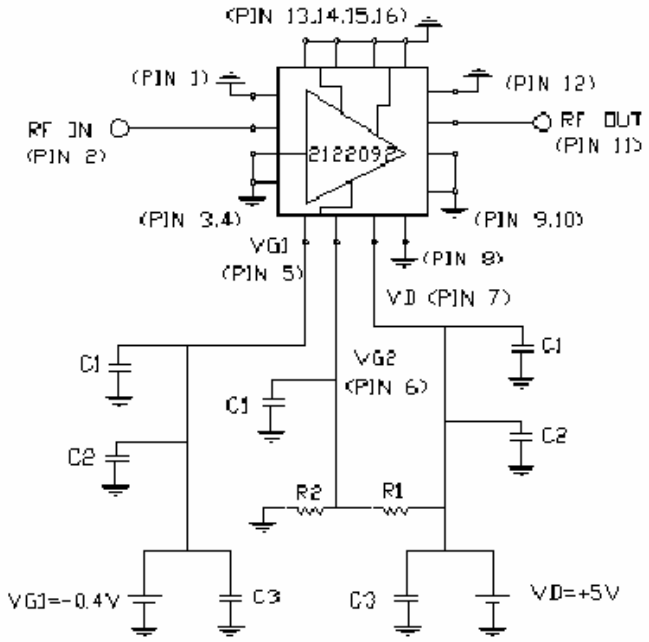
Mechanical Characteristics (16 Pin 3mmx 3mm x 1mm QFN Package)



Pin Configuration

PIN	Function	Description
1,3,4,8,9,10,12,13,14,15,16	GND	Ground
2	RF In	RF Input
5	Vg1	1st Gate Voltage Input
6	Vg2	2nd Gate Voltage Input
7	Vdd	Drain Voltage Input
11	RF Out	RF output

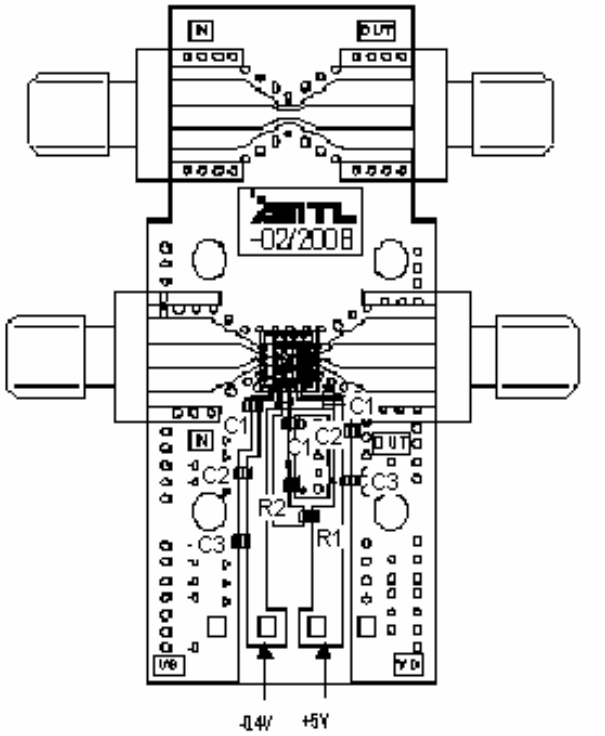
Application Circuit



Note :

1. R1=15K, R2=10K
2. C1=470pF
3. C2=0.1uF
4. C3=1uF

Evaluation PCB



List of Components

Component ID	Value	Description / Part No.
C1	470 pF	1st Bypass capacitor (0402Pkg)
C2	0.1 uF	2nd Bypass Capacitor (0402 Pkg.)
C3	1uF	2nd Bypass Capacitor (0402 Pkg.)
R1	15K Ohm	Resistor in VG2 Bias network (0402 Pkg.)
R2	10K Ohm	Resistor in VG2 Bias network (0402 Pkg.)
Board Material : RT/Duroid 5880, 10mil		

***N*ote:**

1. Input and Output Lines should be of 50Ω I mpedance.
2. Sufficient numbers of via holes should be provided for good grounding.
3. Vg2 can be applied independently without using R1 & R2 and tuned.
4. All capacitors shown in the assembly diagram are multi-layer capacitors.
5. Evaluation PCB is available from AMTL upon request.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice