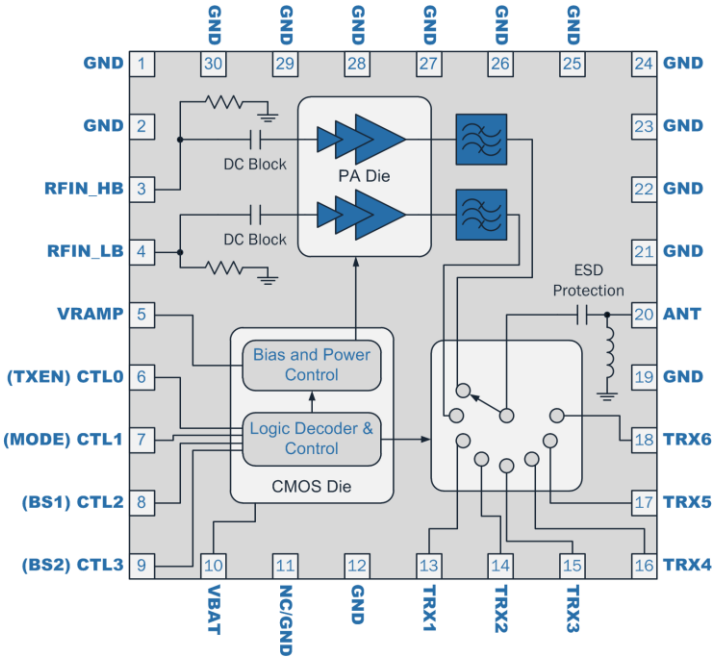
RF3241

Quad-Band GSM, Polar EDGE Transmit Module, Six UMTS TRX Switch Ports

The RF3241 is a quad-band GSM/GPRS, Polar EDGE transmit module with six interchangeable RF switch ports. The power amplifier supports GSM and EDGE Class 12 transmit in the 850, 900, DCS, and PCS bands. The six switch ports support UMTS transmit power. RF3241 operates in saturated mode for both GSM and EDGE transmit for optimum efficiency.



Functional Block Diagram

Ordering Information

RF3241SB	5-Piece Sample Bag
RF3241SQ	25-Piece Sample Bag
RF3241SR	100-Piece 7” Sample Reel
RF3241TR13	2500-Piece 13” Reel
RF3241PCBA	Fully Assembled Evaluation Board

Package: Module, 30-pin, 6.0mm x 6.0mm x 1.0mm

Features

- EDGE Large Signal Polar Modulation Capable
- 8kV Robust ESD Protection at Antenna Port
- Supports 4.5V max VBAT
- Six high linearity TRX Ports
- Low TRX Insertion Loss
- High TRX to TRX isolation

Applications

- EDGE Large Signal Polar Modulation Transceivers
- GSM, EDGE, Uplink Plus Multiband 3G
- WEDGE, Handsets and Connected Devices
- Battery Powered, Multimode Mobile Devices

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS20160209

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (VBAT)	-0.3 to 6.0	V
Control Voltage (VRAMP)	-0.3 to 3.0	V
Control Voltage (CTL0, CTL1, CTL2, CTL3)	-0.3 to 3.0	V
RF Input Power	10	dBm
Transmit Duty Cycle, Period = 4.6ms	50	%
Output Load VSWR	20:1	
Operating Temperature Range	-30 to +85	°C
Storage Temperature Range	-55 to +150	°C
ESD, HBM, JESD22-A114	1000	V
ESD, CDM, JESD22-C101	1000	V
ESD, CD ANT, IEC 61000-4-2	8000	V
Moisture Sensitivity Level	MSL3	

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Requirements					**Nominal test conditions unless otherwise stated. All unused ports terminated in 50Ω. VBAT=3.5V, P_{IN}=3dBm, T_A=+25°C**
Operating Ambient Temperature (T_A)	-30	25	85	°C	
Supply Voltage, VBAT	3.2	3.5	4.5	V	Normal Operation
Leakage Current, VBAT	-	1	10	µA	CTL0, CTL1, CTL2, CTL3, VRAMP ≤0.30V; VBAT≤4.5V
VRAMP Voltage	-	0.25	-	V	GSM/EDGE transmit; minimum RF output power
	-	-	1.6	V	GSM/EDGE transmit; maximum RF output power
VRAMP Capacitance	-	-	10	pF	DC to 2MHz
VRAMP Current	-	-	10	µA	0 ≤ VRAMP ≤ 1.60V
VRAMP 3dB Loop Bandwidth	2.5	10	-	MHz	EDGE Power Control Range
VRAMP Group Delay	-	45	-	ns	At frequency of -3dB BW
VRAMP Group Delay Variation	-20	-	20	ns	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C
Control Voltage Logic Low	0	0	0.5	V	CTL0, CTL1, CTL2, CTL3
Control Voltage Logic High	1.25	2.0	3.0	V	
Control Current	-	-	10	µA	
RF Port Impedance	-	50	-	Ω	Pins 3, 4, 13, 14, 15, 16, 17, 18, 20

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Transmit, 850 Band					**Nominal test conditions unless otherwise stated. All unused ports terminated in 50Ω. VBAT=3.5V; P_{IN}=3dBm; T_A=+25°C; VRAMP=1.6V; Duty Cycle=25%; Period=4.6ms; Logic State=TX_LB**
Frequency	824	-	849	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR	-	-	2.5	X:1	5dBm ≤ P_{OUT} ≤ 33dBm
RF Output Power (P_{OUT}), Maximum	33.3	34.7	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	31	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
RF Output Power (P_{OUT}), EDGE	27	-	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	25	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
Efficiency (PAE), 33.0dBm	36	41	-	%	VRAMP adjusted for P_{OUT}=33dBm
Peak Supply Current, 33.0dBm	-	1389	1619	mA	
Harmonic Peak, 2fo	-	-40	-33	dBm	
Harmonic Peak, 3fo	-	-40	-33	dBm	
Harmonic Peak, 4fo to 12.75GHz	-	-40	-33	dBm	
RF Leakage, Any TRX Port	-	-10	1.5	dBm	
Non-harmonic Spurious up to 12.75GHz	-	-40	-36	dBm	5dBm ≤ P_{OUT} ≤ 33dBm
Forward Isolation, OFF	-	-70	-41	dBm	CTL0=Low; P_{IN} ≤ 6dBm; VRAMP=0.25V
Forward Isolation, TX_LB	-	-26	-17	dBm	CTL0=High; P_{IN} ≤ 6dBm; VRAMP=0.25V
Noise Power 728MHz to 763MHz	-	-85	-82	dBm	VRAMP adjusted for P_{OUT}=33dBm; RBW=100kHz
Noise Power 869MHz to 894MHz	-	-83	-81	dBm	
Noise Power 1930MHz to 1990MHz	-	-	-77	dBm	
Stability (Spurious), VSWR 10:1	-	-	-36	dBm	VSWR=10:1; 0° ≤ Phase ≤ 360°; (VRAMP adjusted for P_{OUT}=33dBm into 50Ω load); RBW=3MHz
Ruggedness, VSWR 20:1	No damage or permanent degradation to device				VSWR=20:1; 0° ≤ Phase ≤ 360°; (VRAMP adjusted for P_{OUT}=33dBm into 50Ω load); RBW=3MHz ; 3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Transmit, 900 Band					**Nominal test conditions unless otherwise stated. All unused ports terminated in 50Ω. VBAT=3.5V; P_{IN}=3dBm; T_A=+25°C; VRAMP=1.6V; Duty Cycle=25%; Period=4.6ms; Logic State=TX_LB**
Frequency	880	-	915	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR	-	-	2.5	X:1	5dBm ≤ P_{OUT} ≤ 33dBm
RF Output Power (P_{OUT}), Maximum	33.3	34.3	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	31	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
RF Output Power (P_{OUT}), EDGE	27	-	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	25	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
Efficiency (PAE), 33.0dBm	39	43	-	%	VRAMP adjusted for P_{OUT}=33dBm
Peak Supply Current, 33.0dBm	-	1324	1494	mA	
Harmonic Peak, 2fo	-	-40	-33	dBm	
Harmonic Peak, 3fo	-	-40	-33	dBm	
Harmonic Peak, 4fo to 12.75GHz	-	-40	-33	dBm	
RF Leakage, Any TRX Port	-	-10	1.5	dBm	
Non-harmonic Spurious up to 12.75GHz	-	-40	-36	dBm	5dBm ≤ P_{OUT} ≤ 33dBm
Forward Isolation, OFF	-	-73	-41	dBm	CTL0=Low; P_{IN} ≤ 6dBm; VRAMP=0.25V
Forward Isolation, TX_LB	-	-26	-17	dBm	CTL0=High; P_{IN} ≤ 6dBm; VRAMP=0.25V
Noise Power 925MHz to 935MHz	-	-81	-77	dBm	VRAMP adjusted for P_{OUT}=33dBm; RBW=100kHz
Noise Power 935MHz to 960MHz	-	-87	-83	dBm	
Noise Power 1805MHz to 1880MHz	-	-	-77	dBm	
Stability (Spurious), VSWR 10:1	-	-	-36	dBm	VSWR=10:1; 0° ≤ Phase ≤ 360°; (VRAMP adjusted for P_{OUT}=33dBm into 50Ω load); RBW=3MHz
Ruggedness, VSWR 20:1	No damage or permanent degradation to device				VSWR=20:1; 0° ≤ Phase ≤ 360°; (VRAMP adjusted for P_{OUT}=33dBm into 50Ω load); RBW=3MHz ; 3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Transmit, DCS Band					**Nominal test conditions unless otherwise stated. All unused ports terminated in 50Ω. VBAT=3.5V; P_{IN}=3dBm; T_A=+25°C; VRAMP=1.6V; Duty Cycle=25%; Period=4.6ms; Logic State=TX_HB**
Frequency	1710	-	1785	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR	-	-	2.5	X:1	0dBm ≤ P_{OUT} ≤ 30dBm
RF Output Power (P_{OUT}), Maximum	30.5	31.7	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	28.5	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
RF Output Power (P_{OUT}), EDGE	26	-	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	24	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
Efficiency (PAE), 30.0dBm	30	32	-	%	VRAMP adjusted for P_{OUT}=30dBm
Peak Supply Current, 30.0dBm	-	891	973	mA	
Harmonic Peak, 2fo	-	-40	-33	dBm	
Harmonic Peak, 3fo	-	-40	-33	dBm	
Harmonic Peak, 4fo to 12.75GHz	-	-40	-33	dBm	
RF Leakage, to Any TRX Port	-	-3	1.5	dBm	
Non-harmonic Spurious up to 12.75GHz	-	-40	-36	dBm	0dBm ≤ P_{OUT} ≤ 30dBm
Forward Isolation, OFF	-	-64	-53	dBm	CTL0=Low; P_{IN} ≤ 6dBm; VRAMP=0.25V
Forward Isolation, TX_HB	-	-30	-15	dBm	CTL0=High; P_{IN} ≤ 6dBm; VRAMP=0.25V
Noise Power 925MHz to 960MHz	-	-91	-81	dBm	VRAMP adjusted for P_{OUT}=30dBm; RBW=100kHz
Noise Power 1805MHz to 1880MHz	-	-88	-77	dBm	
Stability (Spurious), VSWR 12:1	-	-	-36	dBm	VSWR=12:1; 0° ≤ Phase ≤ 360°; (VRAMP adjusted for P_{OUT}=30dBm into 50Ω load); RBW=3MHz
Ruggedness, VSWR 20:1	No damage or permanent degradation to device				VSWR=20:1; 0° ≤ Phase ≤ 360°; (VRAMP adjusted for P_{OUT}=30dBm into 50Ω load); RBW=3MHz ; 3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Transmit, PCS Band					**Nominal test conditions unless otherwise stated. All unused ports terminated in 50Ω. VBAT=3.5V; P_{IN}=3dBm; T_A=+25°C; VRAMP=1.6V; Duty Cycle=25%; Period=4.6ms; Logic State=TX_HB**
Frequency	1880	-	1910	MHz	
Input Power (P_{IN})	0	3	6	dBm	
Input VSWR	-	-	2.5	X:1	0dBm ≤ P_{OUT} ≤ 30dBm
RF Output Power (P_{OUT}), Maximum	30.5	31.7	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	28.5	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
RF Output Power (P_{OUT}), EDGE	26	-	-	dBm	0dBm ≤ P_{IN} ≤ 6dBm
	24	-	-	dBm	3.2V ≤ VBAT ≤ 4.5V; -20°C ≤ T_A ≤ 85°C; 0dBm ≤ P_{IN} ≤ 6dBm
Efficiency (PAE), 30.0dBm	30	34	-	%	VRAMP adjusted for P_{OUT}=30dBm
Peak Supply Current, 30.0dBm	-	839	973	mA	
Harmonic Peak, 2fo	-	-40	-33	dBm	
Harmonic Peak, 3fo	-	-40	-33	dBm	
Harmonic Peak, 4fo to 12.75GHz	-	-40	-33	dBm	
RF Leakage, Any TRX port	-	-1	1.5	dBm	
Non-harmonic Spurious up to 12.75GHz	-	-40	-36	dBm	0dBm ≤ P_{OUT} ≤ 30dBm
Forward Isolation, OFF	-	-64	-53	dBm	CTL0=Low; P_{IN} ≤ 6dBm; VRAMP=0.25V
Forward Isolation, TX_HB	-	-30	-15	dBm	CTL0=High; P_{IN} ≤ 6dBm; VRAMP=0.25V
Noise Power 728MHz to 763MHz	-	-95	-81	dBm	VRAMP adjusted for P_{OUT}=30dBm; RBW=100kHz
Noise Power 869MHz to 894MHz	-	-96	-81	dBm	
Noise Power 1930MHz to 1990MHz	-	-88	-77	dBm	
Stability (Spurious), VSWR 10:1	-	-	-36	dBm	VSWR=12:1; 0° ≤ Phase ≤ 360°; (VRAMP adjusted for P_{OUT}=30dBm into 50Ω load); RBW=3MHz
Ruggedness, VSWR 20:1	No damage or permanent degradation to device				VSWR=20:1, all phase angles, (VRAMP adjusted for P_{OUT}=30dBm into 50Ω load), VSW=5.0V, VCC=3.2V to 4.5V, P_{IN}=0dBm to 6dBm, T_A=30°C to +85°C

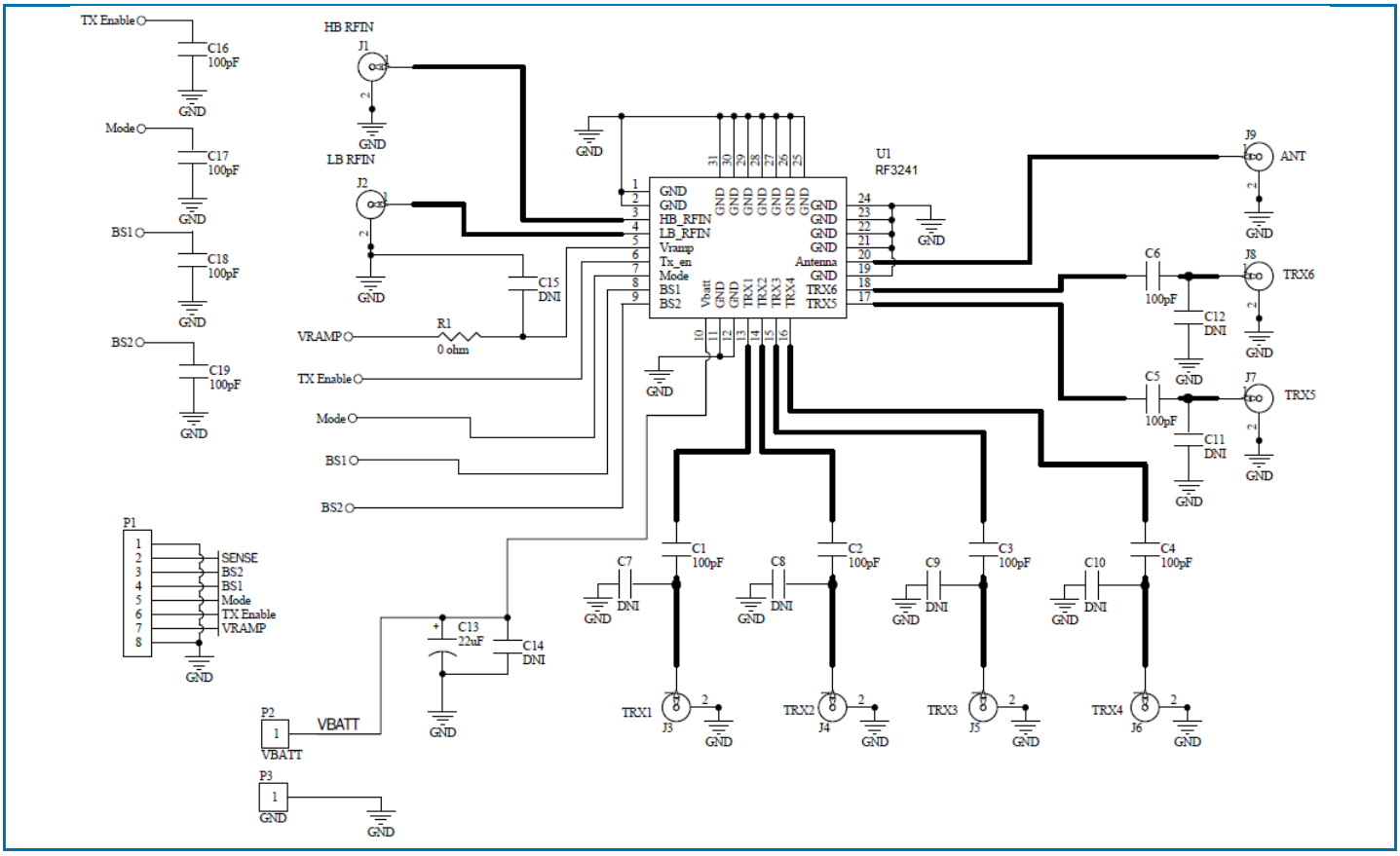
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
RF Switch, Low Bands					**Nominal test conditions unless otherwise stated. All unused ports terminated in 50Ω. Logic State given in condition. VBAT=3.5V; P_{IN}=-6dBm; T_A=+25°C; Duty Cycle=100%; VRAMP≤0.3V**
Frequency	824	-	960	MHz	
Insertion Loss, TRXn - ANT	-	0.6	1.0	dB	Logic State=TRX1, TRX2, TRX3, TRX4, TRX5, TRX6
Input VSWR, TRXn - ANT	1.0	-	1.5	X:1	Logic State=TRX1, TRX2, TRX3, TRX4, TRX5, TRX6
Isolation, TRX1 – Any TRX Port	25	35	-	dB	Logic State=TRX1
Isolation, TRX2 – Any TRX Port	25	34	-	dB	Logic State=TRX2
Isolation, TRX3 – Any TRX Port	25	34	-	dB	Logic State=TRX3
Isolation, TRX4 – Any TRX Port	25	33	-	dB	Logic State=TRX4
Isolation, TRX5 – Any TRX Port	25	33	-	dB	Logic State=TRX5
Isolation, TRX6 – Any TRX Port	25	35	-	dB	Logic State=TRX6
IMD2, Any TRX Port	-	-108	-102	dBm	IMD TX Signal Freq = 836.5, 897MHz; IMD TX Signal Power = 20dBm; IMD Blocker Freq = 45MHz; IMD Blocker Power = -15dBm; IMD Measured Freq = 881.5, 942MHz
IMD2, Any TRX Port	-	-124	-105	dBm	IMD TX Signal Freq = 836.5, 897MHz; IMD TX Signal Power = 20dBm; IMD Blocker Freq = 1718, 1839MHz; IMD Blocker Power = -15dBm; IMD Measured Freq = 881.5, 942MHz
IMD3, Any TRX Port	-	-118	-105	dBm	IMD TX Signal Freq = 836.5, 897MHz; IMD TX Signal Power = 20dBm; IMD Blocker Freq = 791.5, 852MHz; IMD Blocker Power = -15dBm; IMD Measured Freq = 881.5, 942MHz
Harmonic, 2fo	-	-100	-76	dBc	Logic State=TRX1, TRX2, TRX3, TRX4, TRX5, TRX6; Input Power=28dBm; Freq=824, 849, 880, 915MHz
Harmonic, 3fo	-	-83	-76	dBc	
Harmonics, 4fo to 12.75GHz	-	-103	-76	dBc	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
RF Switch, High Bands					**Nominal test conditions unless otherwise stated. All unused ports terminated in 50Ω. Logic State given in condition. VBAT=3.5V; P_{IN}=-6dBm; T_A=+25°C; Duty Cycle=100%; VRAMP≤0.3V**
Frequency	1710		2170	MHz	
Insertion Loss, TRXn - ANT	-	0.9	1.2	dB	Logic State=TRX1, TRX2, TRX3, TRX4, TRX5, TRX6
Input VSWR, TRXn - ANT	1.0	-	1.5	X:1	Logic State=TRX1, TRX2, TRX3, TRX4, TRX5, TRX6
Isolation, TRX1 – Any TRX Port	25	28	-	dB	Logic State=TRX1
Isolation, TRX2 – Any TRX Port	25	28	-	dB	Logic State=TRX2
Isolation, TRX3 – Any TRX Port	25	28	-	dB	Logic State=TRX3
Isolation, TRX4 – Any TRX Port	20	25	-	dB	Logic State=TRX4
Isolation, TRX5 – Any TRX Port	25	27	-	dB	Logic State=TRX5
Isolation, TRX6 – Any TRX Port	25	28	-	dB	Logic State=TRX6
IMD2, Any TRX Port	-	-114	-105	dBm	IMD TX Signal Freq = 1747, 1880MHz; IMD TX Signal Power = 20dBm; IMD Blocker Freq = 95, 3589, 80, 3840MHz; IMD Blocker Power = -15dBm; IMD Measured Freq = 1842, 1960MHz
IMD3, Any TRX Port	-	-118	-105	dBm	IMD TX Signal Freq = 1747, 1880MHz; IMD TX Signal Power = 20dBm; IMD Blocker Freq = 1652, 1800MHz; IMD Blocker Power = -15dBm ; IMD Measured Freq = 1842, 1960MHz
Harmonic, 2fo	-	-100	-76	dBc	Logic State=TRX1, TRX2, TRX3, TRX4, TRX5, TRX6; Input Power=28dBm; Freq=1710, 1785, 1850, 1910, 1920, 1980MHz
Harmonic, 3fo	-	-92	-76	dBc	
Harmonics, 4fo to 12.75GHz	-	-103	-76	dBc	

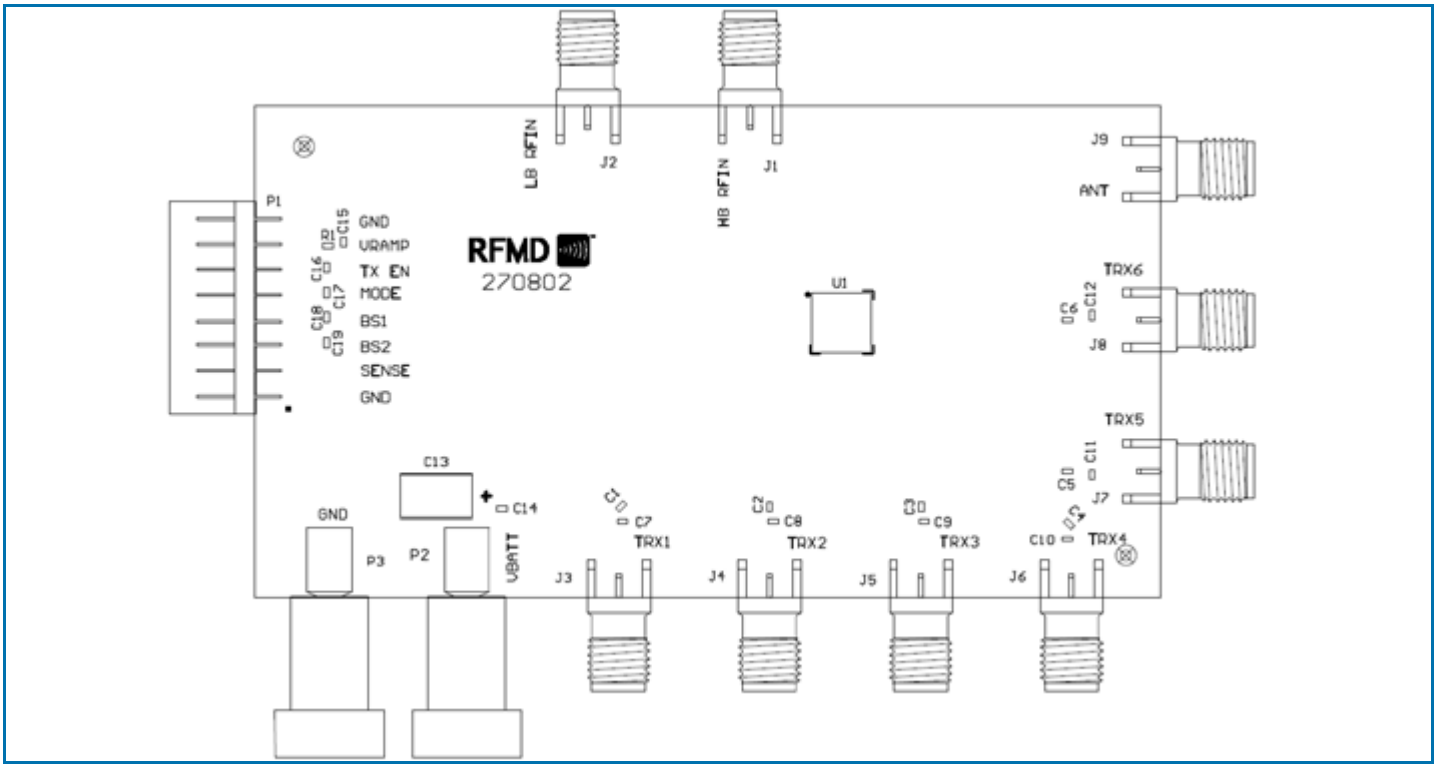
Module Control Logic

Logic State	Description	VRAMP	CTL0 (TXEN)	CTL1 (MODE)	CTL2 (BS1)	CTL3 (BS2)
Off	All circuits off (standby)	X	0	0	0	0
TRX1	TRX1 to ANT path is active. Power amplifier is off.	X	0	1	0	1
TRX2	TRX2 to ANT path is active. Power amplifier is off.	X	0	0	1	0
TRX3	TRX3 to ANT path is active. Power amplifier is off.	X	0	0	0	1
TRX4	TRX4 to ANT path is active. Power amplifier is off.	X	0	0	1	1
TRX5	TRX5 to ANT path is active. Power amplifier is off.	X	0	1	1	0
TRX6	TRX6 to ANT path is active. Power amplifier is off.	X	0	1	0	0
TX_LB	Low Band power amplifier active	0.2 to 1.6V	1	0	1	0
TX_HB	High Band power amplifier active	0.2 to 1.6V	1	0	0	1

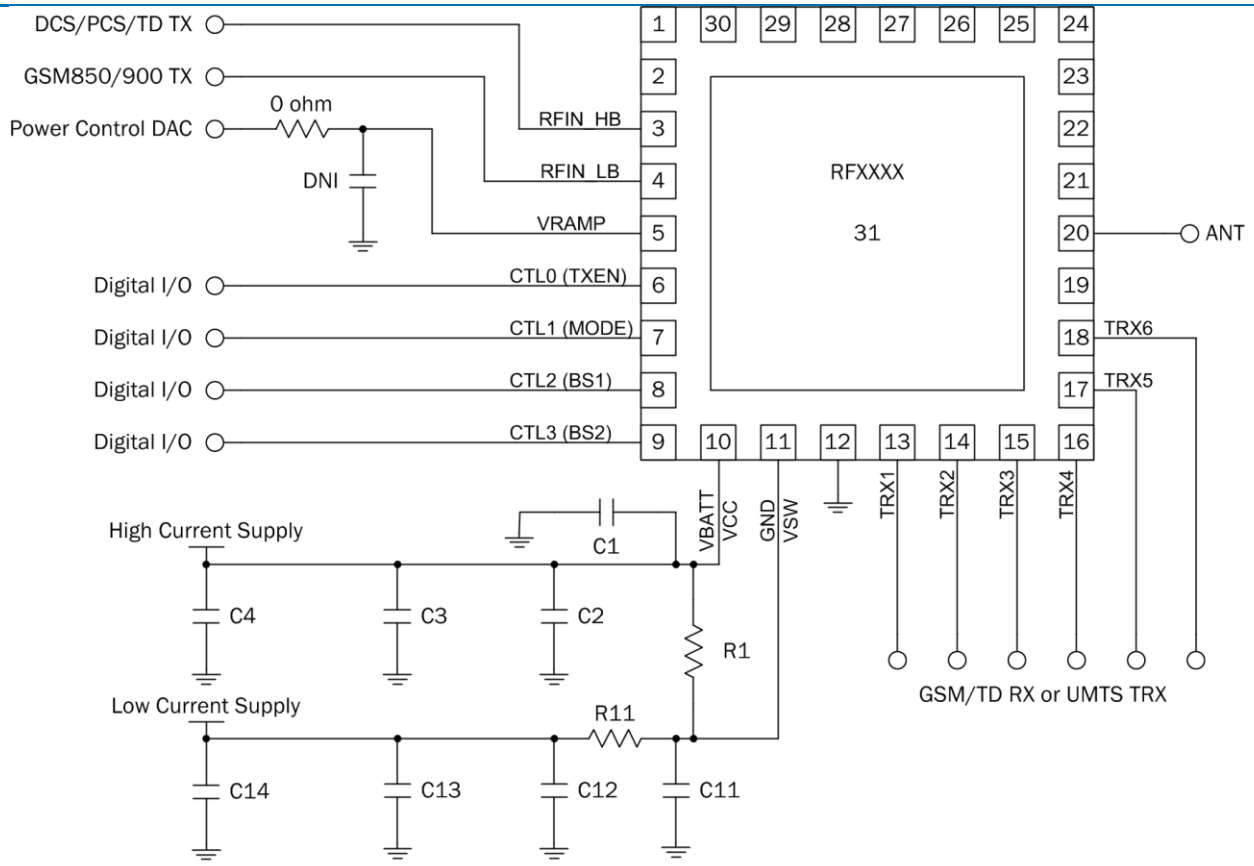
Evaluation Board Schematic



Evaluation Board Assembly Drawing



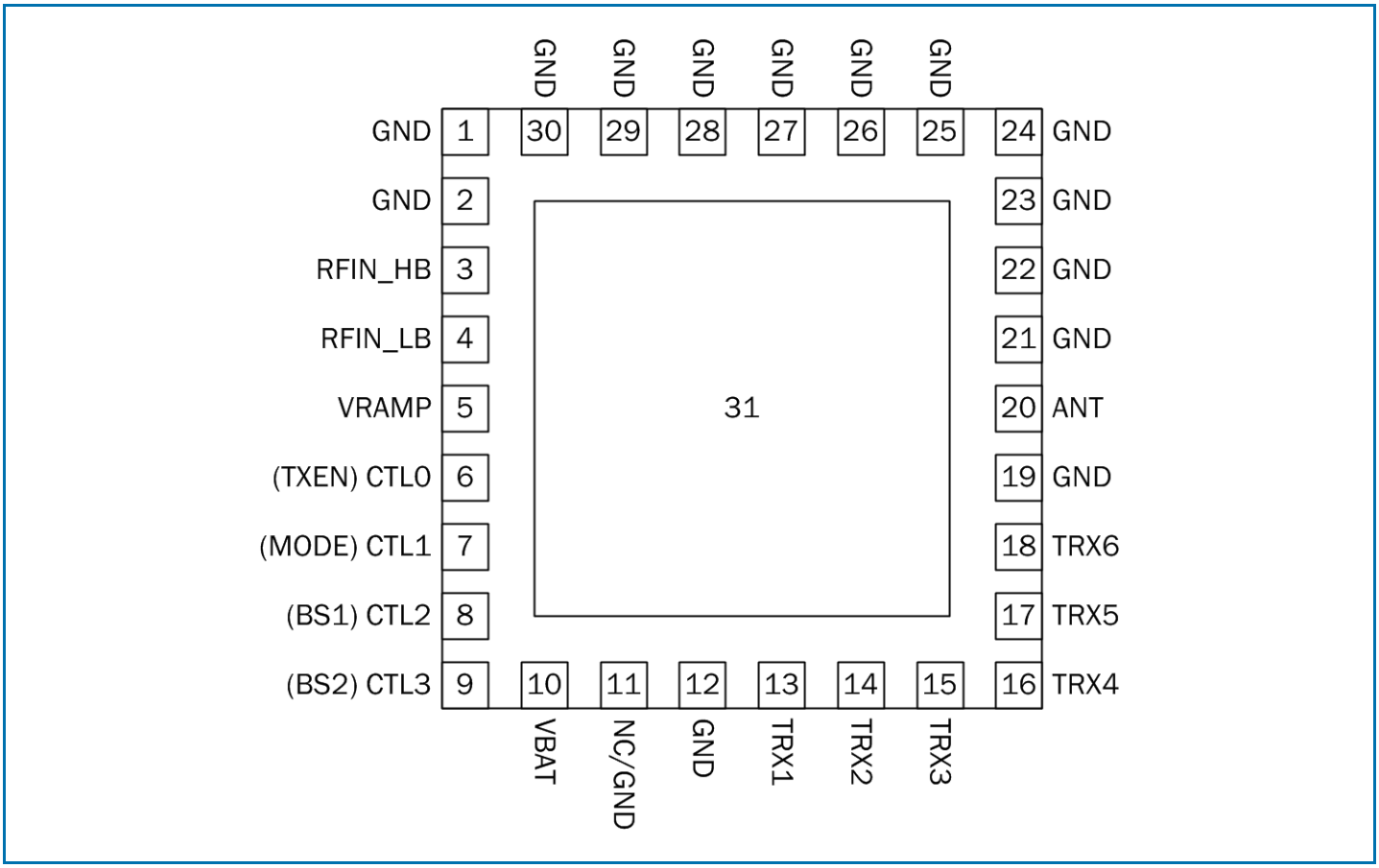
Application Schematic



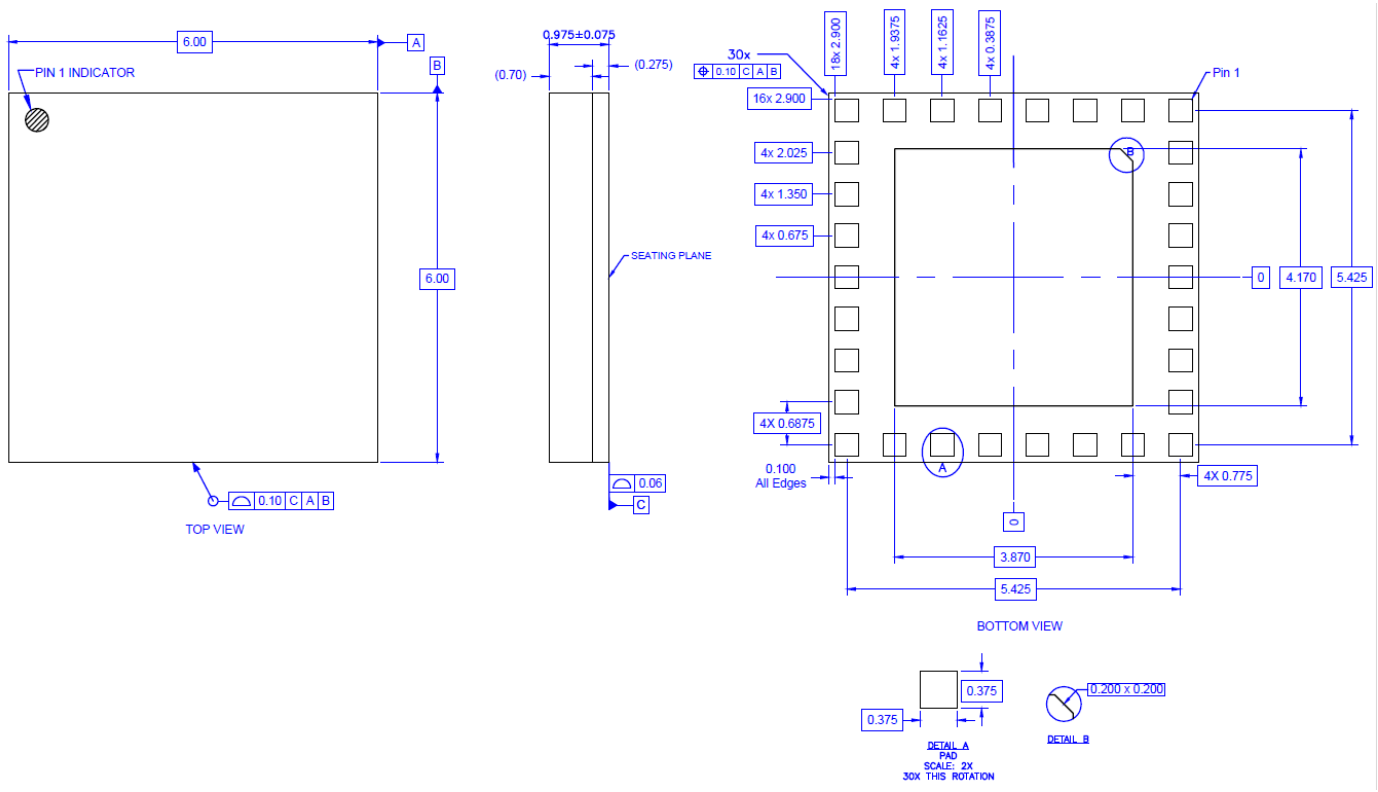
Notes:
- Suggested decoupling values. Actual requirements may vary with application.
- All RF paths should be designed as 50 ohm microstrip or stripline.
- TRX1 – TRX6 not supported on all pin compatible products
- TD not supported on all pin compatible products

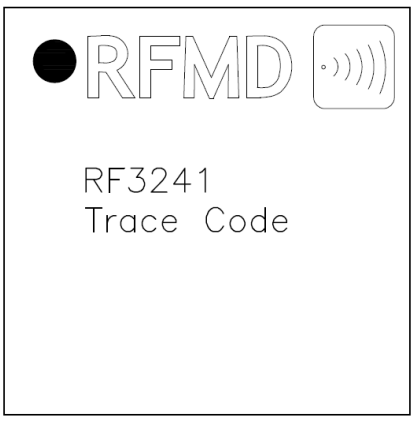
Application/ Product(s)	R1	R11	C1	C2	C3	C4	C11	C12	C13	C14
Single Supply/ RF3235, RF3236, RF3237, RF3239, RF3241	DNP	DNP	pF	nF	uF	uF	0Ω	DNP	DNP	DNP
Single Supply/ RF3240, RF3246, RF9820, RF9818	0Ω	DNP	pF	nF	uF	uF	DNP	DNP	DNP	DNP
Two Supply/ RF3240, RF3246, RF9820, RF9818	DNP	0Ω	pF	nF	uF	uF	pF	nF	uF	uF

Pin Out



Package Outline and Branding Drawing (Dimensions in millimeters)



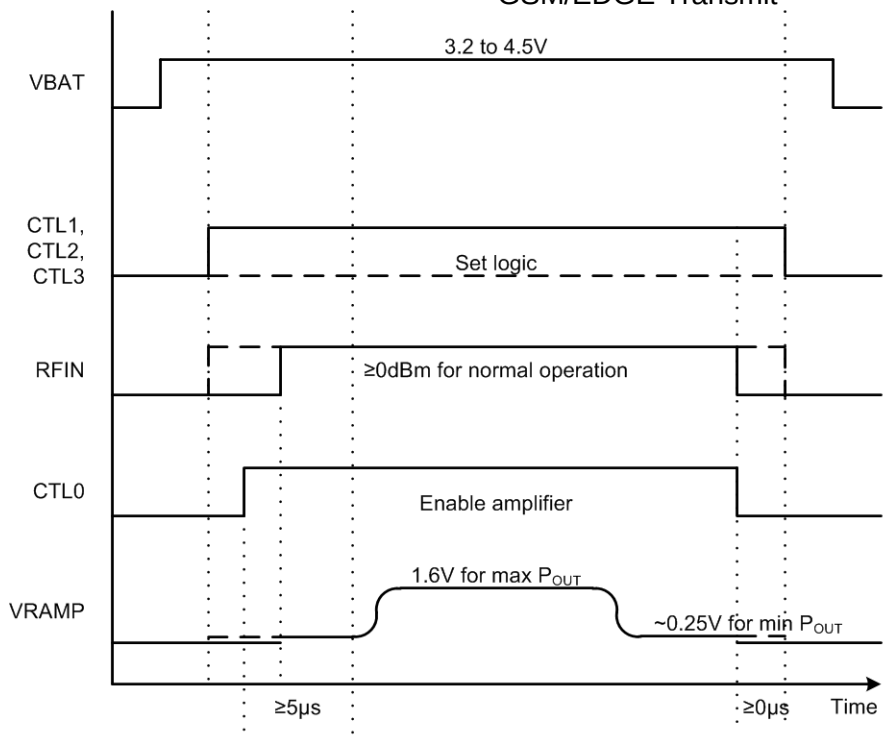


Dot indicates Pin 1

Pin Names and Descriptions

Pin	Name	Description
1	GND	Pin connected to module ground.
2	GND	Pin connected to module ground.
3	RFIN_HB	RF input to the high band power amplifier. This is a 50Ω input.
4	RFIN_LB	RF input to the low band power amplifier. This is a 50Ω input.
5	VRAMP	Power control signal from transceiver. Board routing to this high impedance, high bandwidth power control input must avoid coupling to noise sources. Stray signals coupled to this input may cause modulation spectrum degradation.
6	CTL0	Logic control signal. See Module Control Logic table.
7	CTL1	Logic control signal. See Module Control Logic table.
8	CTL2	Logic control signal. See Module Control Logic table.
9	CTL3	Logic control signal. See Module Control Logic table.
10	VBAT	DC power supply for the module. Traces running to this pin will have high current pulses during transmit operation. Proper decoupling and routing to handle this condition should be observed.
11	NC/GND	Pin connected to module ground. Board routing can leave this pin unconnected for compatibility reasons.
12	GND	Pin connected to module ground.
13	TRX1	Interchangeable GSM/EDGE/UMTS port. External circuitry must maintain zero volts on this port.
14	TRX2	Interchangeable GSM/EDGE/UMTS port. External circuitry must maintain zero volts on this port.
15	TRX3	Interchangeable GSM/EDGE/UMTS port. External circuitry must maintain zero volts on this port.
16	TRX4	Interchangeable GSM/EDGE/UMTS port. External circuitry must maintain zero volts on this port.
17	TRX5	Interchangeable GSM/EDGE/UMTS port. External circuitry must maintain zero volts on this port.
18	TRX6	Interchangeable GSM/EDGE/UMTS port. External circuitry must maintain zero volts on this port.
19	GND	Pin connected to module ground.
20	ANT	Bidirectional RF port. This is the common port of the antenna switch. An inductor makes this port appear as a DC short to ground.
21	GND	Pin connected to module ground.
22	GND	Pin connected to module ground.
23	GND	Pin connected to module ground.
24	GND	Pin connected to module ground.
25	GND	Pin connected to module ground.
26	GND	Pin connected to module ground.
27	GND	Pin connected to module ground.
28	GND	Pin connected to module ground.
29	GND	Pin connected to module ground.
30	GND	Pin connected to module ground.
31	GND	Main thermal ground. Board must provide a solid heat sink area under this pad. Thermal vias are required to disperse heat generated in the module into the main board or module performance will degrade.

Timing Diagram



Power On Sequence:

1. Apply VBAT
2. Apply CTL1, CTL2, CTL3
3. Apply RFIN
4. Apply VRAMP pedestal value (~0.25V)
5. Apply CTL0
6. Increase VRAMP for desired output power

Steps 3, 4, and 5 can occur at the same time.

RFIN can be applied at any time without damage. For good transient response, RFIN should be applied at least 2 microseconds before power ramp begins.

The Power Down Sequence is the reverse order of the Power On Sequence.

Revision History

Revision	Description
DS20140303	Release
DS20160209	Correction to Logic table - values in CTL2, CTL3 columns were swapped.