AWR

A National Instruments Company™

Analog Office®

HIGH-FREQUENCY DESIGN SOFTWARE FOR ANALOG AND RFICS

www.awrcorp.com

Advancing the Design of RFICs

INTRODUCTION

Analog Office® offers designers of RFICs and analog ICs an ease-to-use, flexible, accurate design environment within a single, integrated solution. The unique architecture of Analog Office software lets you control and seamlessly integrate best-in-class tools to capture, synthesize, simulate, optimize, layout, extract, and verify RFIC and analog designs from the system level through final tape-out. Analog Office streamlines designs, increases your productivity, and lets you get products to market faster.

YOUR PRODUCTIVITY MATTERS

A Familiar Look'n'Feel – Zero Learning Curve: Since AWR was founded in 1994, our mission has been simple: to improve design productivity with a superior use-model that cuts complex tasks down to size. Whether you're just learning the software or embracing a new capability, every facet of Analog Office software is so well integrated that it's easy to forget the exceptionally powerful solvers and technology working behind the scenes.

Synchronized Data from Beginning to End: The Unified Data Model™ (UDM) is the basis of the AWR Design Environment™. This single, object-oriented database is synchronized at its core, not through multiple layers of software and translators. So whether you're driving the design from the schematic, simulation, or layout, the Analog Office design environment lets you take your ideas from concept through simulation and directly to fabrication - all in one platform.

Breadth of Solvers – Plug & Play: Only the AWR design environment lets you easily integrate software from third-party vendors like Synopsys' HSPICE into your design to enable you to choose the best tool for the task. Analog Office software also lets you export design layouts to an OpenAccess-based database so you can use the same libraries across a range of design tools from OpenAccess-based tool vendors. The result: big time savings to get your product through development faster.

ANALOG OFFICE TOOLS, TECHNOLOGY & INNOVATIONS

Circuit Simulation Technology:

APLAC® "Battle tested" and foundry-proven in the design of Nokia® mobile phones for more than a decade, powerful APLAC engines deliver efficient harmonic balance and time-domain simulators specifically tailored for large-scale and extremely nonlinear RFIC designs. APLAC harmonic balance simulation is enhanced further by our patented Multi-Rate Harmonic Balance (MRHB™) technology for even more complex designs.

HSPICE Directly import HSPICE-formatted encrypted netlists into Analog Office software for immediate simulation/co-simulation within the AWR environment, allowing you to bring in legacy designs from your own firm, other design groups, or even outside companies.

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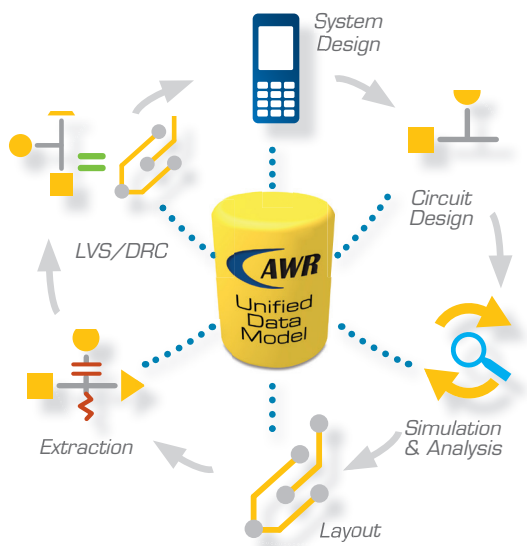
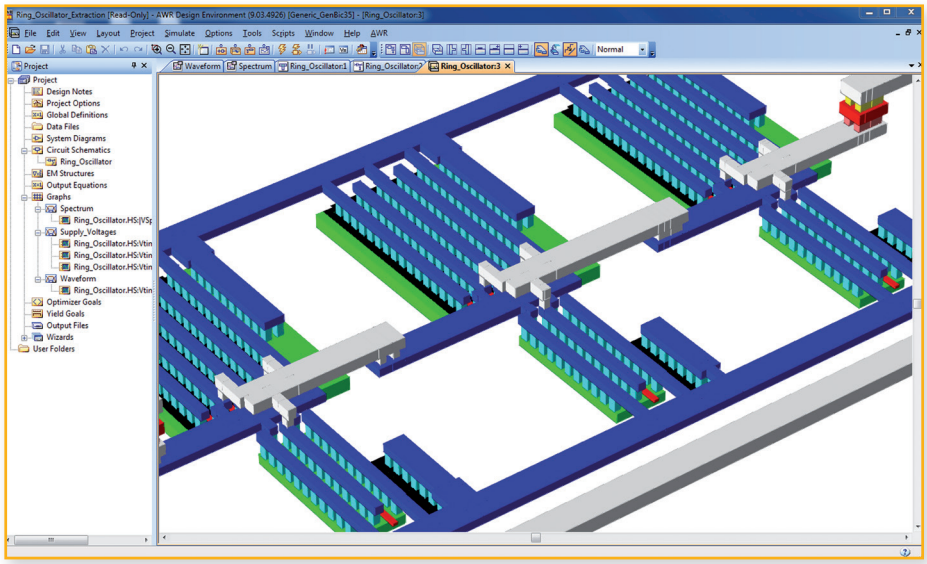
"A key aim is to develop highly accurate models for transistors and passives such as spiral inductors at frequencies up to 40 GHz. Analog Office software enables us to accurately model active devices, passives, and interconnects on SoS so that our customers realize first-time-right designs."

Yash Moghe
Design Engineering Manager
Silanna



Analog Office software is a complete design environment offering all of the essential technologies: linear and nonlinear circuit simulators, EM analysis tools, layout-vs.-schematic checks, statistical design capabilities, and parametric cell libraries.



Ring oscillator layout in Analog Office.

Electromagnetic Technology:

Automatic Circuit Extraction (ACE™) Using layout-based models for circuit extraction, ACE dramatically reduces the time required to initially model complex interconnects by automatically identifying transmission lines from the layout and partitioning them into existing models.

AXIEM® Tailored for 3D high-frequency planar passives like spiral inductors, AXIEM delivers exceptionally accurate EM simulation that's fast and efficient for even the most complex designs.

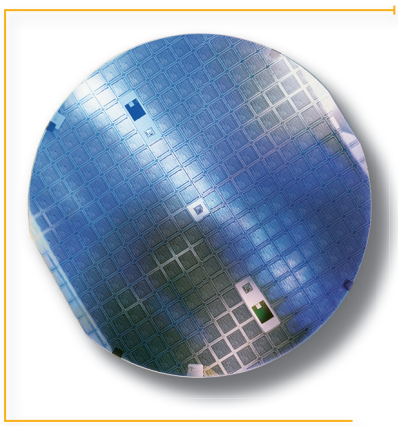
Analyst™ For 3D on-chip interconnects like tapered vias, air-bridges, and finite dielectric/sidewalls, Analyst is only one click away from precise 3D finite element EM analysis.

EM Socket™ Integrate specialized "silicon-wise" third-party EM point tools from OEA into the design environment without leaving Analog Office.

Automation Technology:

Intelligent Net (iNet™) Automatically tailors timing-driven and wire-driven digital design to high-frequency design.

DRC/LVS Access signed-off/approved links to EDA vendors from within Analog Office software. This gives you access to multiple sign-off verification flows, including PowerDRC/LVS, Mentor Graphics Calibre®, Cadence Assura, and even open-source ICED.



FEATURES AT A GLANCE

- Transient/time-domain, AC and noise analysis using HSPICE and APLAC
- APLAC high-performance harmonic balance and transient solver technologies, including transient-assisted harmonic balance, multi-rate harmonic balance, and transient/time-domain (optional)
- iNet interconnect extraction technology
- ACE automatic circuit extraction technology for interconnect modeling
- AXIEM planar 3D EM analysis of on-chip passives (optional)
- Analyst 3D FEM EM analysis for 3D on-chip interconnects (optional)
- OEA International NET-AN for 3D RLCK extraction
- EM Socket interface for integration with third-party EM tools
- DRC/LVS support for tools such as PowerDRC/LVS, Calibre, Assura, and ICED
- Seamless integration with AWR's Visual System Simulator™ software for system co-simulation

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CAPABILITIES

- Linear and nonlinear circuit simulation
- Layout with parasitic extraction
- EM analysis
- Co-simulation with system tools
- Statistical design and design centering
- Links to back-end DRC/LVS

APPLICATIONS

- RFIC
- Analog IC

Advancing the wireless revolution®

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