VFVX321
VCXO Ultra Low Jitter 2.5V, 3.3V
5x7mm SMD, LVPECL / LVDS / LVCMOS

CTS ELECTRONIC COMPONENTS

Features

- 60MHz to 800MHz* frequency range
- Differential output levels (LVPECL/LVDS)
- Single ended LVCMOS output available
- <0.2ps RMS jitter over 12kHz to 20MHz
- Selectable OE logic

RoHS Status

RoHS 6/6

Applications

- Optical Networking, SONET / SDH
- 10 Gigabit Ethernet
- Broadband Access

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Frequency Range	F		60 60 60		800* 320 250	MHz	PECL LVDS CMOS
Frequency Stability	ΔF/F	Vs. Operating temperature			± 50 ± 25 ± 20	ppm	*Order Code B* *Order Code C* *Order Code D*
		Vs. Supply voltage		± 3		ppm/V	
		Vs. Aging / Year		± 3 ±1		ppm ppm	First Year After first year
Operating Temperature	T		0° -40°		+70° +85°	°C	*Order Code B* *Order Code G*
Output		LVPECL LVDS LVCMOS					*Order Code L* *Order Code D* *Order Code C*
Supply Voltage	V_{CC}		3.15 2.25	3.3 2.5	3.45 2.75	V	*Order Code E* *Order Code G*
Period RMS Jitter		155.52MHz 311.04MHz 622.08MHz		2.5 2.8 4	3 3.3 6	ps	
Integrated RMS Jitter **12kHz to 20MHz**		155.52MHz 311.04MHz 622.08MHz		0.25 0.18 0.09		ps	

* NOTE: Certain frequencies above 300MHz ($2.5V_{DD}$) are not available.
Consult factory for availability.

Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Supply Current	I_{CC}	38 – 100MHz 100 – 300MHz 300 – 640MHz			65 80 90	mA	PECL
		38 – 100MHz 100 – 320MHz			45 60	mA	LVDS
		At 100MHz, load = 15pF		16	20	mA	CMOS
Load	50 Ohms to V_{DD}-2V (PECL) 100 Ohms (LVDS)						
Output High Voltage	V_{OH}	R_L = 50 Ohms to (V_{DD}-2V) I_{OH} = -8.5mA	2.4	V_{DD}-1.025 1.4	1.6	V	PECL LVDS CMOS
Output Low Voltage	V_{OL}	I_{OL} = -8.5mA	0.9	1.1	V_{DD}-1.620 0.4	V	PECL LVDS CMOS
Output Differential Voltage	V_{OD}		247	355	454	mV	LVDS
Output Drive Current	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V		8.5		mA	CMOS
Offset Voltage	V_{OS}		1.125	1.2	1.375	V	LVDS
Rise / Fall Time	T_R/T_F	20% to 80%		0.25 0.5 1.2	0.45 0.7 1.6	ns	PECL LVDS CMOS
Duty Cycle		V_{DD} – 1.3V @ 1.25V 50% V_{DD}	45	50	55	%	PECL LVDS CMOS
Modulation Bandwidth		0V < V_C <3.3V; -3dB	16			kHz	
V_C Input Impedance			130			kΩ	
Linearity				5	10	%	
APR*		3.3V V_{DD} / V_C 1.65V ± 1.65V	±100 ±75 ±50	±120 ±100 ±75		ppm	60 ≤ 150MHz 151 ≥ 399MHz 400 – 800MHz
		2.5V V_{DD} / V_C 1.25V ± 1.25V	±100 ±75 ±50	±120 ±90 ±65		ppm	60 – 130MHz 131 – 200MHz 200 – 400MHz
Stabilization Time		From valid power			10	ms	
Tristate	"1": Output Enable – Pin 2 may float or 2.8V min (3.3V V_{DD}) or 2.25V min (2.5V V_{DD}) "0": Tristate – Pin 2 requires 0.4V max (3.3V or 2.5V V_{DD})						

*Consult factory for wider pull availability

Phase Noise Performance

Parameter	Output Type	Frequency Range (MHz)	Carrier Freq. (MHz)	10Hz	100Hz	1kHz	10 kHz	100 kHz	1 MHz	10 MHz
Phase Noise (dBc/Hz)	PECL	400 - 800	622.08	-49	-85	-110	-130	-137	-148	-150
	CMOS	120 – 250	155.52	-50	-82	-110	-128	-142	-148	-150
	PECL LVDS	120 – 320	155.52	-50	-82	-110	-128	-142	-148	-150
	CMOS	60 – 160	155.52	-65	-95	-122	-138	-142	-148	-149
	PECL LVDS	60 – 160	155.52	-65	-95	-122	-138	-142	-148	-149

Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Lead Temperature		Soldering, 10s max			260	°C	
Storage Temperature	T_S		-55		+125°	°C	
Junction Temperature	T_J				+125°	°C	
ESD Protection		Input static discharge voltage protection			2	kV	
Supply Voltage	V_{DD}				4.6	V	
Output Voltage	V_O		GND -0.5		V_{DD}+0.5	V	
Input Voltage			GND -0.5		V_{DD}+0.5	V	

Environmental and Mechanical Conditions

Parameter	Condition
Shock	1000 Gs, 0.35ms, ½ sine wave, 3 shocks in each plane
Humidity	Resistant to 85% R.H. at 85 °C
Vibration	10-2000 Hz of 0.06" d.a. or 20 Gs, whichever is less
Leak	MIL STD 883, Method 1014, Condition A and Condition C
Case	Ceramic with hermetic resistance-welded metal lid
Pads	Solderable gold over nickel
Marking	Epoxy ink or laser engraved
Resistance to Solvents	MIL STD 202, Method 215

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Pin Assignments

LVPECL, LVDS

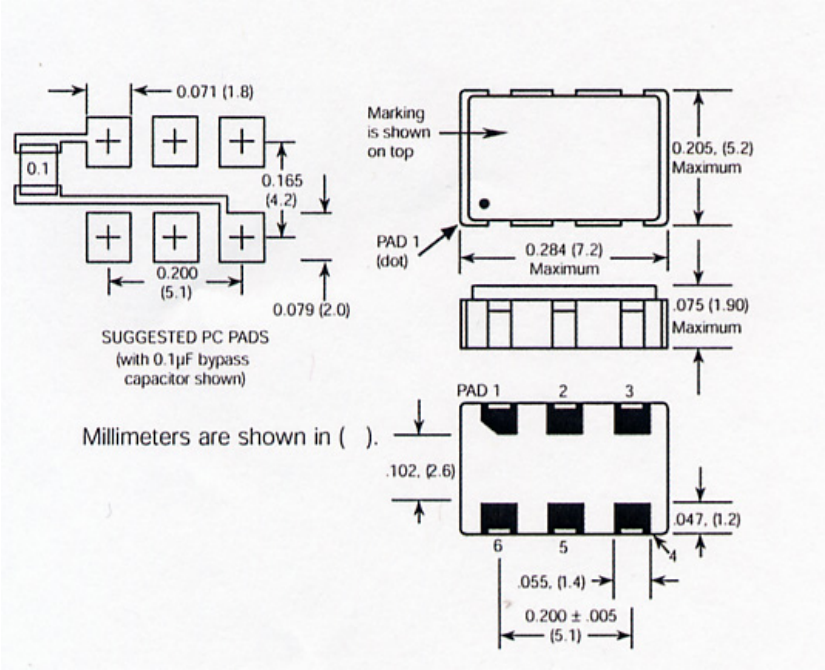
Pin #	Connection
1	V_C
2	Tristate
3	Case, GND
4	Output
5	$\overline{\text{Output}}$
6	Supply Voltage

LVCMOS

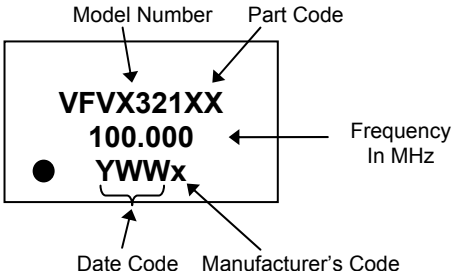
Pin #	Connection
1	V_C
2	Tristate
3	Case, GND
4	Output
5*	N/C
6	Supply Voltage

*For LVCMOS, Dual single ended outputs available – consult factory

Package



Marking Specification



How to Order

VFVX321 — □□□□ — FREQUENCY, MHz

Stability

Code	Specification
B	50 ppm
C	25 ppm
D	20 ppm

Temperature Range

Code	Specification
B	0°C to 70°C
G	-40°C to 85°C

Supply Voltage

Code	Specification
E	3.3V
G	2.5V

Output

Code	Output
L	LVPECL
D	LVDS
C	CMOS

Note: DG combination not available at all frequencies. Consult factory.