XP1035-QH

Power Amplifier
5.9 - 9.5 GHz

Rev. V1

Features

- 26 dB Small Signal Gain
- 39 dBm Third Order Intercept Point (OIP3)
- Integrated Power Detector
- Lead-Free 4 mm 24-lead QFN Package
- 100% RF Testing
- RoHS* Compliant and 260°C Reflow Compatible

Description

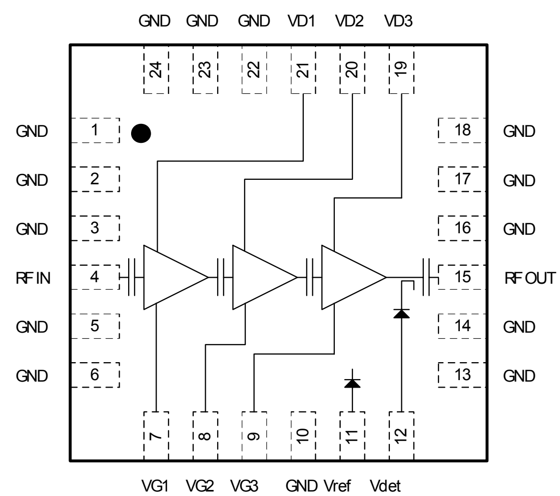
The XP1035-QH is a packaged linear power amplifier that operates over the 5.9-9.5 GHz frequency band. The device provides 26 dB gain and 39 dBm Output Third Order Intercept Point (OIP3) across the band and is offered in an industry standard, fully molded 4x4mm QFN package. The packaged amplifier is comprised of a three stage power amplifier with an integrated, temperature compensated on-chip power detector. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part. The device is manufactured in GaAs PHEMT device technology with BCB wafer coating to enhance ruggedness and repeatability of performance. The XP1035-QH is specifically designed for PtP radio applications and is well suited for other telecom applications such as SATCOM and VSAT.

Ordering Information [1]

Part Number	Package
XP1035-QH-0G00	bulk quantity
XP1035-QH-0G0T	tape and reel
XP1035-QH-EV1	evaluation module

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration [2]

Pin No.	Function	Pin No.	Function
1-3	Ground	12	Pwr Det
4	RF Input	13-14	Ground
5-6	Ground	15	RF Output
7	Gate 1 Bias	16-18	Ground
8	Gate 2 Bias	19	Drain 3 Bias
9	Gate 3 Bias	20	Drain 2 Bias
10	Ground	21	Drain 1 Bias
11	Pwr Det Ref.	22-24	Ground

2. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications: 5.9 - 9.5 GHz (Ambient Temperature T = 25°C)

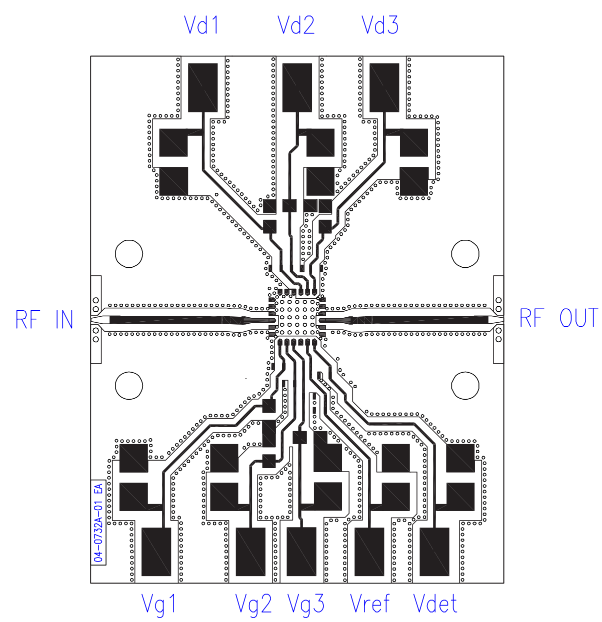
Parameter	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB	-	26	-
Input Return Loss (S11)	dB	-	13	-
Output Return Loss (S22)	dB	-	10	-
Reverse Isolation (S12)	dB	-	45	-
Psat	dBm	-	29	-
P1dB	dBm	-	27.5	-
OIP3	dBm	-	39	-
Drain Bias Voltage (Vd1,2,3)	VDC	-	6	-
Detector Bias Voltage (Vdet,ref)	VDC	-	5	-
Gate Bias Voltage (Vg1,2,3)	VDC	-2	-1	-
Supply Current (Id1)	mA	-	70	-
Supply Current (Id2)	mA	-	140	-
Supply Current (Id3)	mA	-	280	-

Absolute Maximum Ratings [3,4]

Parameter	Absolute Max.
Supply Voltage (Vd1,2,3)	+7.2 V
Supply Current (Id1,2,3)	600 mA
Gate Bias Voltage (Vg1,2,3)	-3 V
Max Power Dissipation (Pdiss)	4.2 W
RF Input Power	+15 dBm
Operating Temperature (Ta)	-55°C to +85°C
Storage Temperature (Tstg)	-65°C to +165°C
Channel Temperature (Tch)[2]	150°C
MSL Level (MSL)	MSL3

3. Operation of this device above any one of these parameters may cause permanent damage.
4. Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

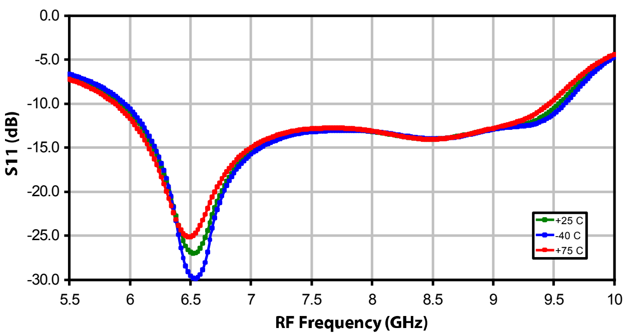
Recommended Layout



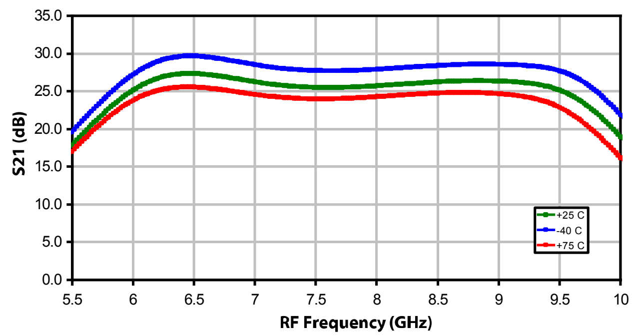
Recommended Decoupling Capacitors: 100pF 0402, 10µF 0805

Typical Performance Curves

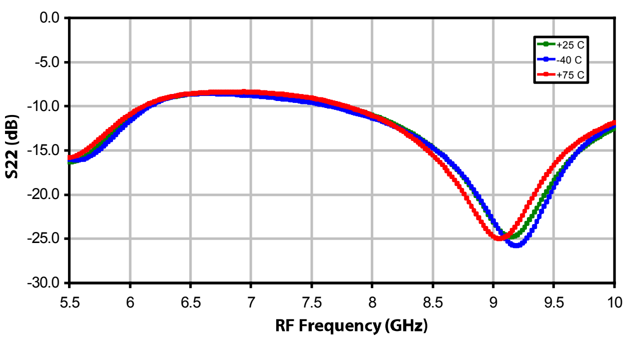
XP1035-QH: S11 (dB) at Vd=6V, Id=500mA



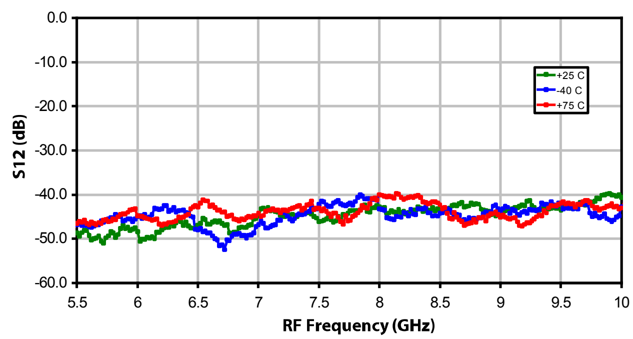
XP1035-QH: S21 (dB) at Vd=6V, Id=500mA



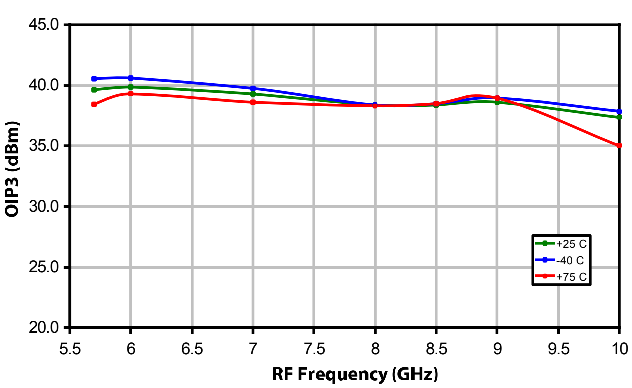
XP1035-QH: S22 (dB) at Vd=6V, Id=500mA



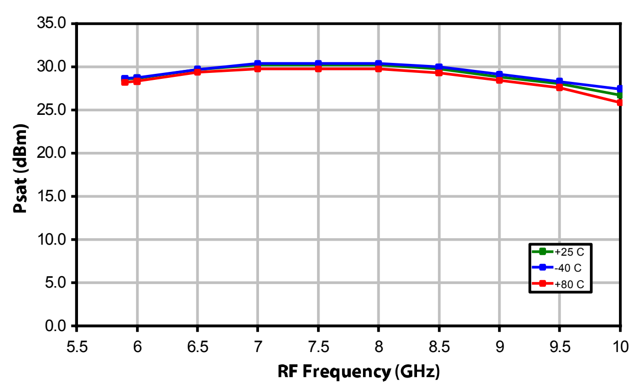
XP1035-QH: S12 (dB) at Vd=6V, Id=500mA



XP1035-QH: OIP3 (dBm) at Vd=6V, Id=500mA

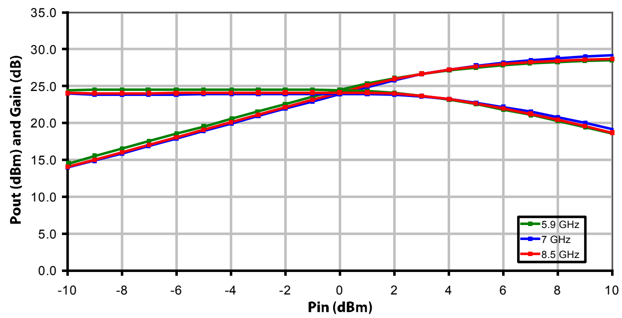


XP1035-QH: Psat (dBm) at Id=500mA, Vd=6V

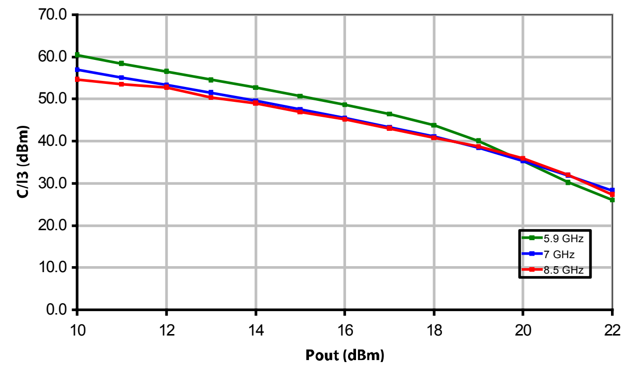


Typical Performance Curves (cont.)

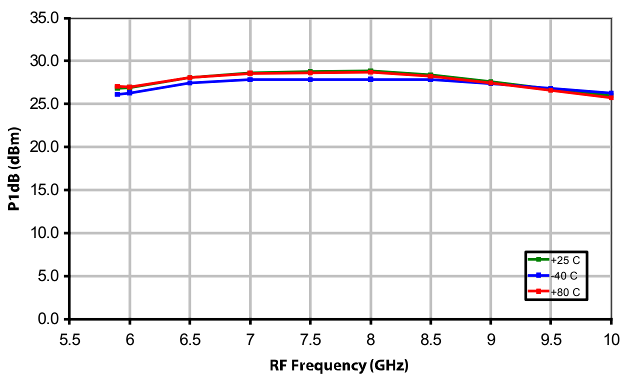
XP1035-QH: Pout (dBm) and Gain (dB) vs Pin (dBm) Id=500mA, Vd=6V, +25 C



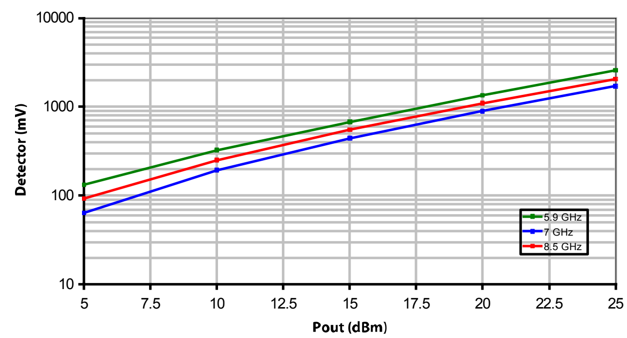
XP1035-QH: C/I3 vs Pout at Id=500mA, Vd=6V, +25 C, 10 MHz Span



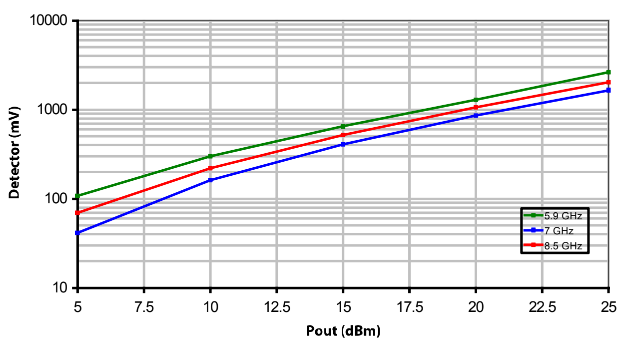
XP1035-QH: P1dB (dBm) at Id=500mA, Vd=6V



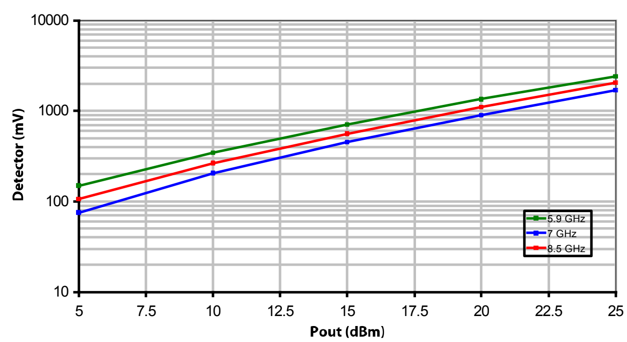
XP1035-QH: Detector (mV) vs Pout (dBm) at Id=500mA, Vd=6V, +25 C



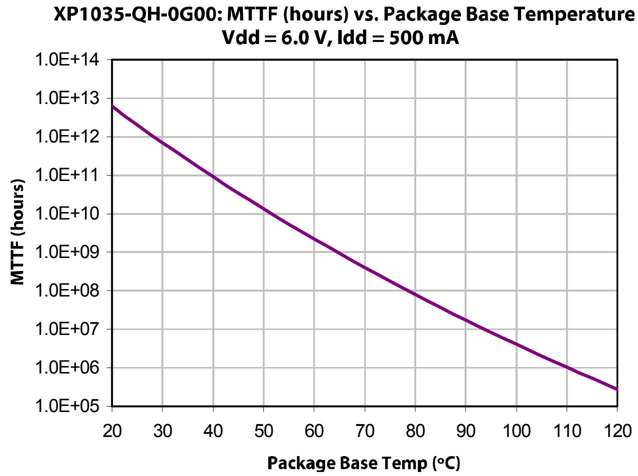
XP1035-QH: Detector (mV) vs Pout (dBm) at Id=500mA, Vd=6V, -40 C

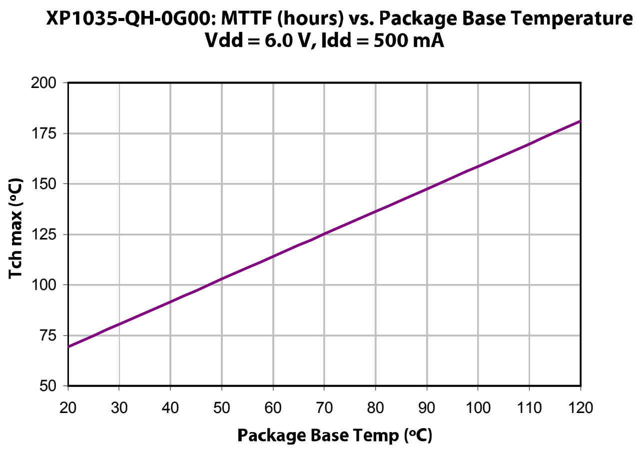


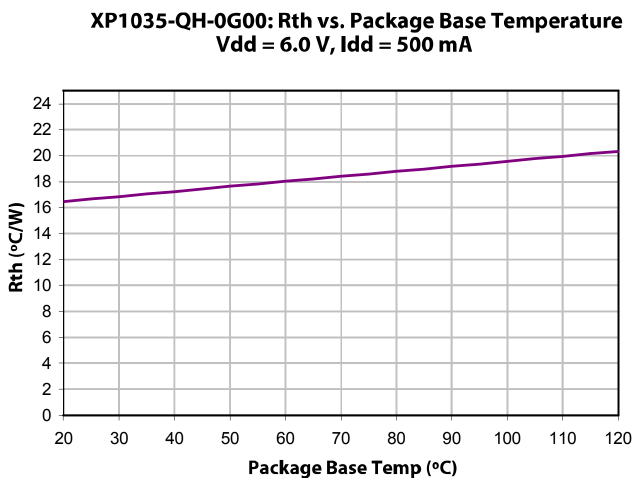
XP1035-QH: Detector (mV) vs Pout (dBm) at Id=500mA, Vd=6V, +80 C



MTTF


XP1035-QH-0G00: MTTF (hours) vs. Package Base Temperature
Vdd = 6.0 V, Idd = 500 mA
MTTF (hours)
1.0E+14
1.0E+13
1.0E+12
1.0E+11
1.0E+10
1.0E+09
1.0E+08
1.0E+07
1.0E+06
1.0E+05
20
30
40
50
60
70
80
90
100
110
120
Package Base Temp (°C)

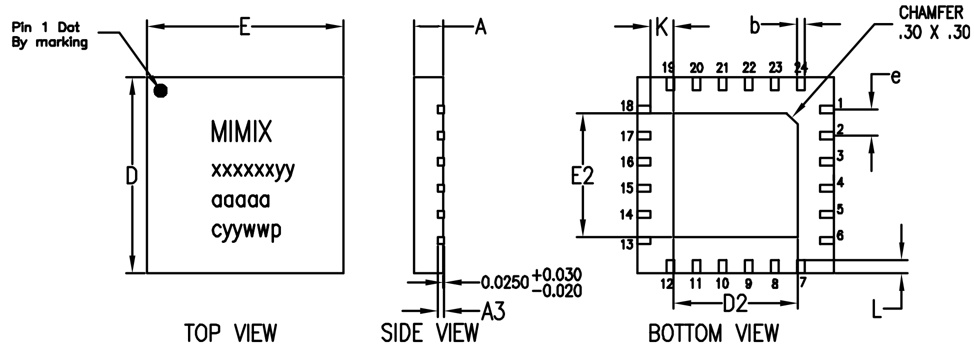

XP1035-QH-0G00: MTTF (hours) vs. Package Base Temperature
Vdd = 6.0 V, Idd = 500 mA
Tch max (°C)
200
175
150
125
100
75
50
20
30
40
50
60
70
80
90
100
110
120
Package Base Temp (°C)


XP1035-QH-0G00: Rth vs. Package Base Temperature
Vdd = 6.0 V, Idd = 500 mA
Rth (°C/W)
24
22
20
18
16
14
12
10
8
6
4
2
0
20
30
40
50
60
70
80
90
100
110
120
Package Base Temp (°C)

App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing VD1,2,3 at 5.0V with 70, 140, 280mA respectively. It is recommended to use active bias to keep the currents constant in order to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -1.0V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

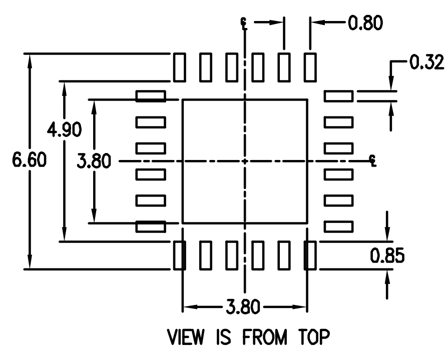
App Note [2] Board Layout - As shown in the board layout, it is recommended to provide 100pF decoupling caps as close to the bias pins as possible, with additional 10µF decoupling caps.

Lead-Free 4 mm 24-Lead PQFN†



MARKINGS:
MIMIX PART/MODEL NO.
WAFER LOT NUMBER
DATE CODE = YYWW
C = COUNTRY OF ORIGIN
P = PLATING OPTION

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
DIMENSIONS ARE IN MM



NOTES:
1. DIMENSIONS ARE IN MM.

	DIMENSION IN MM		
SYM	MIN	TYP	MAX
A	0.85	0.90	0.95
A3	0.20 REF		
b	0.18	0.23	0.28
K	0.70	–	–
D	6.00 BSC ±0.1		
E	6.00 BSC ±0.1		
e	0.80		
D2	3.70	3.80	3.90
E2	3.70	3.80	3.90
L	0.35	0.40	0.45

1. VIEWS MAY NOT BE TO SCALE: USE DIMENSIONS AND TABLE.
2. MARKINGS ARE FOR ILLUSTRATION PURPOSES ONLY. ACTUAL MARKINGS MAY VARY FOR EACH DEVICE TYPE.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.