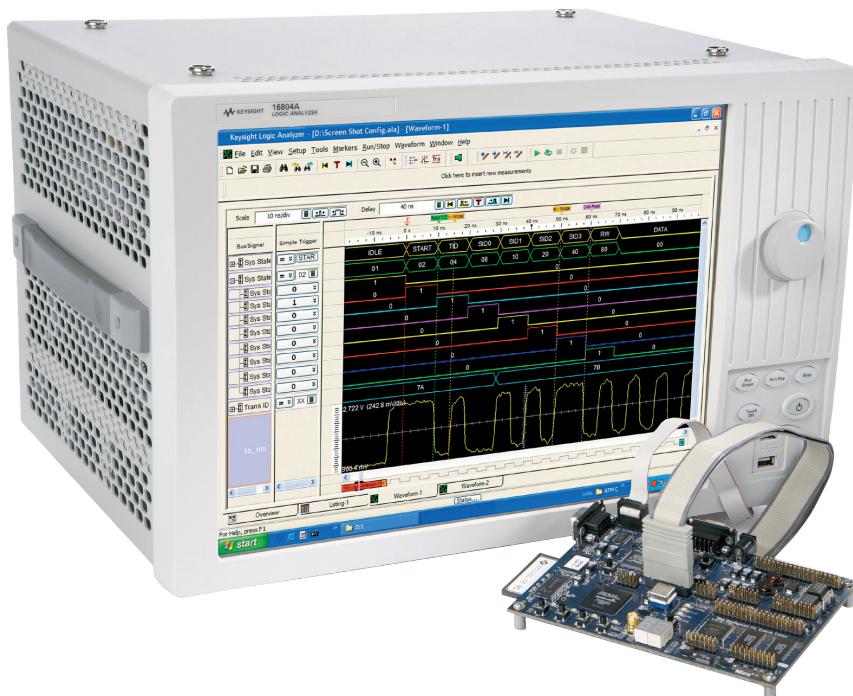


Keysight Technologies

B4656A FPGA Dynamic Probe for Altera

Data Sheet



The Challenge

You rely on the insight a logic analyzer provides to understand the behavior of your FPGA in the context of the surrounding system. Design engineers typically take advantage of the programmability of the FPGA to route internal nodes to a small number of physical pins that a logic analyzer can measure. While this approach is very useful, it has significant limitations.

- Since pins on the FPGA are typically an expensive resource, there are a relatively small number available for debug. This limits internal visibility (i.e. one pin is required for each internal signal to be probed).
- When you need to access different internal signals, you must change your design to route these signals to the available pins. This can be time consuming and can affect the timing of your FPGA design.
- Finally, the process required to map the signal names from your FPGA design to the logic analyzer setup is manual and tedious. When new signals are routed out, you need to manually update these signal names on the logic analyzer, which takes additional time and is a potential source of confusing errors.

Debug Your FPGAs Faster and More Effectively with a Logic Analyzer

FPGA dynamic probe lets you:

View internal activity – With a logic analyzer, you are normally limited to measuring signals at the periphery of the FPGA. With the FPGA dynamic probe, you can now access signals internal to the FPGA. You can measure up to 256 internal signals for each external pin dedicated to debug,

unlocking visibility into your design that you never had before.

Make multiple measurements in seconds – Moving probe points internal to an FPGA used to be time consuming. Now, in less than a second, you can easily measure different sets of internal signals without design changes. FPGA timing stays constant when you select new

sets of internal signals for probing.

Leverage the work you did in your design environment – The FPGA dynamic probe maps internal signal names from your FPGA design tool to your Keysight Technologies, Inc. logic analyzer. Eliminate unintentional mistakes and save hours of time with this automatic setup of signal and bus names on your logic analyzer.

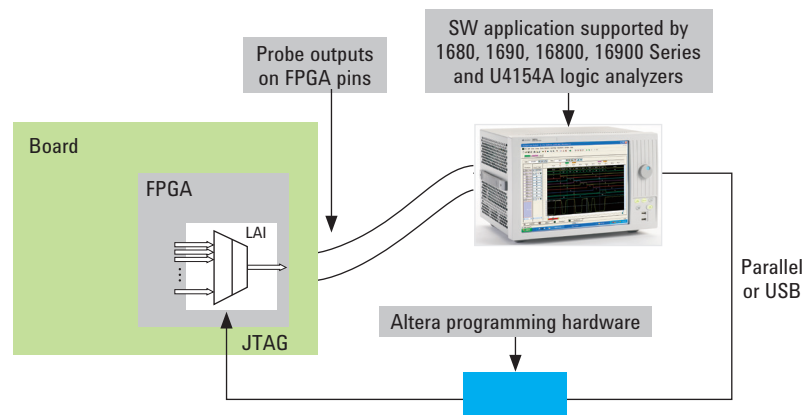


Figure 2. The FPGA dynamic probe requires Altera's Quartus II design software with its logic analyzer interface and Altera programming hardware setup. The Quartus II (ver. 6.0 or higher) logic analyzer interface allows you to create and insert the core for use by the FPGA dynamic probe application on the logic analyzer. This configuration allows you to probe the FPGA pins with the Keysight FPGA dynamic probe software. The FPGA dynamic probe controls which group of internal signals to measure via the Altera programming hardware connected to the JTAG port of the FPGA.

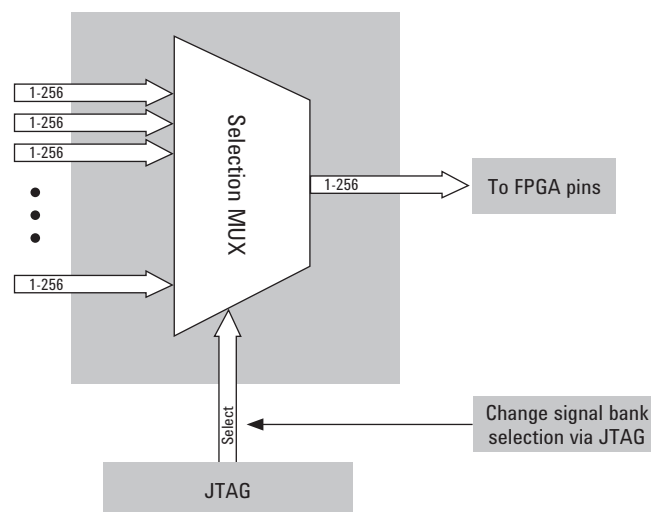
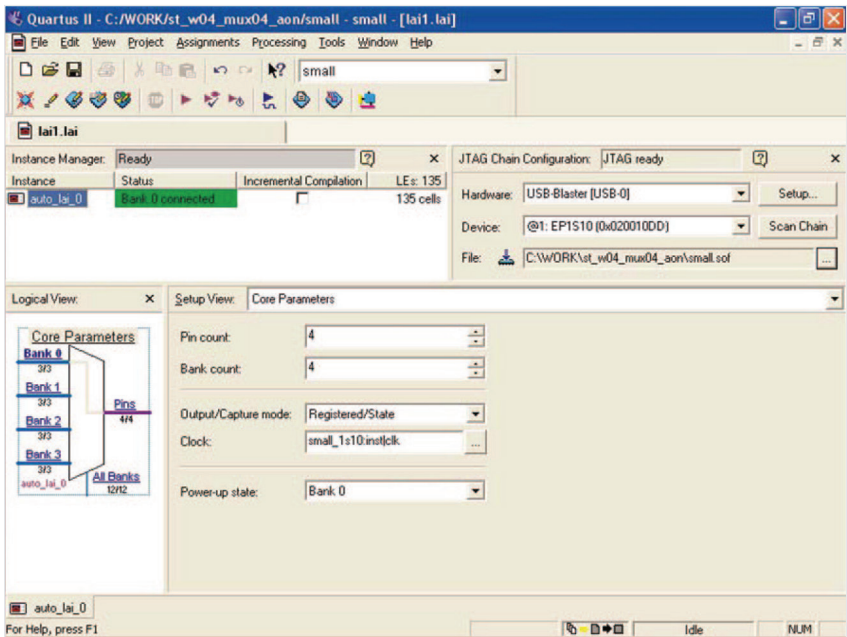


Figure 3. Access up to 256 internal signals for each debug pin. Signal banks all have identical width (1 to 256 signals wide) determined by the number of device pins you devote for debug. Each pin provides sequential access to one signal from every input bank.

A Quick Tour of the Application

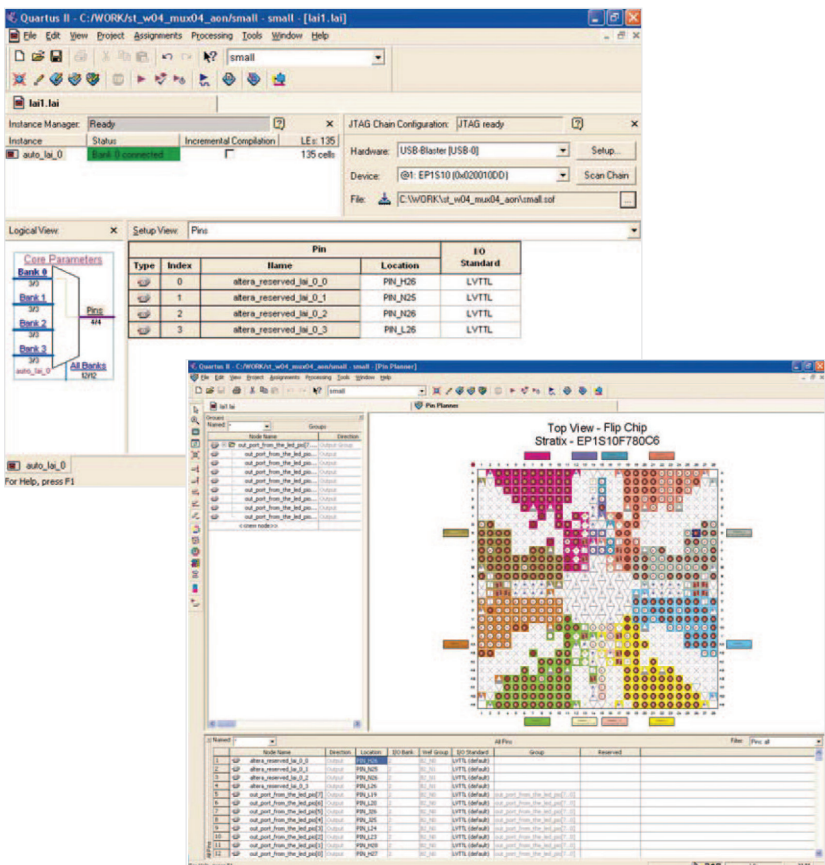
Design step 1: Configure the logic analyzer interface file and core parameters

You need to create a logic analyzer interface file with the logic analyzer interface in Quartus II. This file defines the interface that builds a connection between the internal FPGA signals and the logic analyzer. You can then configure the core parameters, which include number of pins, number of signal banks, the type of measurement (state or timing), clock and the power-up state.



Design step 2: Map the logic analyzer interface core outputs to available I/O pins

Use Pin Planner in Quartus II to assign physical pin locations for the logic analyzer interface core.

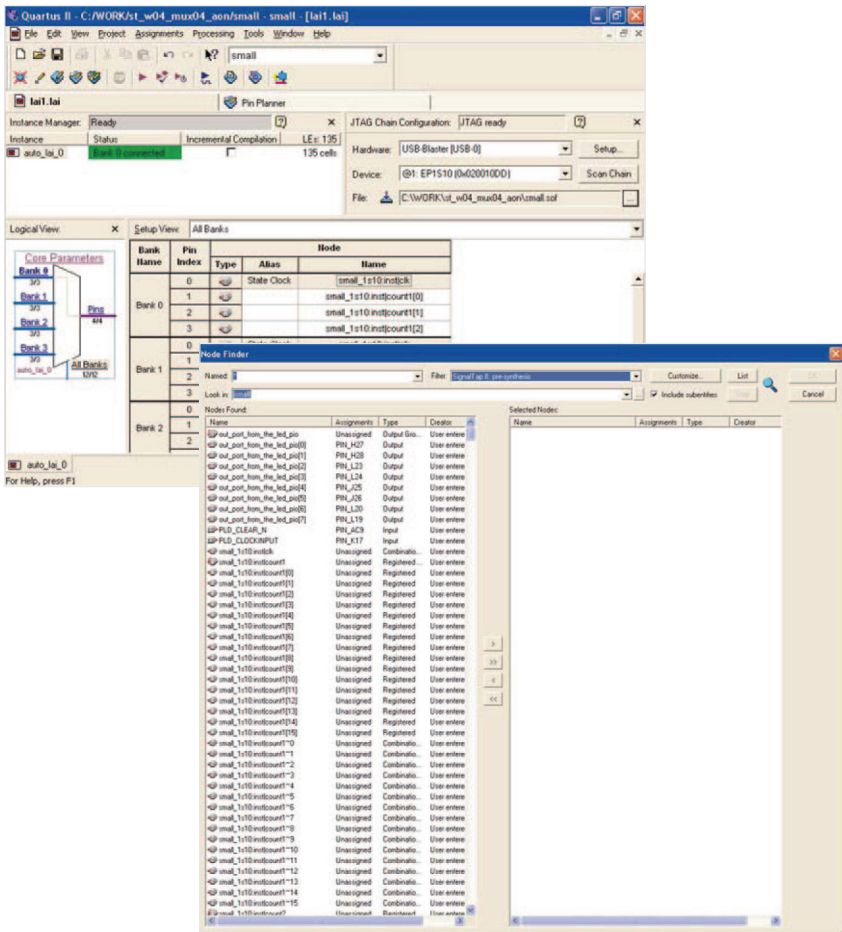


A Quick Tour of the Application (continued)

Design step 3: Assign logic analyzer interface bank parameters

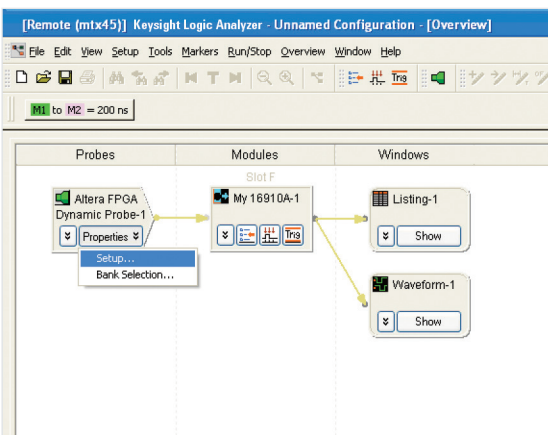
Assign internal signals to each bank in the logic analyzer interface after you have specified the number of banks to use in the core parameters. Find the signals you want to acquire with the Node Finder and assign them to the banks.

With the logic analyzer interface core fully configured and instantiated into your FPGA design, you're ready to compile your design to create the device programming file (.sof). Then, to make measurements you'll move to the Keysight logic analyzer software.



Activate FPGA dynamic probe for Altera

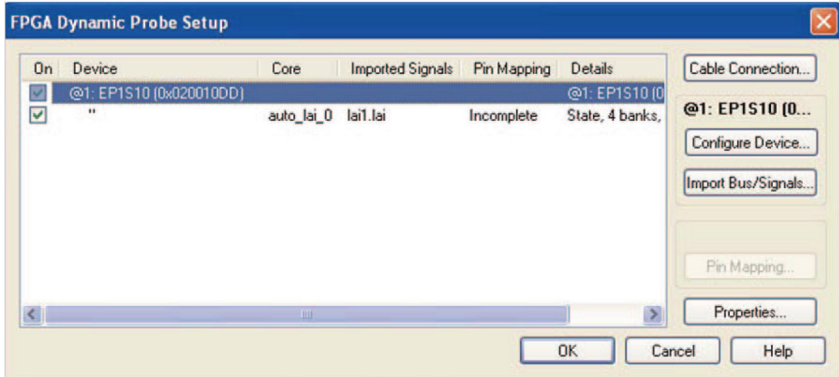
The FPGA dynamic probe icon allows you to control the logic analyzer interface and set up the logic analyzer for the desired measurements.



A Quick Tour of the Application (continued)

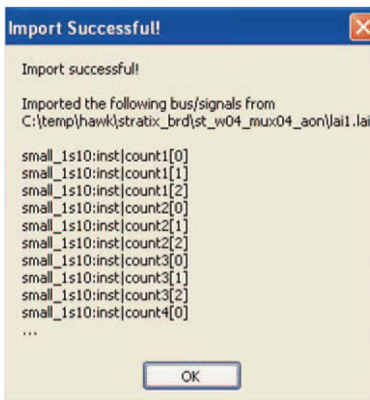
Measurement setup step 1:
Establish a connection
between the logic analyzer
and the logic analyzer
interface

The FPGA dynamic probe application establishes a connection between the logic analyzer and the FPGA via a JTAG cable. It also determines what devices are on the JTAG scan chain and lets you pick the one with which you wish to communicate.



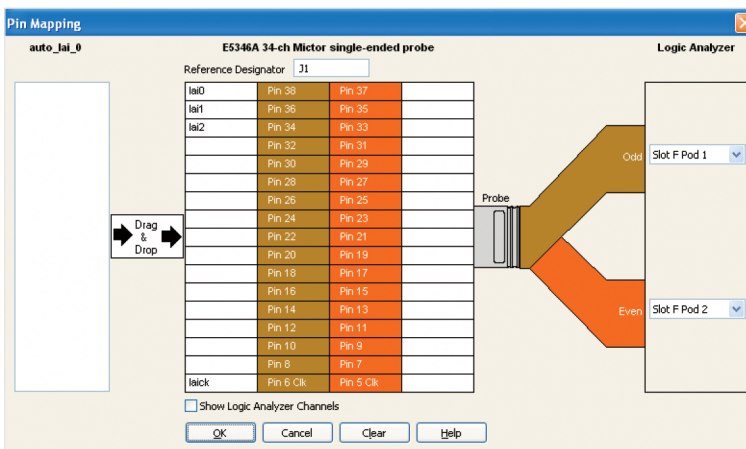
Measurement setup step 2:
Configure the device and
import signal names

If needed, you can configure the device with the SRAM object file (.sof) that includes the logic analyzer interface file. The FPGA dynamic probe application reads a .lai file produced by Quartus II. The names of signals you measure will now automatically appear in the label names on your Keysight logic analyzer.



Measurement setup step 3:
Map FPGA pins

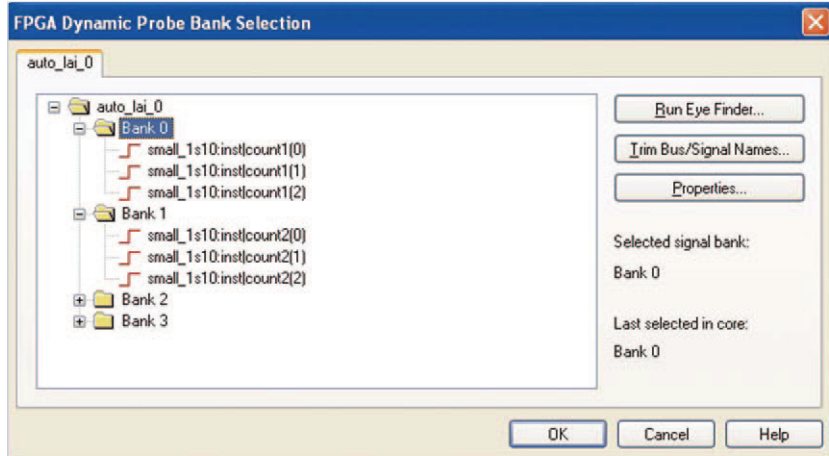
Select your probe type and easily provide the information needed for the logic analyzer to automatically track names of signals routed through the logic analyzer interface file.



A Quick Tour of the Application (continued)

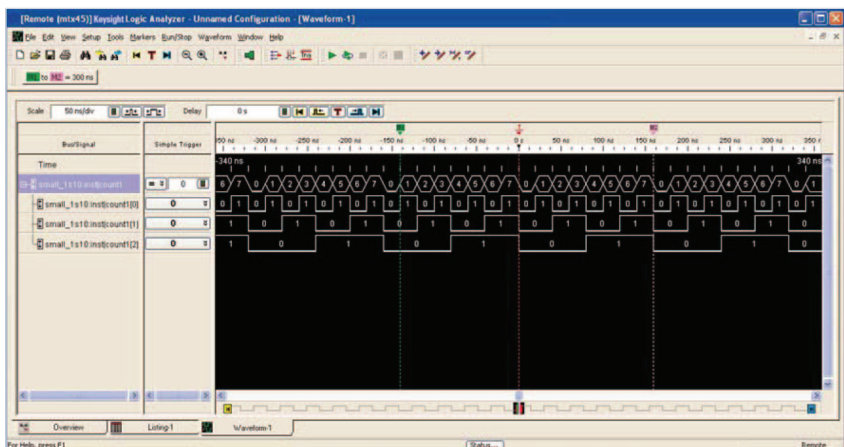
Setup complete: Make measurements

Quickly change which signal bank is routed to the logic analyzer. A single mouse click tells the logic analyzer interface core to switch to the newly specified signal bank without any impact to the timing of your design. To make measurements throughout your FPGA, change signal banks as often as needed. With each new selection of a signal bank, FPGA Dynamic Probe updates new signal names from your design to the logic analyzer. User-definable signal bank names make it straight forward to select a part of your design to measure.



Correlate internal FPGA activity with external measurements

View internal FPGA activity and time-correlate internal FPGA measurements with external events in the surrounding system. FPGA Dynamic Probe unlocks the power of the logic analyzer for system-level debug with FPGAs.



Keysight B4656A Specifications and Characteristics

Supported logic analyzers	
Standalone logic analyzers	1680 Series, 1690 Series, 16800 Series
Modular logic analysis systems	16900 Series with one or more state/timing modules: A single node-locked FPGA dynamic probe license will enable all modules within a 16900 Series system
AXIe-based Logic Analyzer	U4154A
Triggering capabilities	Determined by logic analyzer
Supported Altera FPGA families	All families that the Altera LAI core supports including: Stratix IV GX (where SOF* support is available), Stratix IV, Stratix III, Stratix II, and Stratix; Cyclone IV (where SOF* support is available), Cyclone III, Cyclone II, and Cyclone; Arria II and Arria *SOF is the SRAM Object File (.sof) that is generated in Quartus for a specific device.
Supported Altera cables (required)	Altera USB Blaster or ByteBlaster
Supported probing mechanisms	Soft touch (34-channel and 17-channel), Mictor, Samtec, Flying lead
Logic analyzer interface characteristics	
Number of output signals	User definable: 1 to 256 signals in 1 signal increments
Signal banks	User definable: 1 to 256 banks
Modes	State (synchronous) or timing (asynchronous) mode
Compatible software	
Altera Quartus II 6.0 or greater	1680, 1690, 16800, 16900 Series software version 03.55 or greater

Additional information available via the Internet (www.keysight.com/find/FPGA)

Ordering Information

Ordering options for the Keysight B4656A FPGA dynamic probe for Altera	
Option 010	<ul style="list-style-type: none">– Entitlement certificate for perpetual node-locked license– CD with application software
Option 020	<ul style="list-style-type: none">– Entitlement certificate for perpetual floating license– CD with application software

Related Keysight Literature

Publication title	Pub number
<i>Frequently Asked Questions for Keysight B4656A FPGA Dynamic Probe for Altera Data Sheet</i>	5989-5716EN
<i>Keysight Technologies 16900 Series Logic Analysis Systems Color Brochure</i>	5989-0420EN
<i>Keysight Technologies Measurement Modules for the 16900 Series Data Sheet</i>	5989-0422EN
<i>U4154A Logic Analyzer Module Data Sheet</i>	5990-7513EN
<i>Probing Solutions for Keysight Technologies Logic Analyzers Catalog</i>	5966-4632E
<i>Keysight 16800 Series Portable Logic Analyzers Color Brochure</i>	5989-5062EN
<i>Keysight 16800 Series Portable Logic Analyzers Data Sheet</i>	5989-5063EN
<i>Keysight 1680 and 1690 Series Logic Analyzers Data Sheet</i>	5988-2675EN

For the most up-to-date and complete application and product information, please visit our product Web site at www.keysight.com/find/logic

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