M31544, M31564

3G/HD/SD-SDI Long Reach Adaptive Cable Equalizer with Integrated Jitter Cleaner

The M31544/64 are multi-rate, highly integrated, adaptive cable equalizers for SDI and DVB-ASI video as well as digital audio applications. It provides adaptive, low noise, high gain equalization for 75 Ω coaxial cables at SDI and MADI data rates from 125 Mbps to 2.97 Gbps. The device is capable of compensating for losses accumulated across cable length up to 200 m when operating at 2.97 Gbps.

The M31544/64 feature an integrated jitter cleaner, which automatically removes the jitter generated at HD-SDI and 3G-SDI data rates at the output of the equalizer, eliminating the need for standalone reclockers at the input, reducing system cost, complexity and power consumption. The jitter cleaner may be powered down and bypassed in applications where it is not required to allow for optimized power consumption for each application.

The M31544 also features dual differential outputs, eliminating the need for additional circuitry and simplifying system design. Both outputs feature programmable swing as well as de-emphasis for enabling the signal to be transmitted across 40" of FR4 trace. The second, optional output may be disabled for additional power savings.

The device operates using a single 2.5 V supply voltage and has extremely low power consumption with the equalizer and jitter cleaner dissipating only 145 mW when one output driver is enabled. It may be used in either hardware mode, or controlled through a standard four-wire serial digital interface. Furthermore, it features advanced diagnostic capabilities such as cable length indication, loss of signal detection, and offers power management functions such as power down upon loss of signal.

The M31544/64 are offered in a green and RoHS compliant small footprint QFN package.

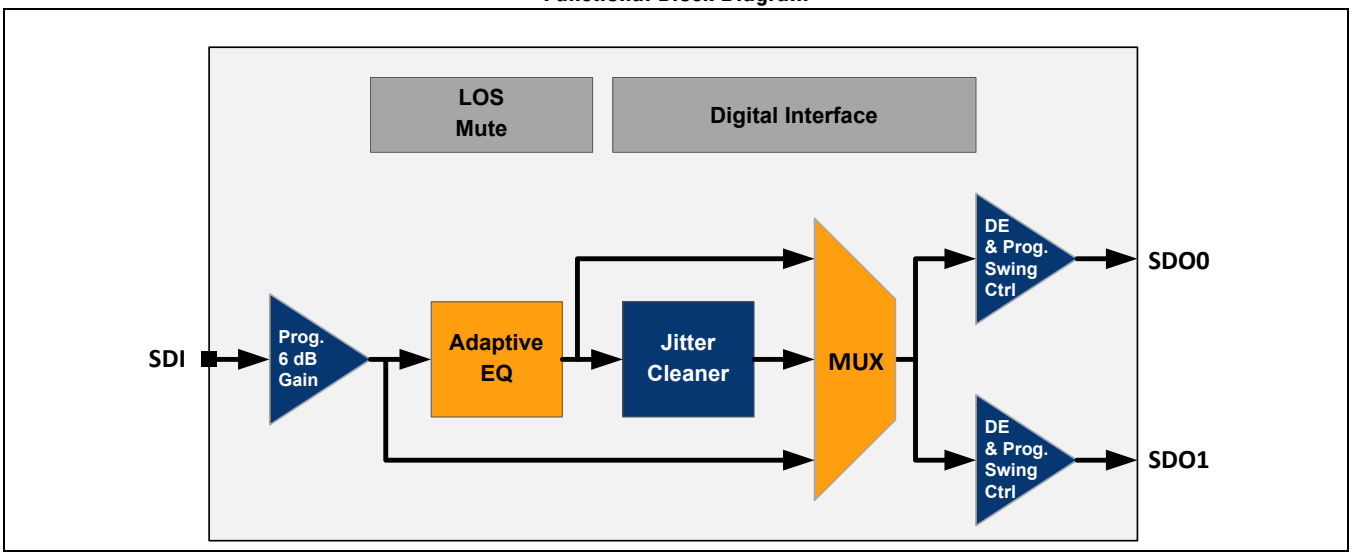
Features

- SMPTE 424M, SMPTE 292M, SMPTE 344M, SMPTE 259M, and DVB-ASI compliant
- Robust adaptive cable equalization for up to 200 meters of Belden 1694A at 2.97 Gbps, up to 200 meters of Belden 1694A at 1.485 Gbps and up to 400 meters of Belden 1694A at 270 Mbps
- MADI (125 Mbps) compatible
- Integrated jitter cleaner for 3G/HD-SDI use with automatic rate detection
- Individually controllable dual differential output drivers with programmable 8 dB of de-emphasis
- Optional 6 dB flatband gain at input
- Cable length indication
- SD, HD and 3G Data Rate Detection
- Optional four-wire serial digital interface
- Very low power consumption: 145 mW (single output), 160 mW (dual output)
- Power down and mute features
- Industrial operating temperature range: -40 °C to +85 °C

Applications

- Broadcast video routing and production switchers
- Broadcast video distribution amplifiers
- Broadcast video cameras and monitors

Functional Block Diagram



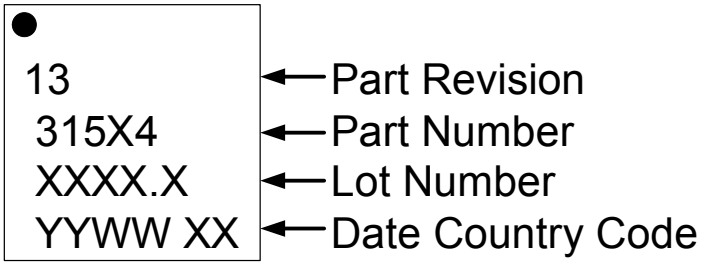
Ordering Information

Part Number	Package	Operating Data Rate	Operating Temperature
M31544G-13*	24-pin QFN (RoHS compliant)	125–2970 Mbps	–40 °C to 85 °C
M31564G-13*	16-pin QFN (RoHS compliant)	125–2970 Mbps	–40 °C to 85 °C
* The letter 'G' designator after the part number indicates a RoHS-compliant package. Refer to www.mindspeed.com for additional information.			

Revision History

Revision	Level	Date	Description
B	Release	November 2013	Removed M31554 support. Updated power consumption specification Table 1-3. Updated PCML I/O electrical characteristics Table 1-4. Updated DC characteristics for digital I/O pins Table 1-5. Added Analog and digital mute sections in the functional description, Section 4.1.3 and Section 4.1.4. Updated timing specifications for the 4-wire interface Table 4-7.
A	Release	July 2013	Initial Release.

M31544/64 Marking Diagram



1.0 Electrical Characteristics

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit
AV_{DD}	Analog power supply voltage	-0.5	2.75	V
$V_{IN,PCML}$	DC input voltage (PCML)	V_{SS} - 0.5	AV_{DD} + 0.5	V
$V_{IN,CMOS}$	DC input voltage (CMOS)	V_{SS} - 0.6	AV_{DD} + 0.5	V
T_{STORE}	Storage temperature	-65	150	°C
T_{JUNC}	Junction temperature	—	125	°C
$V_{ESD,HBM}$	Electrostatic discharge voltage (HBM)	-3000	3000	V
$V_{ESD,CDM}$	Electrostatic discharge voltage (CDM)	-500	500	V
$V_{ESD,}$mm	Electrostatic discharge voltage (mm)	-150	150	V

NOTES:

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage.
2. HBM and CDM per JEDEC Class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

Table 1-2. Recommended Operating Conditions

Symbol	Parameter		Minimum	Typical	Maximum	Unit
AV_{DD}	Analog power supply voltage		2.37	2.5	2.63	V
T_{CASE}	Operating case temperature		-40	—	85	°C
θ_{JC}	Junction to case thermal resistance	M31544/64	—	—	13.8	°C/W

NOTES:

1. Thermal resistance value is calculated using a 5% increase on the supply voltage and includes all temperature variations.

Table 1-3. Power Consumption Specifications (1 of 2)

Symbol	Parameter			Typical	Maximum	Unit
AI_{DD} Core Current Consumption	One output enabled	Jitter cleaner OFF	Intermediate output swing	42	54	mA
			Maximum output swing	44	56	mA
		Jitter cleaner ON	Intermediate output swing	56	68	mA
			Maximum output swing	57	70	mA

Table 1-3. Power Consumption Specifications (2 of 2)

Symbol	Parameter			Typical	Maximum	Unit
AI_{DD} Core Current Consumption	Two outputs enabled	Jitter cleaner OFF	Intermediate output swing	48	61	mA
			Maximum output swing	51	64	mA
		Jitter cleaner ON	Intermediate output swing	62	75	mA
			Maximum output swing	64	78	mA
P_{TOTAL}	One output enabled	Jitter cleaner OFF	Intermediate output swing	105	142	mW
		Jitter cleaner ON		140	179	mW
	Two outputs enabled	Jitter cleaner OFF		120	160	mW
		Jitter cleaner ON		155	197	mW

NOTES:

1. Maximum current and maximum power consumption numbers are calculated using a 5% increase on the supply voltage, with jitter cleaner and include all temperature and process variations.
2. Jitter cleaner is automatically bypassed and turned off for SD data rates.
3. When the jitter cleaner is turned off, the power consumption is data rate independent. Once the jitter cleaner is turned on, the power consumption for HD and 3G data rates will be according to the table above.

Table 1-4. PCML Input/Output Electrical Characteristics (1 of 2)

Symbol	Parameter		Note	Minimum	Typical	Maximum	Unit
Input							
DR	NRZ data rate		—	19	—	2970	Mbps
V_{IN}	Input voltage swing		—	720	800	880	mV_{PP}
S_{11}	Input Return Loss	5 MHz to 1.5 GHz	1	15	18	—	dB
		1.5 GHz to 3 GHz		10	15	—	
Output							
V_{OUT}	Differential output swing	Low output swing	—	250	365	480	mV_{PPD}
		Intermediate output swing	—	390	555	720	
		Maximum output swing	—	540	740	940	
V_{OCM}	Output Common Mode Voltage	0.8V	—	0.4	0.8	0.9	V
		1.0V	—	0.6	1.0	1.1	
		1.2V (Default)	—	0.8	1.2	1.3	
t_R/t_F	Output rise/fall time (20% - 80%)		2	—	90	130	ps
DE	Output De-emphasis range		3	0	—	8	dB
Jitter Cleaner							
DR	Input data rate retimed	SMPTE 292M	—	—	1483, 1485	—	Mbps
		SMPTE424M	—	—	2967, 2970	—	Mbps
F_{LBW}	Loop bandwidth	SMPTE 292M	—	—	2	—	MHz
		SMPTE424M	—	—	4	—	MHz
$t_{LOCK,}$	Lock time	asynchronous	—	—	—	15	ms
		synchronous	—	—	—	1	µs

Table 1-4. PCML Input/Output Electrical Characteristics (2 of 2)

Symbol	Parameter		Note	Minimum	Typical	Maximum	Unit
Jitter Performance, Jitter Cleaner Bypassed							
t_{JIT}	Total jitter added at 270 Mbps	0 - 400 m	4, 5,6	—	—	300	mUI
	Total jitter added at 1.485 Gbps	0 - 200 m	4, 5	—	200	400	
	Total jitter added at 2.97 Gbps	0 - 100 m	4, 5	—	—	230	
		100 - 140 m		—	—	320	
		140 - 180 m		—	—	450	
		180 - 200 m		—	450	—	
Jitter Performance, Jitter Cleaner Enabled							
t_{JIT}	Total jitter added at 1.485 Gbps	0 - 200 m	4, 5, 6	—	50	100	mUI
	Total jitter added at 2.97 Gbps	0 - 200 m	4, 5, 6	—	100	170	

NOTES:

1. Typical values measured on Mindspeed evaluation board MH12-D670. Values depend on layout.
2. Measured using a clock pattern with 50% duty cycle and consisting of 10 Consecutive Identical Digits (10 CID).
3. Programmable in 2 dB steps.
4. Measured according to SMPTE RP184 and SMPTE RP192. Using Belden 1694A cable.
5. Measured using PRBS10 test pattern with default output swing.
6. Jitter cleaner can only be used for HD and 3G data rates, it is automatically bypassed and powered down for SD data rates.

Table 1-5. DC Characteristics for Digital I/O pins

Symbol	Parameter	Reference	Note	Minimum	Typical	Maximum	Unit
V_{OH}	Digital output logic high	MF0, MF1and MF3	1	0.85 x AV_{DD}	AV_{DD}	—	V
V_{OL}	Digital output logic low		2	—	0	0.15 x AV_{DD}	V
V_{IH}	Digital input logic high	MODE_SEL, SDO1_DISABLE, xCS, MF0, MF1, MF2 and MF3	—	0.75 x AV_{DD}	—	AV_{DD}	V
V_{IL}	Digital input logic low		—	0	—	0.25 x AV_{DD}	V
C_{IN}	Input capacitance		—	—	10	—	pF
V_{IF}	Digital input logic float	MF0	—	0.35 x AV_{DD}	—	0.65 x AV_{DD}	V

NOTES:

1. I_{OH} = -4 mA.
2. I_{OL} = 4 mA.

2.0 Typical Performance Characteristics

Unless noted otherwise, typical performance applies for AV_{DD} = 2.5 V, 25 °C ambient temperature, 800 mV_{PPD} differential input/output data swing, PRBS 2^{10} – 1 data pattern at 2.97 Gbps,

Figure 2-1. Eye Diagram @2.97 Gbps Unequalized Signal, After 200 m Belden 1694A Cable

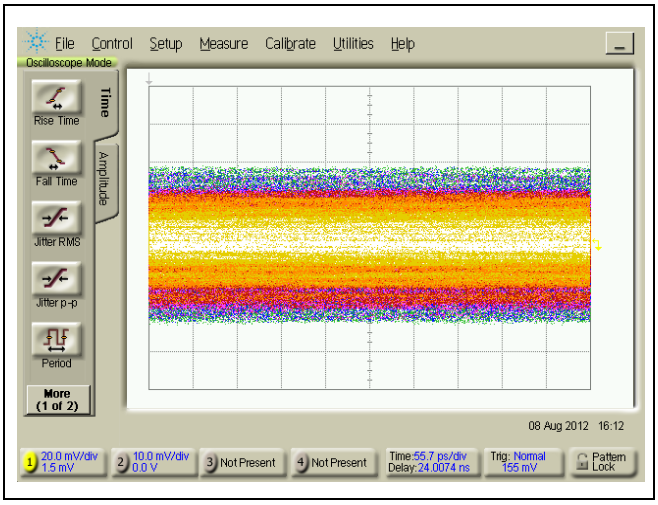


Figure 2-2. Eye Diagram @2.97 Gbps Equalized Signal, After 200 m Belden 1694A Cable (Jitter Cleaner Disabled)

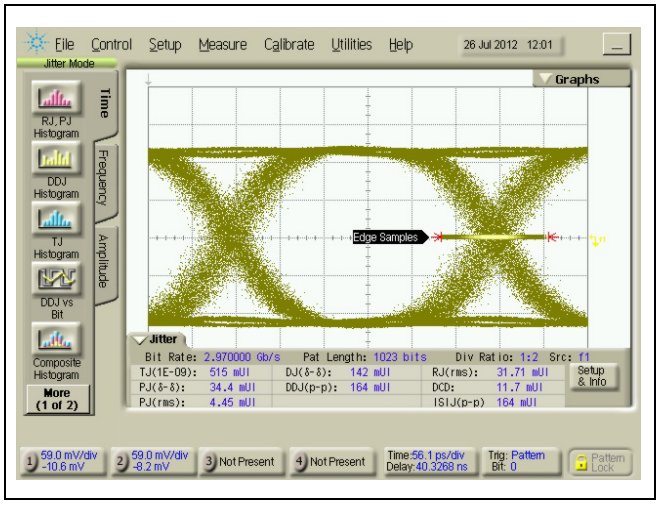
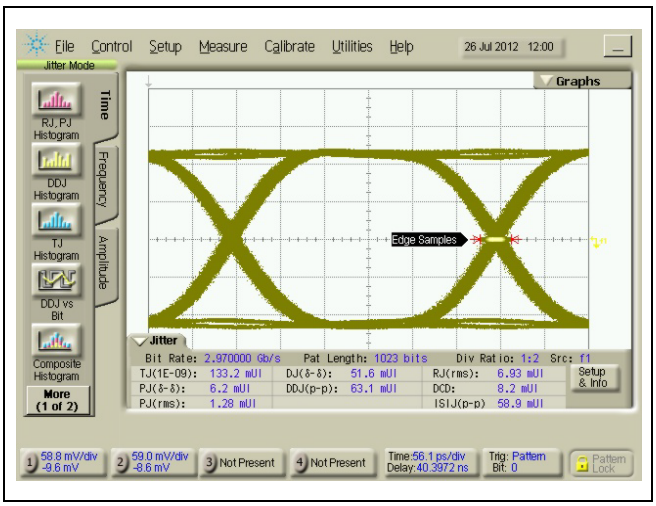


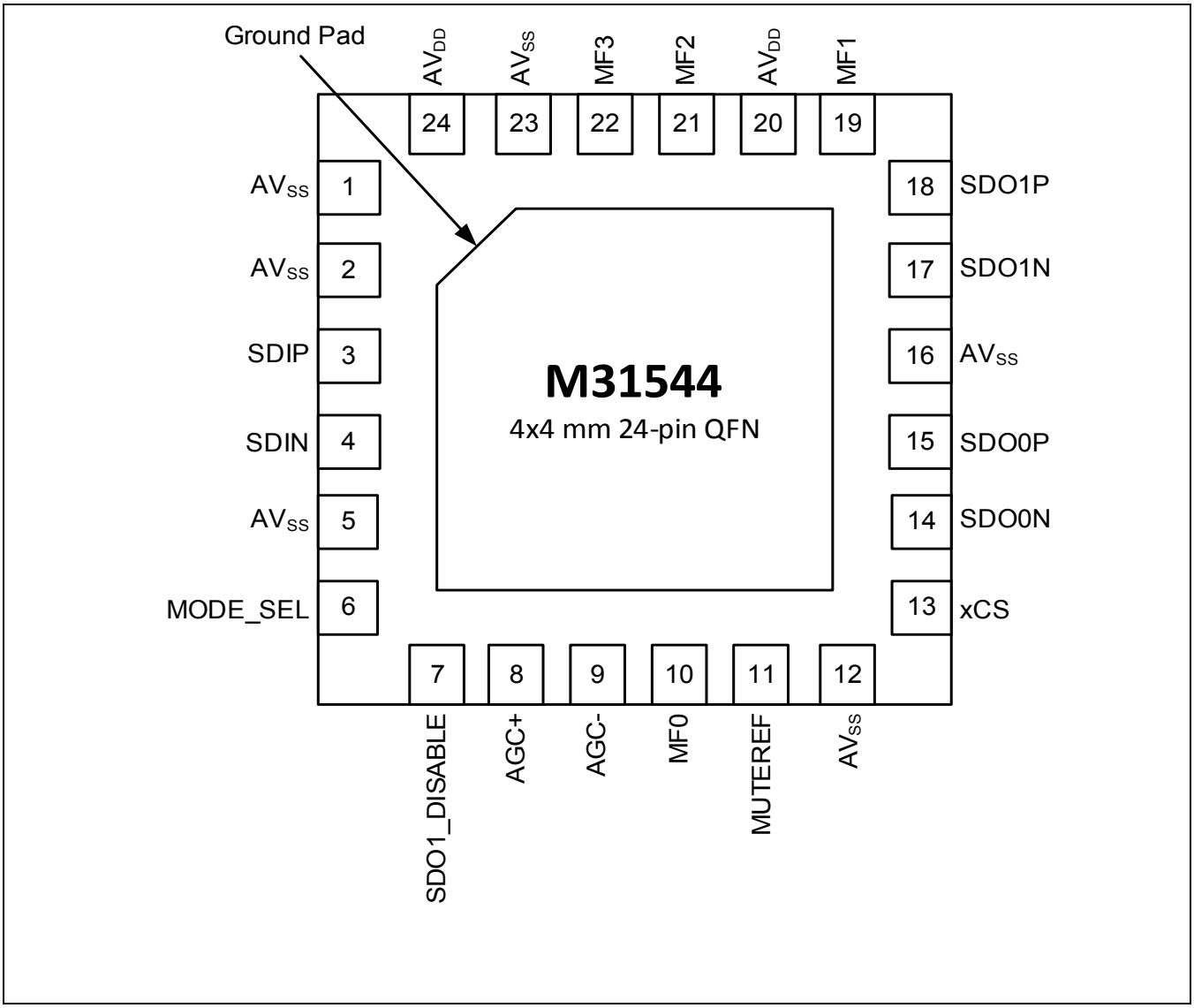
Figure 2-3. Eye Diagram @2.97 Gbps Equalized Signal, After 200 m Belden 1694A Cable (Jitter Cleaner Enabled)



3.0 Pinout Diagram, Pin Descriptions, and Package Outline Drawing

3.1 M31544 Pinout

Figure 3-1. M31544 Pinout Diagram



3.2 M31544 Pin Description

Table 3-1. M31544 Pin Descriptions (1 of 2)

Pin Name	Pin Number(s)	Type	Description
AV_{DD}	20,24	Power	Positive power supply (2.5 V)
AV_{SS}	1,2,5,12,16,23, Ground Pad	Ground	Negative power supply (ground)
SDIP/SDIN	3,4	I, SDI	Serial data input (Positive/Negative)
SDO0P/SDO0N	15,14	O, LVDS	Serial data output 0 (Positive/Negative)
SDO1P/SDO1N	18,17	O, LVDS	Serial data output 1(Positive/Negative)
MODE_SEL	6	I, LVCMOS	Mode Select (Internal pull down) **H: Software Mode Enabled** (4-wire digital interface) **L: Hardware Mode Enabled**
SDO1_DISABLE	7	I, LVCMOS	SDO1 disable pin (Internal pull up) H: SDO1 disable L: SDO1 enable Hardware pin state overrides register settings configurations
AGC+/-	8,9	I/O, Analog	Equalizer loop filter capacitor (33 nF)
MF0	10	I/O, LVCMOS	**Hardware Mode** (MODE_SEL =0) Input, BYPASS H: Bypass entirely the equalizer and jitter cleaner F: Bypass only the jitter cleaner L: Normal operation **Software Mode** (MODE_SEL =1) Output, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is present and cable length is below the MUTEREF threshold
MUTEREF	11	I, Analog	Mute reference input. Defines the cable length threshold at which the signal detect will be asserted. This pin can be left floating or can be grounded for maximum equalization
xCS	13	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Must be set LOW for normal operation. **Software Mode** (MODE_SEL =1) Chip Select Complement (Internal pull up)
MF1	19	I/O, LVCMOS	**Hardware Mode** (MODE_SEL =0) Input, automatic sleep control. Sleep mode has precedence over MUTE and BYPASS. H: Automatic power down when no input is present L: The equalizer is always active **Software Mode** (MODE_SEL =1) 4-wire: Signal Out (Internal pull up)

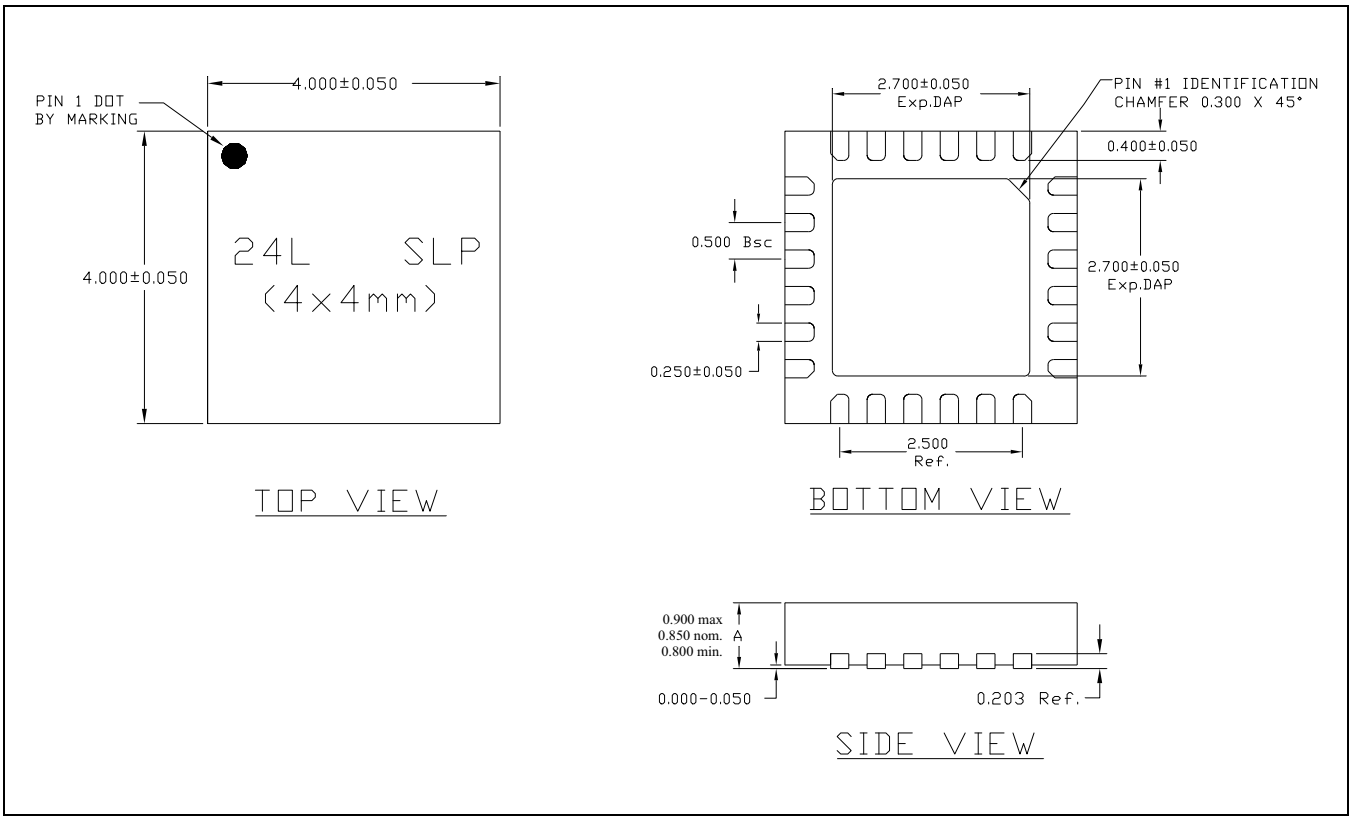
Table 3-1. M31544 Pin Descriptions (2 of 2)

Pin Name	Pin Number(s)	Type	Description
MF2	21	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Input, output buffer MUTE control, MUTE has precedence over BYPASS. H: Outputs are muted L: Normal operation **Software Mode** (MODE_SEL =1) 4-wire: SCLK (Internal pull down)
MF3	22	I/O, LVCMOS	**Hardware Mode** (MODE_SEL =0) Output, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is present and cable length is below the MUTEREF threshold **Software Mode** (MODE_SEL =1) 4-wire: Signal In (Internal pull down)

3.3 M31544 Package Information

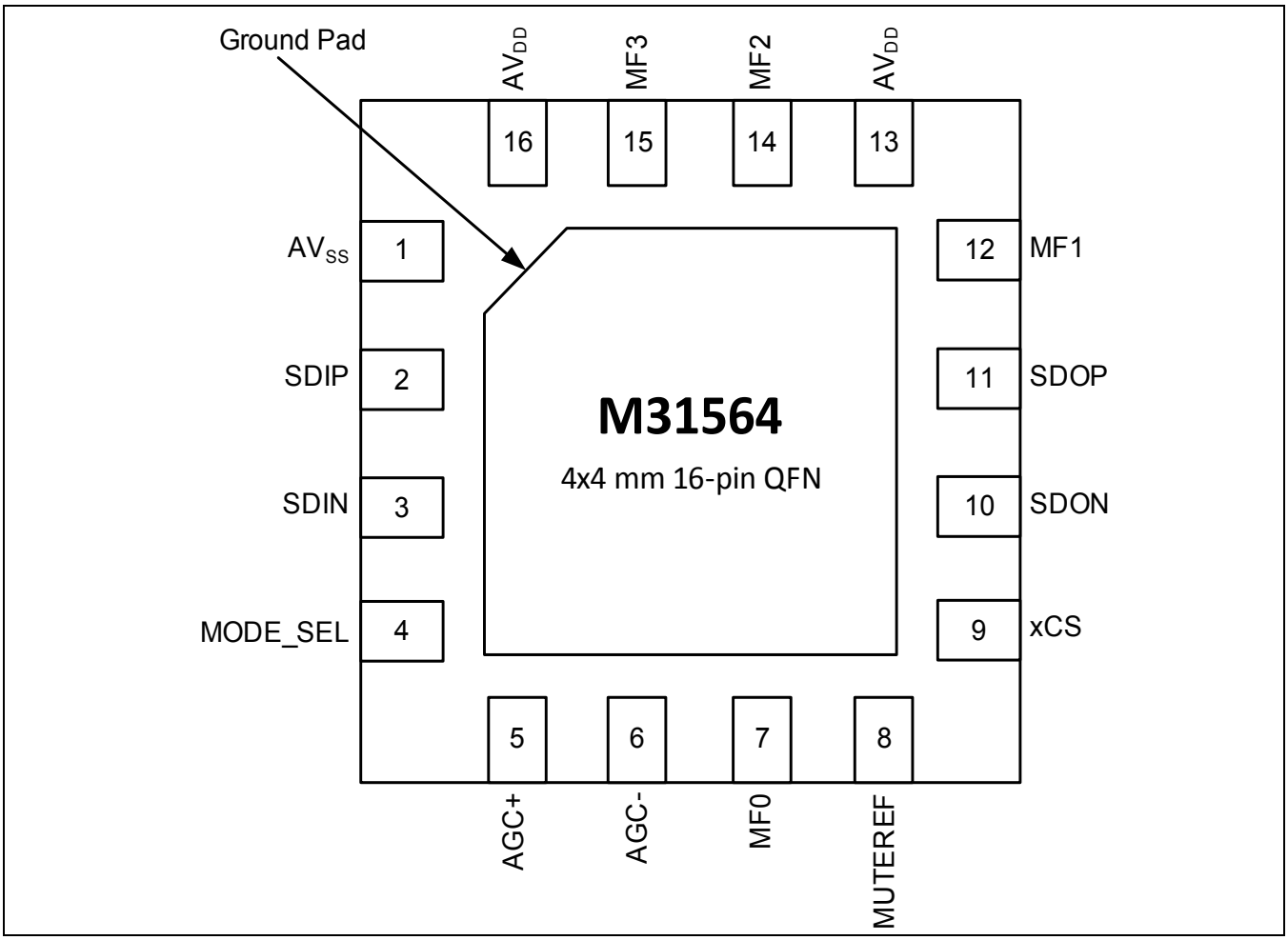
The M31544 is packaged in a 4 mm x 4 mm footprint, 24-pin QFN SLP.

Figure 3-2. M31544 Packaging Drawing



3.4 M31564 Pinout

Figure 3-3. M31564 Pinout Diagram



3.5 M31564 Pin Description

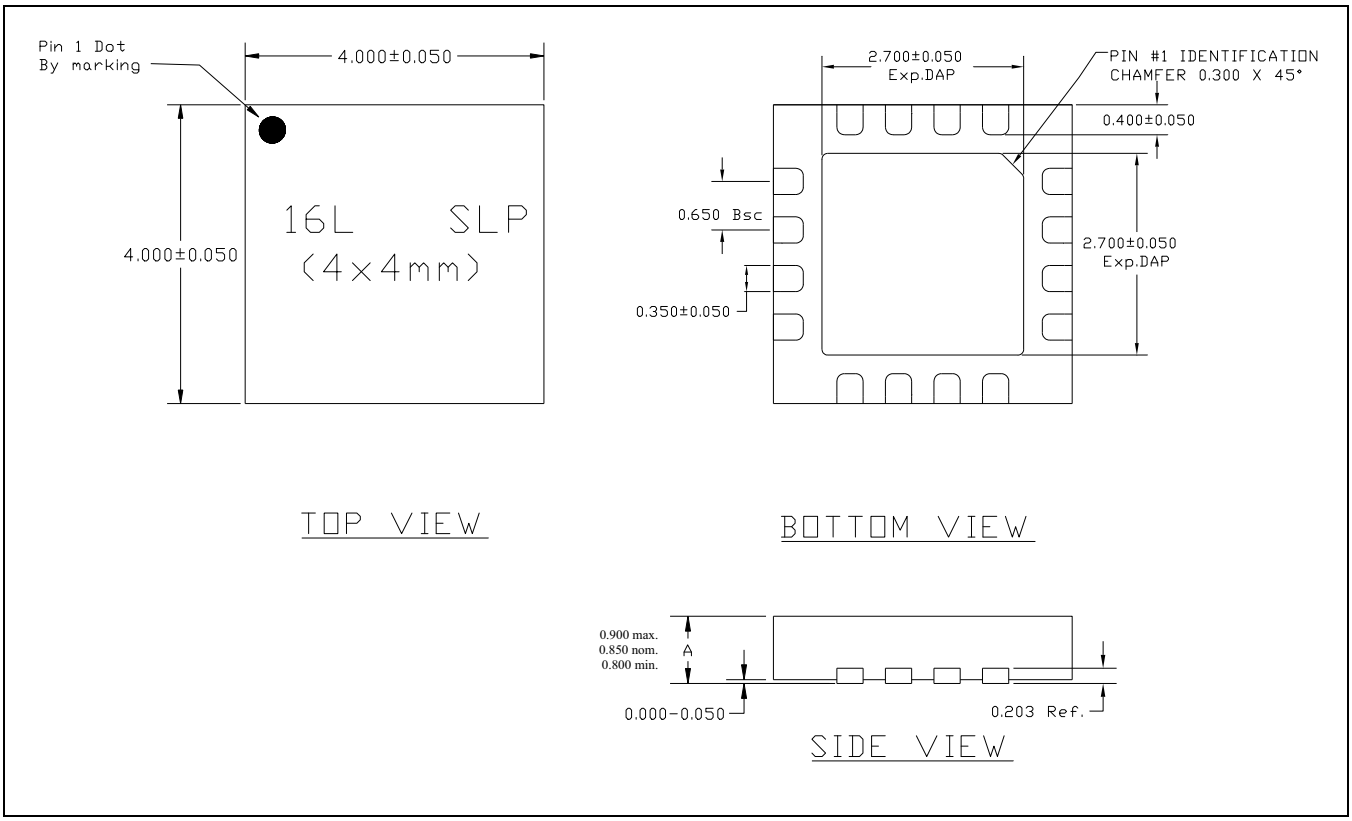
Table 3-2. M31564 Pin Descriptions

Pin Name	Pin Number(s)	Type	Description
AV_{DD}	13,16	Power	Positive power supply (2.5 V)
AV_{SS}	1, Ground Pad	Ground	Negative power supply (ground)
SDIP/SDIN	2,3	I, SDI	Serial data input (Positive/Negative)
SDOP/SDON	11,10	O, LVDS	Serial data output (Positive/Negative)
MODE_SEL	4	I, LVCMOS	Mode Select (Internal pull down) **H: Software Mode Enabled** (4-wire digital interface) **L: Hardware Mode Enabled**
AGC+/-	5,6	I/O, Analog	Equalizer loop filter capacitor (33 nF)
MF0	7	I/O, LVCMOS	**Hardware Mode** (MODE_SEL =0) Input, BYPASS H: Bypass entirely the equalizer and jitter cleaner F: Bypass only the jitter cleaner L: Normal operation **Software Mode** (MODE_SEL =1) Output, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is present and cable length is below the MUTEREF threshold
MUTEREF	8	I, Analog	Mute reference input. Defines the cable length threshold at which the signal detect will be asserted. This pin can be left floating or can be grounded for maximum equalization.
xCS	9	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Must be set LOW for normal operation. **Software Mode** (MODE_SEL =1) Chip Select Complement (Internal pull up)
MF1	12	I/O, LVCMOS	**Hardware Mode** (MODE_SEL =0) Input, automatic sleep control. Sleep mode has precedence over MUTE and BYPASS. H: Automatic power down when no input is present L: Normal mode, the equalizer is always active **Software Mode** (MODE_SEL =1) 4-wire: Signal Out (Internal pull up)
MF2	14	I, LVCMOS	**Hardware Mode** (MODE_SEL =0) Input, output buffer MUTE control. MUTE has precedence over BYPASS. H: Outputs are muted L: Normal operation **Software Mode** (MODE_SEL =1) 4-wire: SCLK (Internal pull down)
MF3	15	I/O, LVCMOS	**Hardware Mode** (MODE_SEL =0) Output, Signal Detect Complement H: No input signal is present or the cable length is above the MUTEREF threshold L: Input signal is present and cable length is below the MUTEREF threshold **Software Mode** (MODE_SEL =1) 4-wire: Signal In (Internal pull down)

3.6 M31564 Package Information

The M31564 is packaged in a 4 mm x 4 mm footprint, 16-pin QFN SLP.

Figure 3-4. M31564 Packaging Drawing



4.0 Functional Descriptions

The M31544/64 devices are part of the next generation cable equalizer family for SDI video applications. They allow the transmission of data over 200 m Belden 1694A cable at 2.97 Gbps, 200 m at 1.485 Gbps and 400 m at 270 Mbps.

The equalizer has an integrated Automatic Rate Detect (ARD) circuit that allows the jitter cleaner to be enabled for HD and 3G data rates and will be automatically bypassed and turned off for SD rates providing additional power consumption savings. The jitter cleaner can provide retimed one or two serial data outputs with very low alignment jitter. In addition, the jitter cleaner does not need the traditional 27 MHz crystal reference clock.

The M31544/64 support limited configuration through hardware pin settings (Hardware Mode) or for additional configuration settings, a digital interface is also available (Software Mode).

Figure 4-1. M31544 Block Diagram

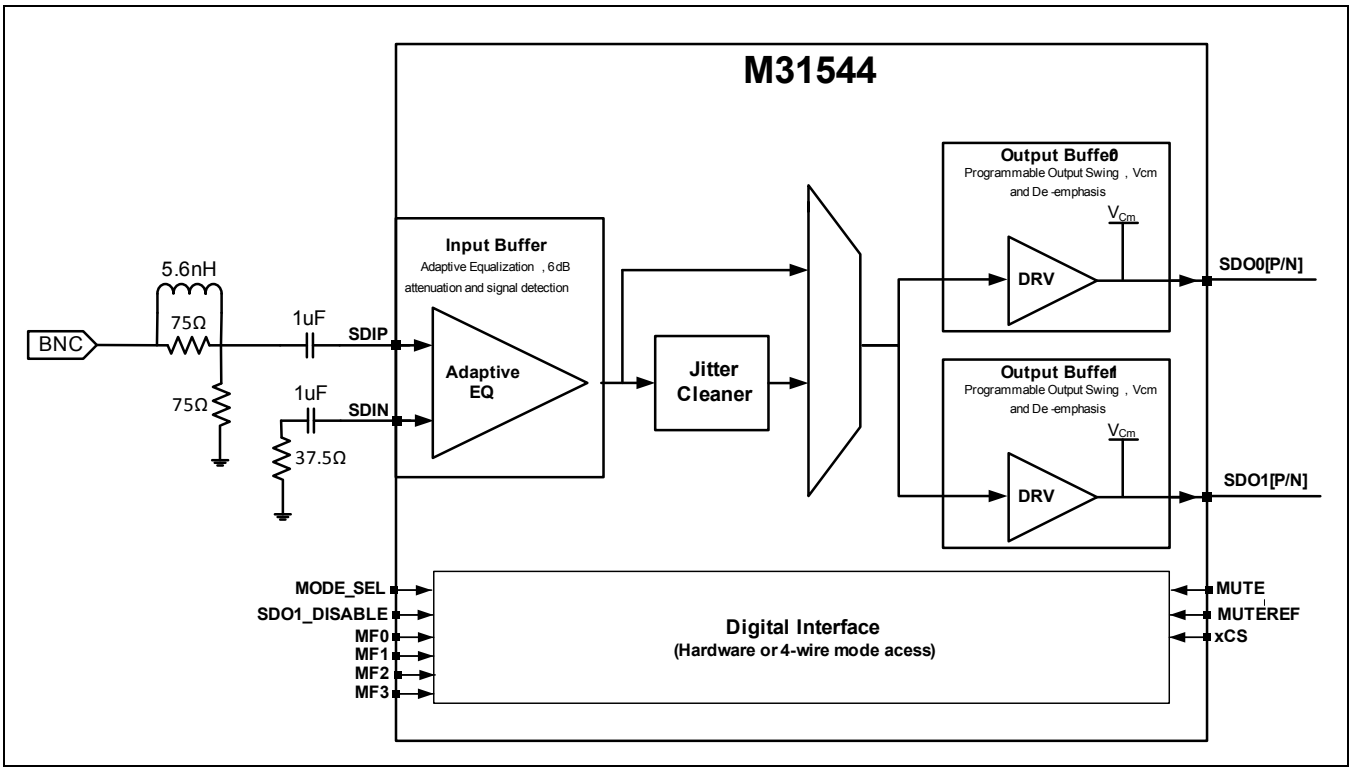
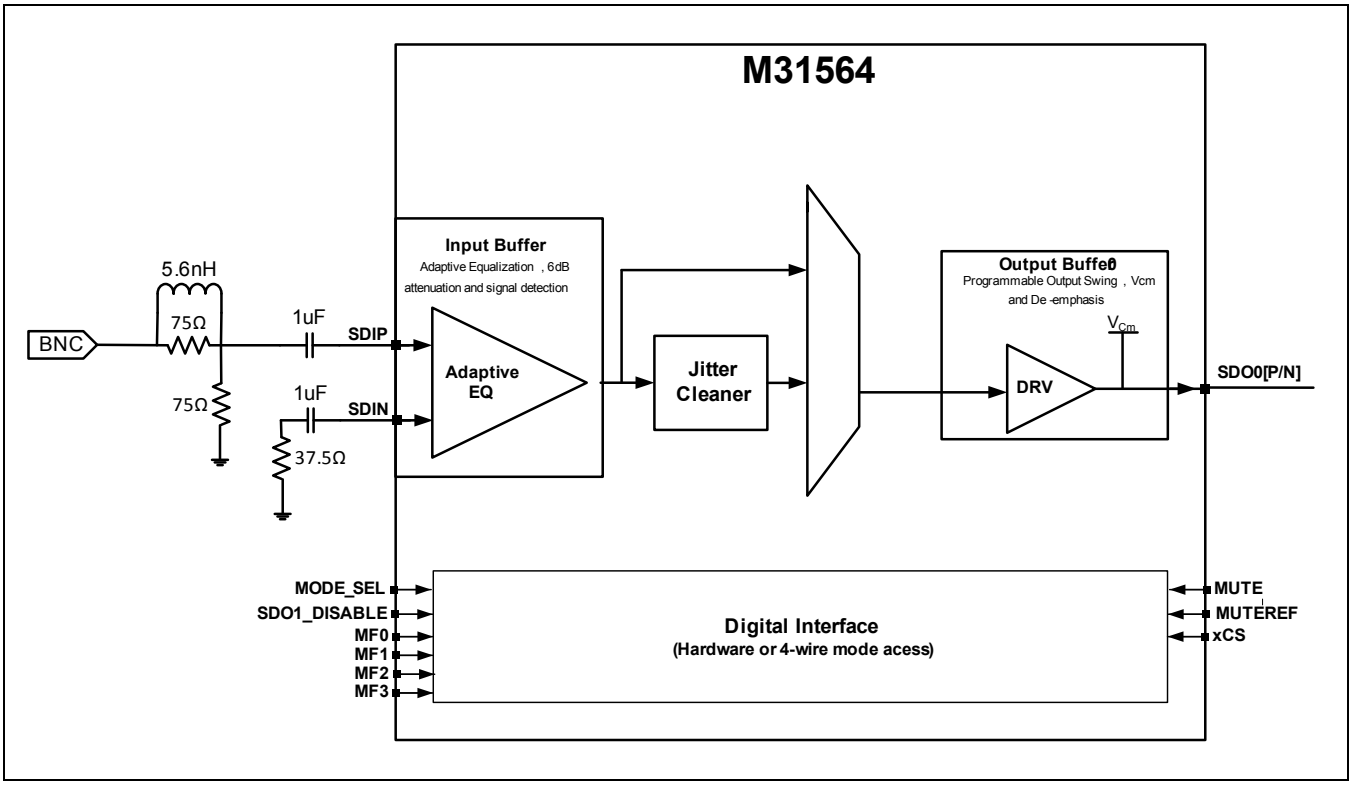


Figure 4-2. M31564 Block Diagram



4.1 High-Speed Input

Digital video coaxial cables are AC-coupled to the high-speed low-noise inputs (**SDIP/SDIN**). These are designed to operate in both single-ended or differential mode. The typical application is single-ended into the non-inverting **SDI** input with the inverting **SDI** input biased to match the bias on the input used.

The M31544/64 do not contain any internal input terminations and require both external input termination as well as the matching circuit to exceed the SMPTE input return loss specifications. The package and IC design have been optimized for high-speed performance, allowing them to exceed the SD/HD/3G SMPTE return loss specification.

For non-inverting single-ended operation, the recommended input circuit is shown in Figure 4-1. For differential operation, the matching/termination circuit on **SDIP** should be duplicated on **SDIN**.

4.1.1 Input Signal Detection

The high-speed input block offers a signal detect function that can be monitored either with pin.**MF3** or register.**GenConfig** bit[7]. The signal detect is also used to turn off the device if there is no signal present at the input. If desired, this function can be bypassed using register.**GenConfig** bit[4:3] or by setting pin.**MF1** = low in hardware mode.

4.1.2 Adaptive Equalizer

In typical hardware mode operation, the adaptive equalization is enabled with pin.**MF0** = Low (bypass disabled). However, with pin.**MF0**= High, the adaptive equalization and DC restore circuit are bypassed and the input is fed directly to the output buffers.

In software mode operation, the equalizer block can be bypassed by setting register.**GenConfig**.bit[5] to 1b.

The adaptive equalizer can be set to have a 6 dB gain for applications that have 400 mV_{PP} launch amplitude instead of 800 mV_{PP}. To have this 6 dB gain, register 00h bit[2] (**register.launch_ctrl**) must be set to 1b.

Once there is a signal detected at the input of the equalizer, the adaptive equalizer has the ability to report what length of Belden 1694A cable is being used. The cable length indicator results can be read on registers 05h bit[0] and register 06h bit[7:0]. The formulas to calculate the estimated cable length are:

CL(m) = 0.625*CLI, for 0-250 m

CL(m) = 2.5*(CLI - 400) + 250, for >250 m

where CLI is the decimal value of the 9 bits from registers 05h bit[0] (msb) and register 06h bit[7:0] (lsb) and CL is the estimated Belden 1694A cable length in meters. Table 4-1 has some of the decoded values for the cable length indicator registers.

Table 4-1. Cable Length Indicator Decoder

CLI Results	Estimated Cable Length*
000000000	0 m
000101000	25 m
001010000	50 m
001111000	75 m
010100000	100 m
011001000	125 m
011110000	150 m
100011000	175 m
101000000	200 m
101101000	225 m
110010000	250 m
110100100	300 m
110111000	350 m
111001100	400 m
111100000	450 m
* All cable length indicator values are approximate and are not guaranteed.	

4.1.3 Analog MUTEREF

The M31544/64 have a pin.**MUTEREF**, the voltage at this pin will set the cable reach threshold. For full cable reach, pin.**MUTEREF** should be left floating or grounded. For a typical application where a lower cable reach threshold is desired, pin.**xSD** and pin.**MUTE** could be connected together and the device will control the maximum cable length after which the outputs will mute forcing the equalizer outputs to logic zero.

The range for the pin.**MUTEREF** is 1.7V to 2.5V (AV_{DD}), its voltage ($V_{MUTEREF}$) can be calculated using the formula:

$$V_{MUTEREF} = V_{MUTEREF,max} - [\text{Cable Length (m)} * V_{MUTEREF,step}] \text{ in volts}$$

Where:

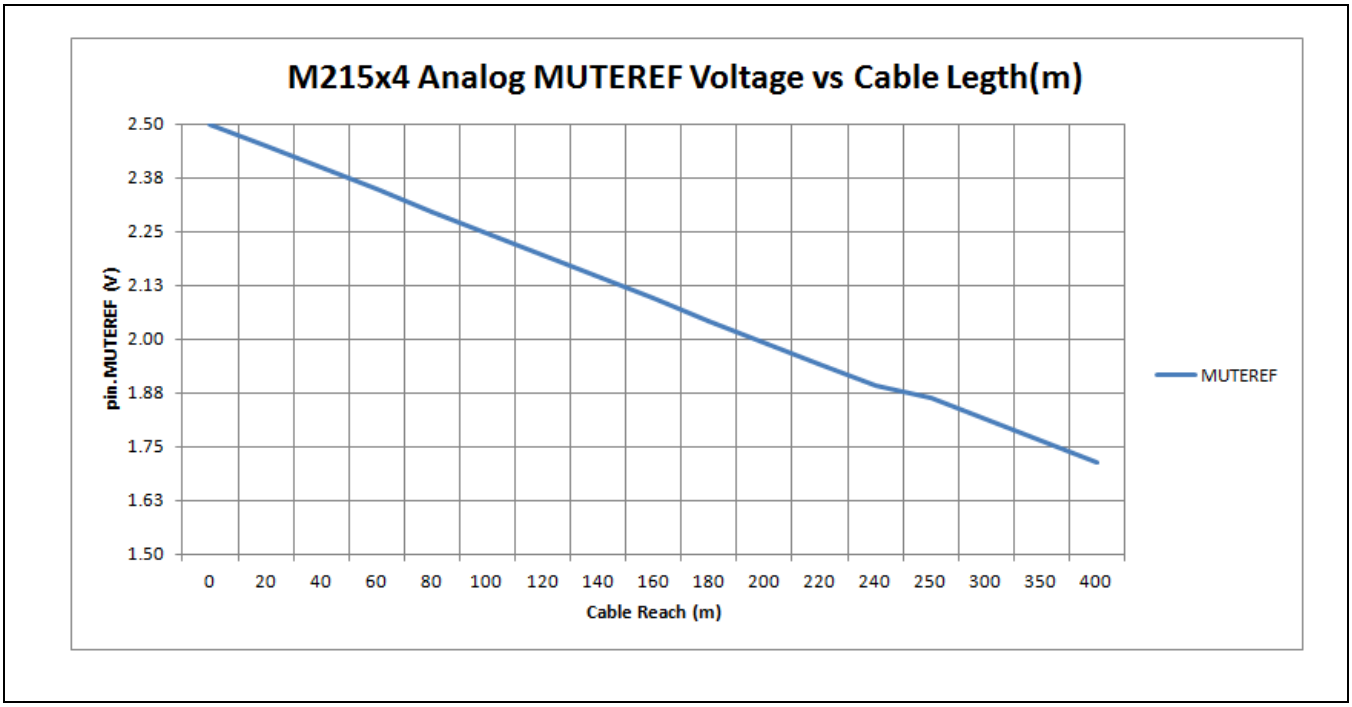
- $V_{MUTEREF,max}$ = 2.5V
- $V_{MUTEREF,step}$ = 12.7mV/5m, for cable lengths < 250m
  12.7mV/25m, for cable lengths > 250m

For example, for a cable length limit of 200m, we have:

$$V_{MUTEREF} = 2.5V - [200m * (0.0127/5)\ V/m] = 1.992V$$

Note: For HD and 3G data rates, 200m is the maximum cable length supported. For other voltages, refer to Figure 4-3.

Figure 4-3. M315x4 Analog MUTEREF Voltage vs. Cable Length



4.1.4 Digital MUTEREF

The digital mute reference allows to set the cable length limit without the need of external components to set a voltage at pin.**MUTEREF**. The digital mute reference is enabled by setting register 03h bit[7] to 1b. Mute will force the equalizer outputs to logic zero.

Table 4-2 Shows some of the different settings to set the appropriate cable length threshold

Table 4-2. Digital MUTE Decoder

Digital Mute Ref Setting Register 03h bit[6:2]	Cable Length Threshold
00000b	Mute when cable is > 10m
00010b	Mute when cable is > 25m
00101b	Mute when cable is > 50m
00111b	Mute when cable is > 75m
01010b	Mute when cable is > 100m
01100b	Mute when cable is > 125m
01111b	Mute when cable is > 150m
10001b	Mute when cable is > 175m
10100b	Mute when cable is > 200m
11001b	Mute when cable is > 250m
11010b	Mute when cable is > 300m
11011b	Mute when cable is > 350m
11100b	Mute when cable is > 400m
11110b	Mute when cable is > 450m
11111b	Never Mute

Notes:
- All cable length threshold values are approximate and are not guaranteed.
- For HD and 3G data rates, 200m is the maximum cable length supported

4.1.5 6 dB Attenuation

The M31544/64 provide an option to compensate for 6 dB of flat attenuation in applications where the launch amplitude is a lot lower than 800 mV_{PPD}. When the expected launch amplitude is between ~300 mV_{PPD} and ~500 mV_{PPD}, setting register.**GenConfig**,bit[2] to 1b will improve the equalizer's performance especially for SD rates. For HD and 3G rates, having the jitter cleaner enabled will result in the best performance in addition to the 6 dB compensation.

4.2 Jitter Cleaner

The jitter cleaner on the M31544/64 is functional only for HD and 3G video data rates and will be automatically bypassed and turned off for SD rates providing additional power consumption savings.

The jitter cleaner features an Automatic Rate Detector (ARD) circuit that monitors the input signal rate and automatically sets the Jitter Cleaner to the correct video rate. The data rate determined by the ARD block may be read from register.**JitCleaner**,bit[7:6].

Table 4-3. Jitter Cleaner Data Rate Detector

Register.JitCleaner,bit[7:6]	Data Rate Detected
00b	SD
01b	HD
10b	3G
11b	HD or 3G (used when the Jitter cleaner is bypassed)

The jitter cleaner is always in auto-bypass mode. If the ARD cannot determine the rate of the input data stream, it will switch the Jitter Cleaner into bypass mode. This allows a data rate other than those specified to be passed through the Jitter Cleaner.

4.3 High-Speed Outputs

The high-speed LVDS differential outputs after equalization are made available on the pin.**SDO0[P/N]** and pin.**SDO1[P/N]** pins. Note that the M31564 has only one output available, pin.**SDO0[P/N]**.

There are three output swings available - 400 mV_{PP}, 600 mV_{PP} (default) and 800 mV_{PP}. The output swing levels can only be controlled via register.**Driver**[1:0].bit[7:6].

In addition to controlling the output swing, the common mode voltage (V_{CM}), can also be modified to Auto mode for low common mode DC impedance, 0.8 V, 1.0 V or 1.2 V(default) by programming the desired value to register.**Driver**[1:0].bit[5:4]. When the output driver is set to have automatic common mode voltage, it will sense the downstream device input common mode and it will match it. Note, the maximum common mode voltage is 1.2 V.

In order to improve signal integrity when used in large systems, each output also comes equipped with programmable de-emphasis (DE) for FR4 traces. There are four settings for output de-emphasis: 0 dB (or no DE), 2 dB, 4 dB, and 6 dB. In software mode, the output de-emphasis level for each output may be set by programming the desired value to register.**Driver**[1:0].bit[3:1].

4.4 Control Modes

The M31544/64 may be configured in two separate control modes. The control mode is determined by the setting of the MODE_SEL pin as shown in Table 4-4 below.

Table 4-4. Control Mode Setting

MODE_SEL	Control Mode
L	Hardware Mode
H	Software Mode (4-wire digital interface)

4.4.1 Hardware Mode

Configuring the M31544/64 in hardware mode avoids the complication of adding a microcontroller, but offers limited control options. When in hardware mode, the MF (Multi Function IO) pins are configured as shown in Table 4-5 below.

Table 4-5. MF Pin Configuration in Hardware Mode (MODE_SEL = 0)

Pin Name	Hardware Mode Pin Name	Function
MF0	BYPASS	EQ and Jitter Cleaner bypass*
MF1	AUTOSLEEP	Power down EQ when no input signal is present
MF2	MUTE	Output mute
MF3	Signal Detect Complement	Input signal detect
* Please see pin descriptions for more details.		

4.4.2 Software Mode (4-wire Digital Interface Access)

In this mode, a four-wire serial interface is used to program the device's internal registers, configuring the operation of the M31544/64. When in software mode, MF[3:0] pins comprise the four-wire bus as well as additional diagnostics as shown in Table 4-6 below.

Table 4-6. MF Pin Configuration in Software mode (4-wire Interface Mode, MODE_SEL = 1)

Pin Name	4-Wire Mode Pin Name	Function
MF0	Signal Detect Complement	Input signal detect
MF1	SO	Serial Data Output
MF2	SCK	Serial Data Clock
MF3	SI	Serial Data Input
xCS	xCS	Chip Select (Active Low)

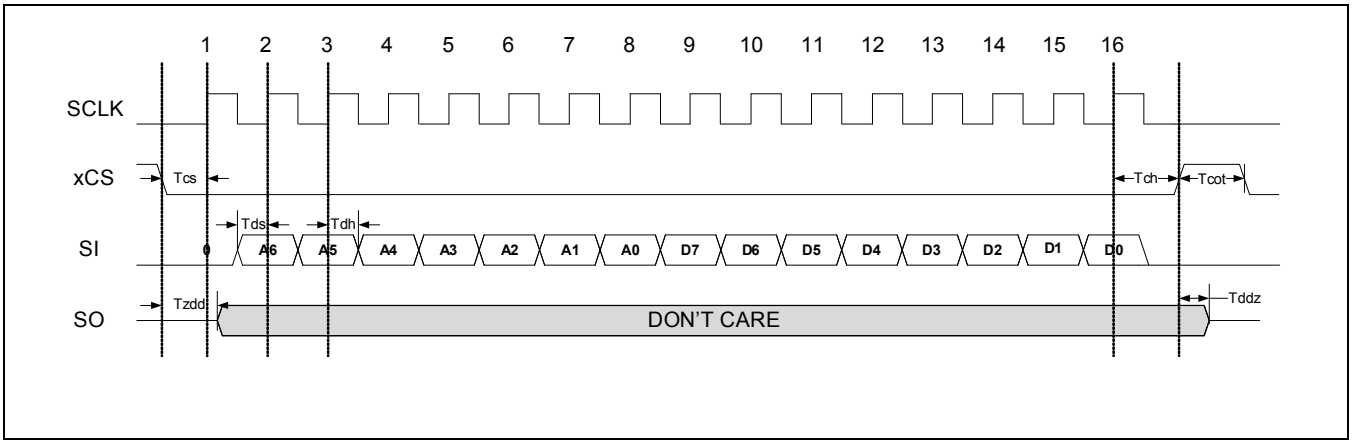
4.5 Digital Interface

The 4-wire serial interface is selected with pin.**MODE_SEL** =H. The M31544/64 serial interface supports daisy chain mode in order to control several devices.

4.5.1 4-Wire Serial Write

Figure 4-4 Illustrates the Serial Write Mode. To initiate the 16-bit long write sequence, **xCS** is driven low before the rising edge of **SCLK.** On each rising edge of the clock, the 16 bits consisting of R/xW = 0 for write, ADDR (7-bit) and DATA (8-bit), are latched into the input shift register through **SI**. After the last data bit is sent, **xCS** must be driven high to complete the write operation.

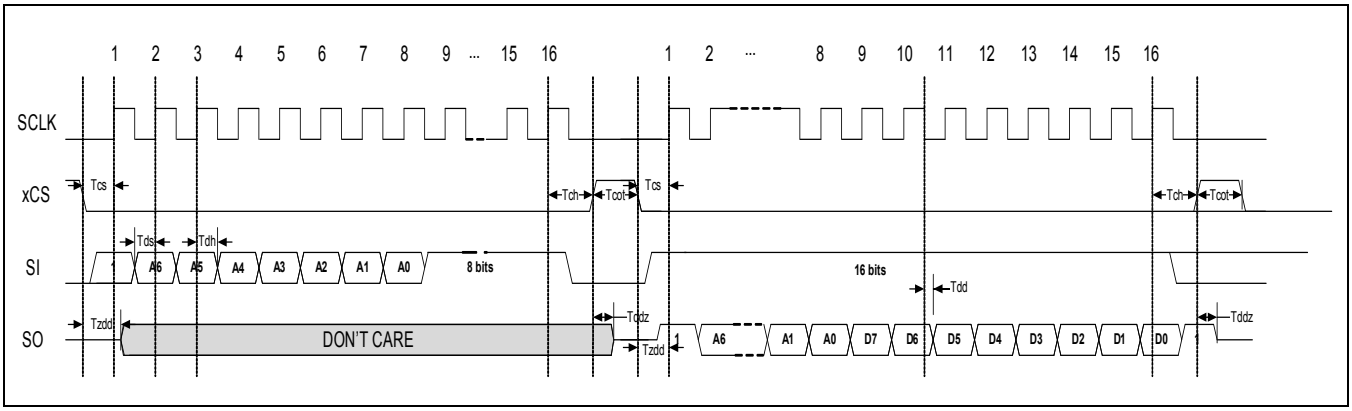
Figure 4-4. 4-wire Serial WRITE Timing Diagram



4.5.2 4-Wire Serial Read

Figure 4-5 Illustrates the Serial Read Mode. To initiate the 32-bit long read sequence, **xCS** is driven low before the rising edge of **SCLK.** On each rising edge of the clock, the first16 bits consisting of R/xW = 1 for read, ADDR (7-bit) and dummy DATA (8 x “1” bits), are latched into the input shift register through **SI**. After the 16th bit is sent, **xCS** must be toggled to start the second part of the operation. The second set of 16 x “1” bits are latched into the input shift register through **SI** while the register address and data requested in the first part of the read transaction are shifted out on **SO** on the failing edge of the clock. Finally, **xCS** must be driven high to complete the read operation.

Figure 4-5. 4-wire Serial READ Timing Diagram

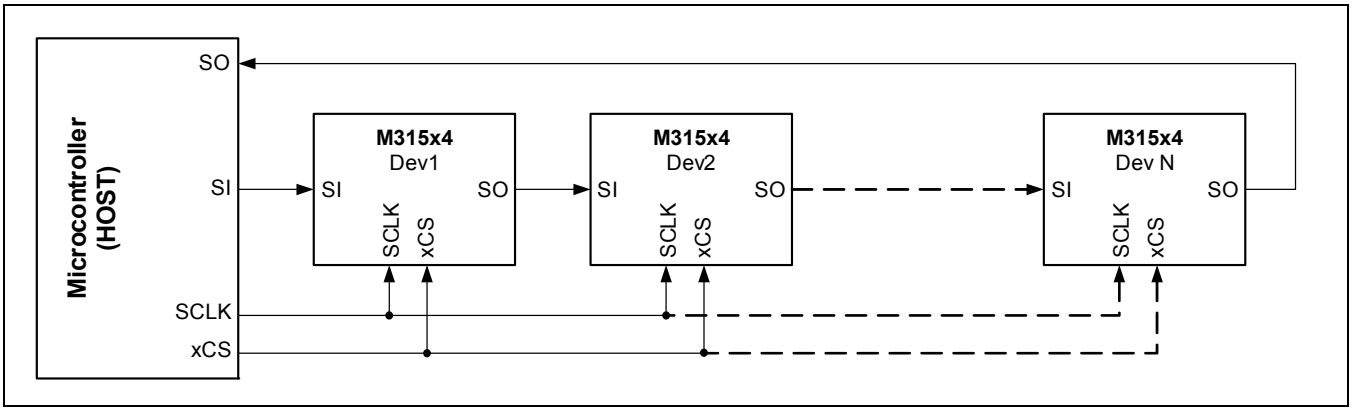


4.5.3 4-Wire Serial Interface Daisy Chain

The M31544/64 4-Wire interface supports daisy chain for an unlimited number of devices as shown in Figure 4-6.

Daisy chain operation provides an architectural advantage in that only one **xCS** and **SCLK** pin is required on the host, as well as one **SO** and one **SI** pin irrespective of the number of devices. The **SO** data of each device shifts into the next device **SI**.

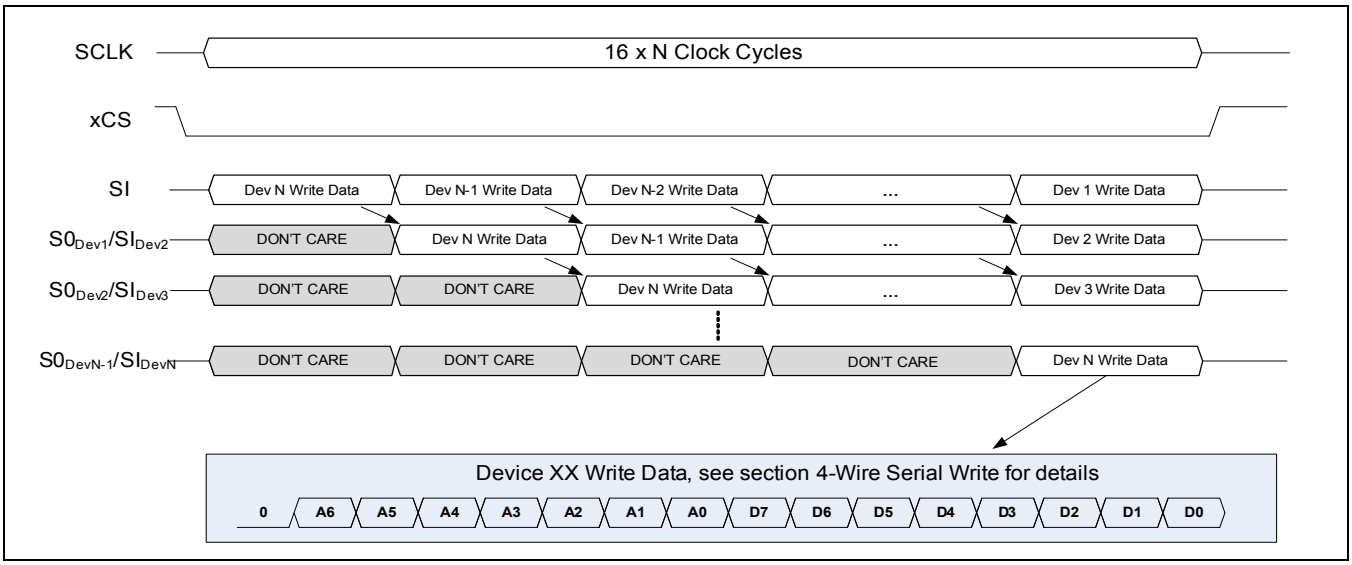
Figure 4-6. 4-wire Serial Interface, Daisy Chain Configuration



4.5.3.1 4-Wire Serial Interface Daisy Chain - Write

Figure 4-7 Illustrates the 4-Wire serial write operation for a daisy chain architecture consisting of N devices. To initiate the (16 x N)-bit long write sequence, **xCS** is driven low before the first rising edge of **SCLK.** The difference in the daisy chain configuration is that **xCS** remains low for (16 x N) clock cycles, where the 16-bit write operation block consists of R/xW = 0 for write, ADDR (7-bit) and DATA (8-bit) as described in **Section 4.5.1**. At the beginning of the last 16-bit block, each device receives the appropriate data to be written on its register table. Finally, **xCS** must be driven high to complete the write operation.

Figure 4-7. 4-wire Serial Interface, Daisy Chain Write



4.5.3.2 4-Wire Serial Interface Daisy Chain - Read

Figure 4-8 Illustrates the 4-Wire serial read operation for a daisy chain architecture consisting of N devices. To initiate the (32 x N)-bit long read sequence, **xCS** is driven low before the first rising edge of **SCLK.** The difference in the daisy chain configuration is that **xCS** remains low for (16 x N) clock cycles to send the appropriate read data to each device, where the 16-bit read operation block consists of R/xW = 1 for read, ADDR (7-bit) and DATA (8-bit) as described in **Section 4.5.2.**

The second set of (16 x N) "1" bits are latched into the input shift register through **SI** while the register address and data requested in the first part of the read transaction are shifted out on **SO.** Finally, **xCS** must be driven high to complete the write operation.

Figure 4-8. 4-wire Serial Interface, Daisy Chain Write

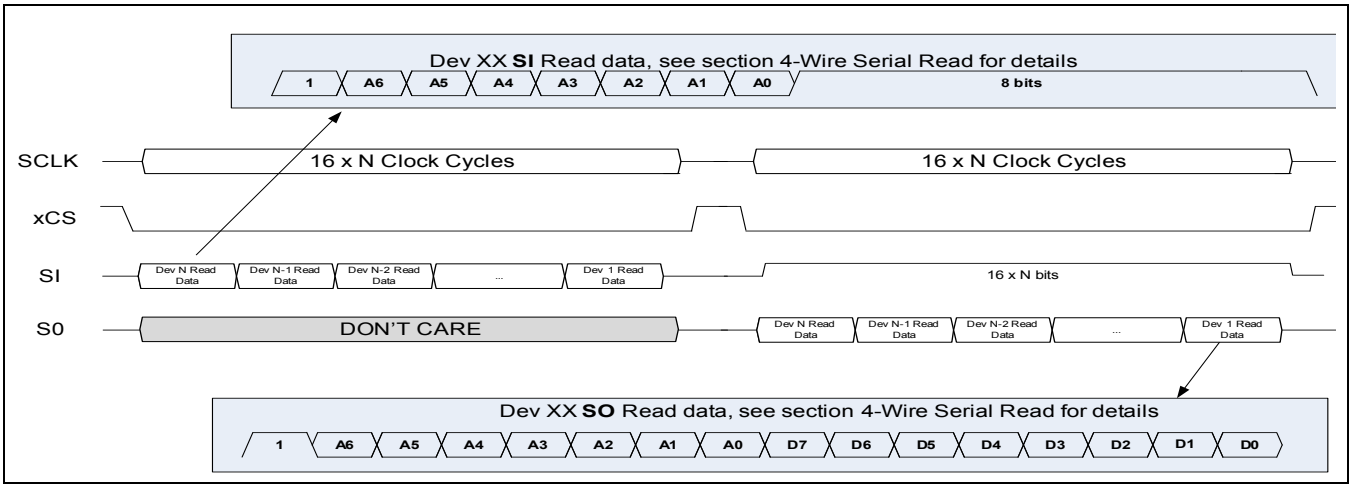


Table 4-7. 4-wire Serial Interface Specifications

Timing Symbol	Description		Min	Max	Unit
T_{FREQW}	4-Wire clock Frequency	Stand Alone Mode	1	20	MHz
		Daisy Chain Mode	1	15	
T_{DCD}	SCLK pulse width		40	60	%
Tds	SI Data set-up time (SCLK↑).		4	—	ns
Tdh	SI Data hold time (SCLK↑).		4	—	ns
Tcs	xCS set-up time (from xCS↓ to SCLK↑).		14	—	ns
Tch	xCS hold time (from xCS↑ to SCLK↑).		4	—	ns
Tcot	xCS off time (from xCS↑ to xCS↓). In addition, the following restrictions apply: • Between consecutive write commands to the same register • After a write command to register 00h (reset) • Between the two 16-bit frames of a read command for registers 00h, 04h, 05h and 06h		1 6 8 6	— — — —	$1/T_{FREQW}$ us us us
Tzdd	SO Read data output delay, Tri-State to Active (xCS↓)		—	16	ns
Tddz	SO Read data output delay, Active to Tri-State (xCS↑)		—	20	ns
Tdd	SO Read data output delay from SCLK↓		—	24	ns

5.0 Control Register Descriptions

Table 5-1. Register Summary

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
00h	GenConfig	signal_det	mute	bypass	sleep mode		lanch_ctrl	master_rst	acq_rst	08'h	R/W
01h	Driver0	output_swing0		offset_voltage0		de_emphasis0			Reserved	B0'h	R/W
02h	Driver1	output_swing1		offset_voltage1		de_emphasis1			Reserved	B0'h	R/W
03h	Misc	mutemode	digital_muteref					Reserved	jc_bypass	7C'h	R/W
04h	JitCleaner	rate_indicator		Reserved		die_rev				80'h	R
05h	Cable_Len1	Reserved							CLI_bit[8]	na	R
06h	Cable_Len0	CLI_bit[7:0]								na	R

5.1 Address Register Description

Address: 00h
Register Name: GenConfig
Default Value: 08'h
Description: General Configuration Register

Bit(s)	Name	Description	Default	Type
7	signal_det	0b: No Signal detected 1b: Signal detected		R
6	mute	0b: Normal operation 1b: Equalizer muted	0b	R/W
5	bypass	0b: Normal operation 1b: Equalizer bypassed	0b	R/W
[4:3]	sleep_mode	00b: Forced enable of the equalizer 01b: Power down when no input signal detected 10b: Forced power down of the equalizer 11b: Reserved	01b	R/W
2	launch_ctrl	0b: Equalizer expects 800 mV launch 1b: Equalizer expects 400 mV (6 dB attenuation)	0b	R/W
1	master_rst	0b: No reset 1b: Reset of registers and state machine (self clearing)	0b	R/W
0	acq_rst	0b: No reset 1b: Reset state machine only (self clearing)	0b	R/W

Address: 01h
Register Name: Driver0
Default Value: B0'h
Description: Output Driver 0 Configuration Register

Bit(s)	Name	Description	Default	Type
[7:6]	output_swing	00b: Power down of driver 0 01b: 400 mV differential peak to peak swing 10b: 600 mV differential peak to peak swing 11b: 800 mV differential peak to peak swing	10b	R/W
[5:4]	offset_voltage	00b: Auto mode to drive a receiver presenting a low common mode DC impedance 01b: 0.8 V output common mode 10b: 1 V output common mode 11b: 1.2 V output common mode	11b	R/W
[3:1]	de_emphasis	000b: De-emphasis disable 001b: 2 dB de-emphasis 011b: 4 dB de-emphasis 101b: 6 dB de-emphasis 111b: 8 dB de-emphasis	000b	R/W
0	Reserved	Reserved (set to default)	0b	R/W

Address: 02h
Register Name: Driver1
Default Value: B0'h
Description: Output Driver1 Configuration Register

Bit(s)	Name	Description	Default	Type
[7:6]	output_swing	00b: Power down of driver 1 01b: 400 mV differential peak to peak swing 10b: 600 mV differential peak to peak swing 11b: 800 mV differential peak to peak swing	10b	R/W
[5:4]	offset_voltage	00b: Auto mode to drive a receiver presenting a low common mode DC impedance 01b: 0.8 V output common mode 10b: 1 V output common mode 11b: 1.2 V output common mode	11b	R/W
[3:1]	de_emphasis	000b: De-emphasis disable 001b: 2 dB de-emphasis 011b: 4 dB de-emphasis 101b: 6 dB de-emphasis 111b: 8 dB de-emphasis	000b	R/W
0	Reserved	Reserved (set to default)	0b	R/W

Address: 03h
Register Name: Misc
Default Value: 7C'h
Description: MuteRef Configuration and Jitter Cleaner Bypass Register

Bit(s)	Name	Description	Default	Type
7	muteref_mode	0b: Analog MuteRef with external pin voltage 1b: Digital MuteRef	0b	R/W
[6:2]	digital_muteref	0 0000b: Mute when cable > 10 m 0 0010b: Mute when cable > 25 m … 0 1010b: Mute when cable > 100 m 0 1100b: Mute when cable > 125 m 0 1111b: Mute when cable > 150 m 1 0001b: Mute when cable > 175 m 1 0100b: Mute when cable > 200 m … 1 1001b: Mute when cable > 250 m 1 1010b: Mute when cable > 300 m 1 1011b: Mute when cable > 350 m 1 1100b: Mute when cable > 400 m 1 1110b: Mute when cable > 450 m 1 1111b: Never mute	1 1111b	R/W
1	Reserved	Reserved (set to default)	0b	R/W
0	jc_bypass	0b: Jitter cleaner active 1b: Jitter cleaner bypassed	0b	R/W

Address: 04h
Register Name: JitCleaner
Default Value: 00'h
Description: Jitter Cleaner Configuration and Status Register

Bit(s)	Name	Description	Default	Type
[7:6]	rate_indicator	00b: SD rate 01b: 1.5 Gbps 10b: 3 Gbps 11b: HD rates (1.5 Gbps or 3 Gbps)	00b	R
[5:4]	Reserved	Reserved	00b	R/W
[3:0]	die_rev	0000b: Die revision	0001b	R

Address: 05h
Register Name: Cable_Len1
Default Value: na

Description: Adaptation Results of Equalizer

Bit(s)	Name	Description	Default	Type
[7:1]	Reserved	Reserved (set to default)	0b	R
0	CLI_bit[8]	Cable_length_ind[8]. Bit 8 of the cable length indication	NA	R

Address: 06h
Register Name: Cable_Len0
Default Value: na
Description: Adaptation Results of Equalizer

Bit(s)	Name	Description	Default	Type
[7:0]	CLI_bit[7:0]	Cable_length[7:0]. Bits [7:0] of the cable length indication	NA	R

NOTES:

1. A numerical value of 0 corresponds to the shortest cable. The maximum value allowed for the cable length indicator is 101111011.

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