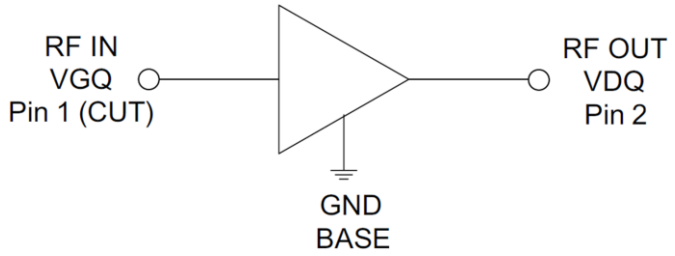
RFHA1043

150W GaN Power Amplifier
1.2GHz to 1.85GHz

The RFHA1043 is optimized for applications in the 1.2GHz to 1.85GHz frequency band. Using an advanced 48V high power density gallium nitride (GaN) semiconductor process optimized for high peak to average ratio applications, these high performance amplifiers achieve high efficiency and flat gain over a broad frequency range in a single amplifier design. The RFHA1043 is an input matched GaN transistor packaged in an air cavity ceramic package, which provides excellent thermal stability. Ease of integration is accomplished through the incorporation of simple optimized matching networks external to the package that provide wideband gain, efficiency, and linearizable performance in a single amplifier.



Functional Block Diagram

Ordering Information

RFHA1043S2	Sample bag with 2 pieces
RFHA1043SB	Bag with 5 pieces
RFHA1043SQ	Bag with 25 pieces
RFHA1043SR	Short reel with 50 pieces
RFHA1043TR13	13” Reel with 300 pieces
RFHA1043PCBA-410	Fully assembled evaluation board

Package: Flanged Ceramic, 2 pin, RF400-2

Features

- Advanced GaN HEMT Technology
- Peak Power 150W
- Advanced Heat-Sink Technology
- Single Circuit for 1.2GHz to 1.85GHz
- 48V Modulated Typical Performance
  - P_{OUT} 45.2dBm
  - Gain 15.5dB
  - Drain Efficiency 30%
  - ACP-30dBc
- 48V CW Typical Broadband Performance
  - P_{OUT} 52dBm
  - Gain 13.5dB
  - Drain Efficiency 51%
- -40°C to 85°C Operating Temperature
- Optimized for Video Bandwidth and Minimized Memory Effects
- Large Signal Models Available

Applications

- Civilian and Military Radar
- Public Mobile Radios
- Industrial, Scientific, and Medical

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS131023

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to 2	V
Gate Current (I_D)	105	mA
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_L)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C, 95% Confidence Limits)*	1.8E + 07	Hours
MTTF (T_J < 250°C, 95% Confidence Limits)*	1.1E + 05	Hours
Thermal Resistance, Rth (junction to case) measured at T_C = 85°C, DC bias only	1.4	°C/W
Thermal Resistance, Rth (junction to case) measured at T_C = 85°C, CW	1.27	°C/W

Caution! ESD sensitive device.

RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, <1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

* MTTF – median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT (random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table above.

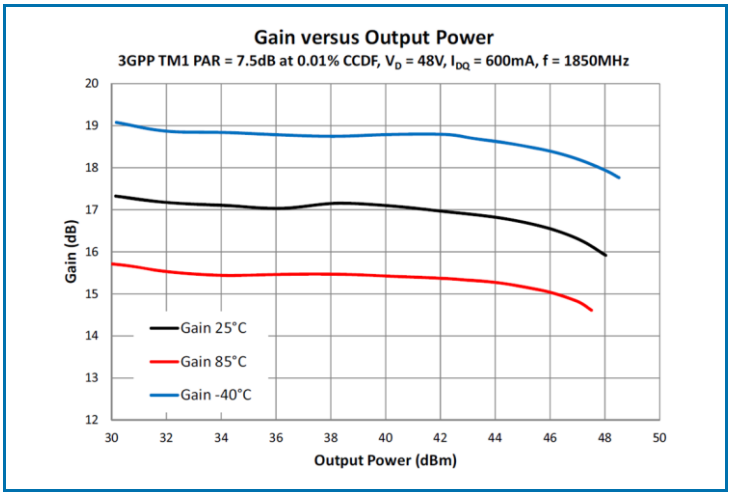
Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH\ J\text{-}C}$ and $T_C = T_{CASE}$

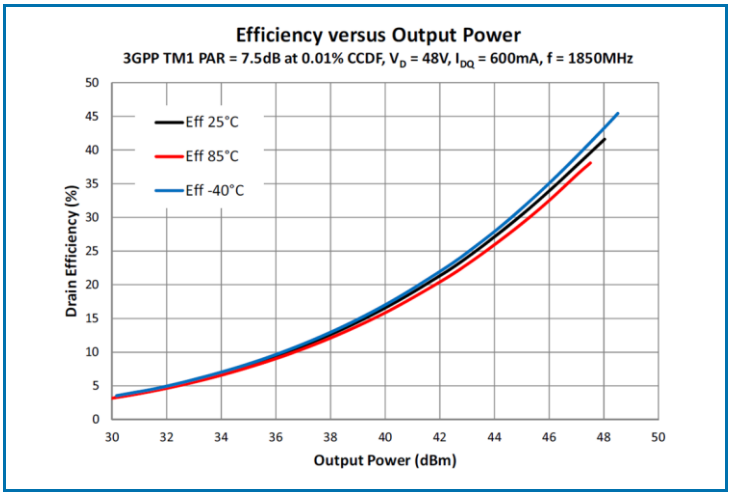
Nominal Operating Parameters

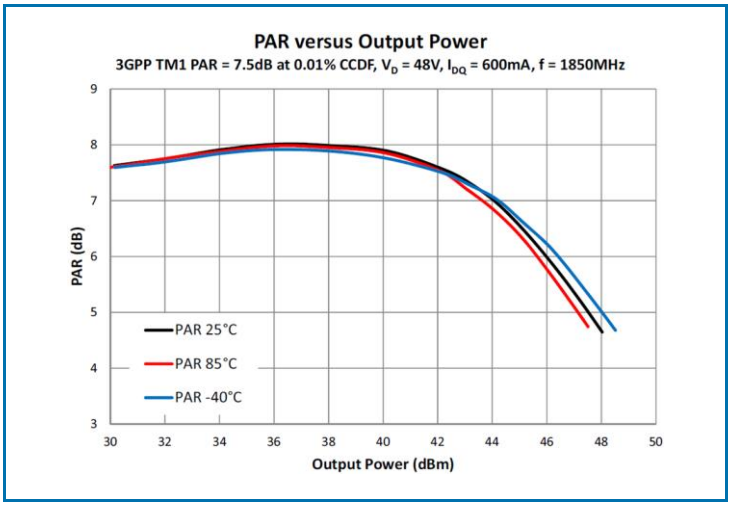
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})		48		V	
Gate Voltage (V_{GSQ})	-4.5	-3.2	-2.5	V	
Drain Bias Current		600		mA	
Frequency of Operation	1.2		1.85	GHz	
DC Functional Test					
$I_{G(OFF)}$ – Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D(OFF)}$ – Drain Leakage			2.5	mA	V_G = -8V, V_D = 48V
$V_{GS(TH)}$ – Threshold Voltage		-3.5		V	V_D = 48V, I_D = 28mA
$V_{DS(ON)}$ – Drain Voltage at High Current		0.215		V	V_G = 0V, I_D = 1.5A

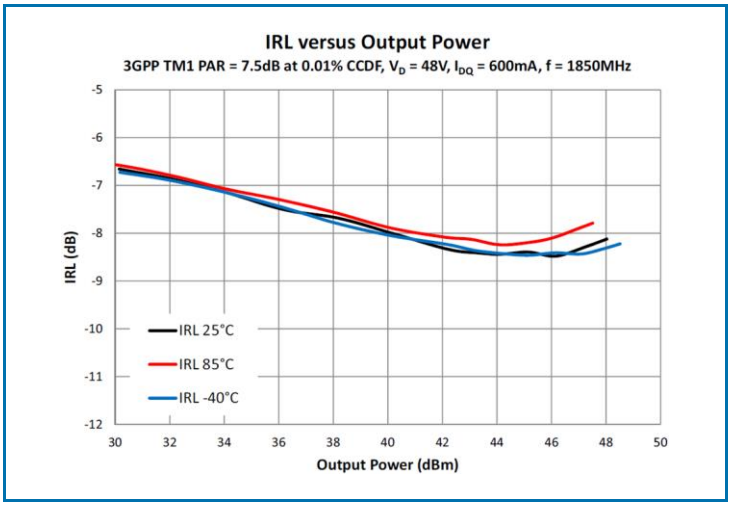
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Capacitance					
C_{RSS}		11.6		pF	V_G = -8V, V_D = 0V
C_{ISS}		109		pF	
C_{OSS}		29.8		pF	
RF Functional Test					**Test Conditions: V_{DSQ} = 48V, I_{DQ} = 600mA, T = 25°C, Performance in a standard tuned test fixture, ACP: ±1.23MHz at 1.5MHz BW**
$V_{GS(Q)}$		-3.2		V	V_D = 48V, I_D = 600mA
Gain	13	15.6		dB	IS95 (9 channel model, 9.8dB PAR at 0.01% CCDF), P_{OUT} = 46dBm, f = 1.85GHz
Drain Efficiency	30	35		%	
Input Return Loss		-6.5	-3	dB	
PAR	6	6.7		d**B**	
RF Typical Performance					**Test Conditions: V_{DSQ} = 48V, I_{DQ} = 600mA, T = 25°C, Performance in a standard tuned test fixture, ACP: ±1.23MHz at 1.5MHz BW**
Gain		15.8		dB	3GPP (TM1, 7.5dB PAR at 0.01% CCDF), P_{OUT} = 45dBm, f = 1.85GHz
Drain Efficiency		30		%	
Input Return Loss		-6.8		dB	
Adjacent Channel Power		-37		dBc	
Power Gain at P3dB		13.6		dB	CW, P_{OUT} = 52dBm, f = 1.85GHz
Output Power at P3dB		52		dBm	
Drain Efficiency at P3dB		54		%	

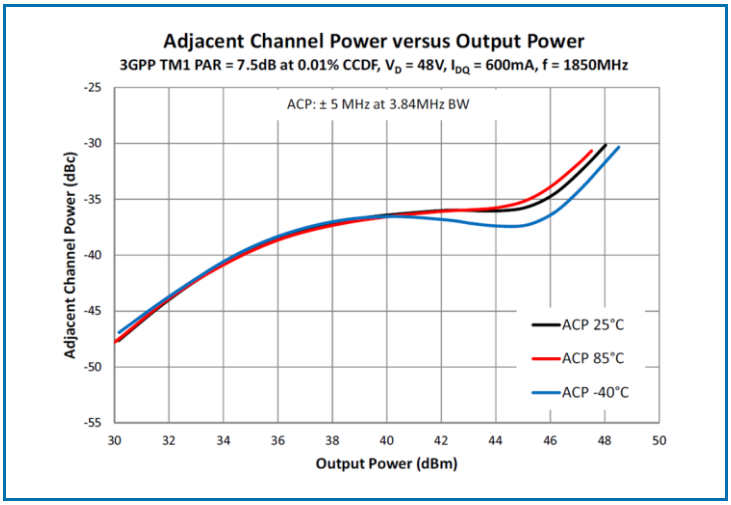
Typical Performance in Fixed Tuned Test Fixture: (T = 25°C unless noted)

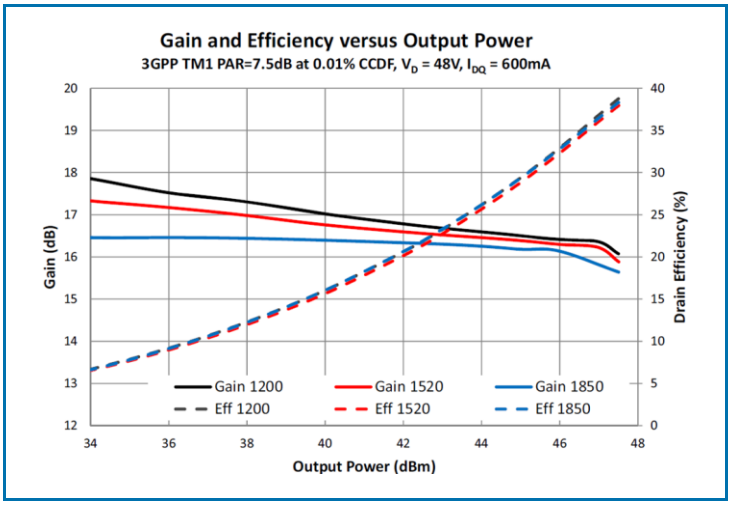




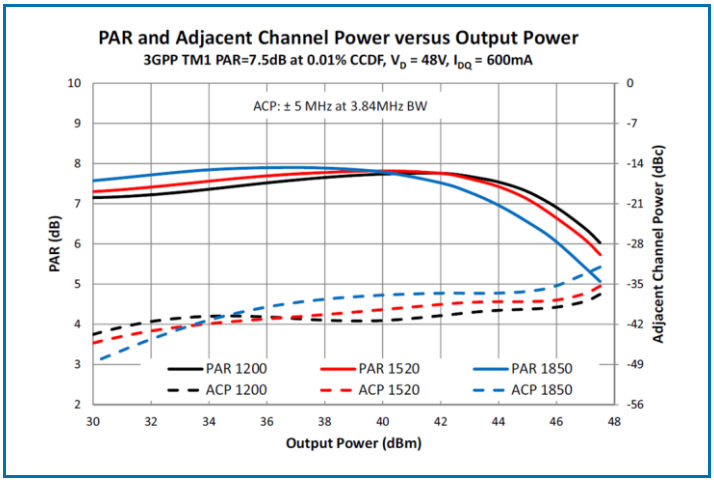


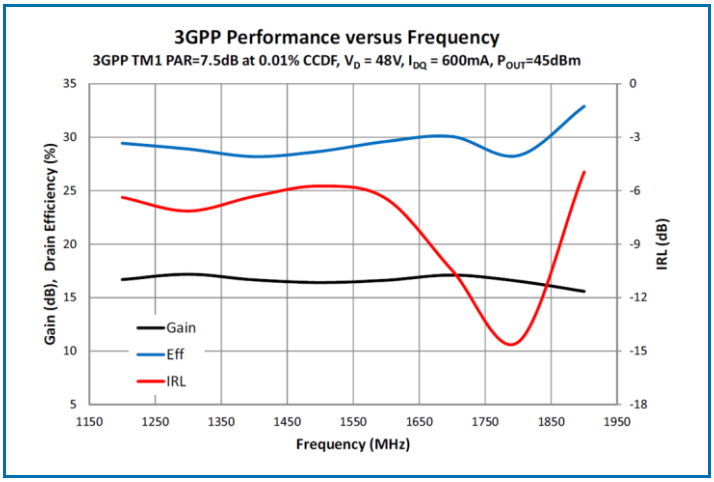


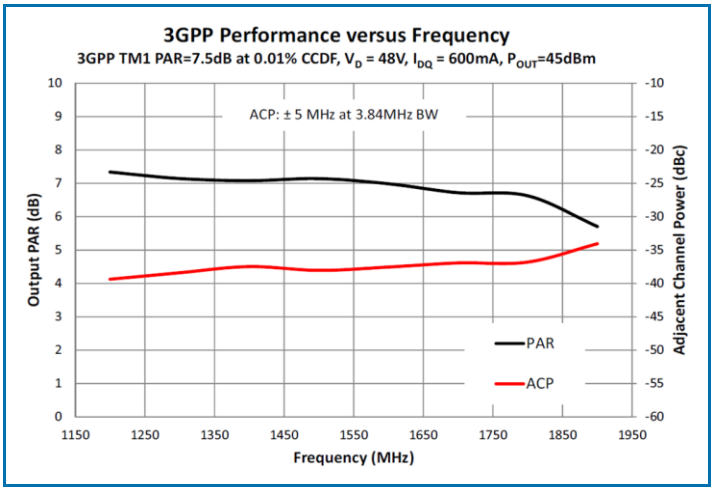


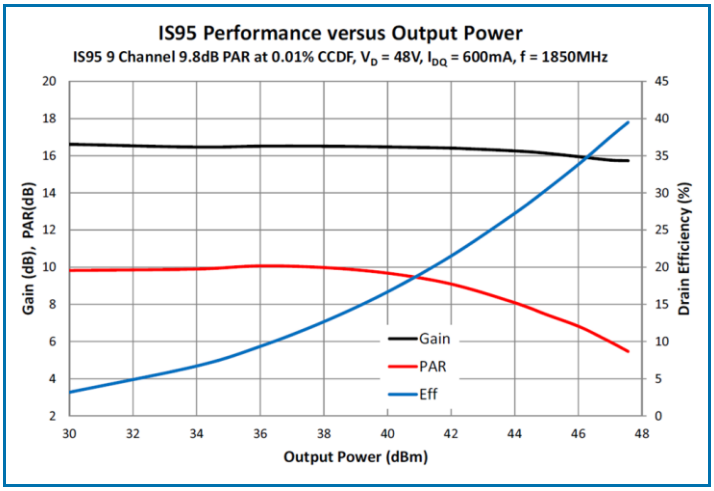


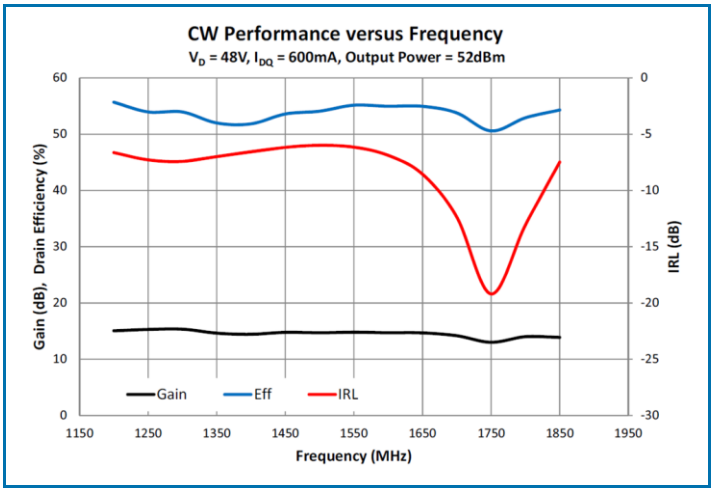
Typical Performance in Fixed Tuned Test Fixture: (T = 25°C unless noted) (continued)

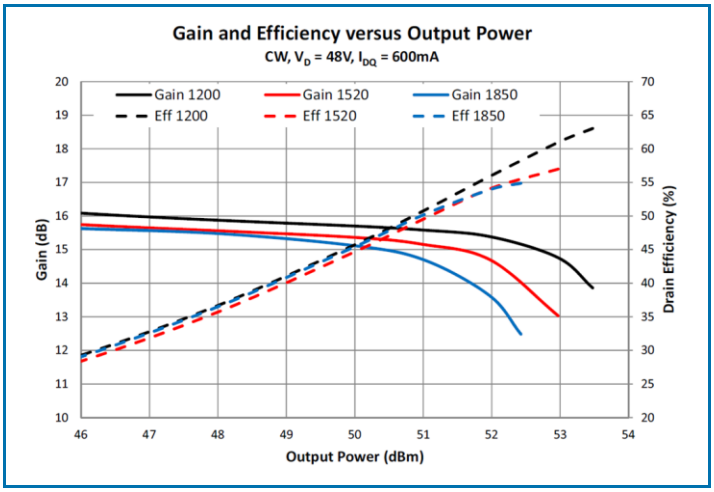




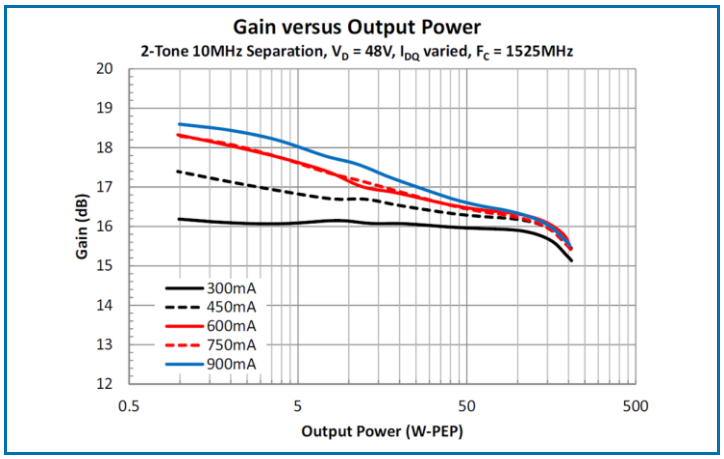


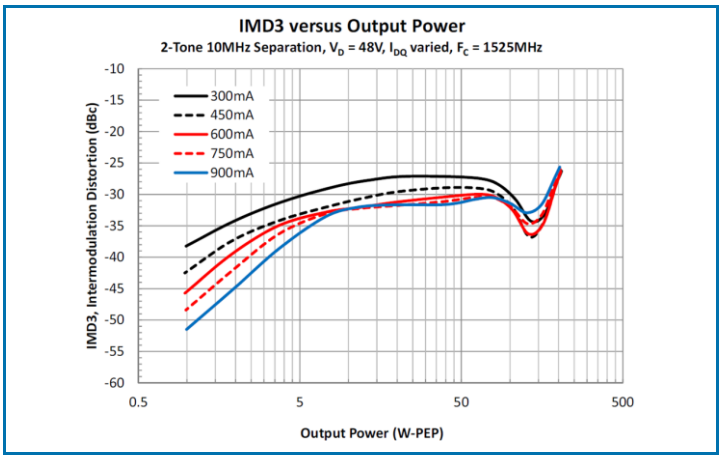


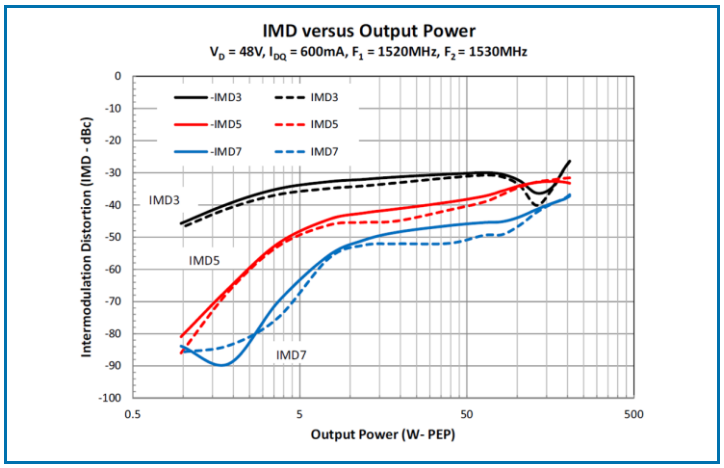


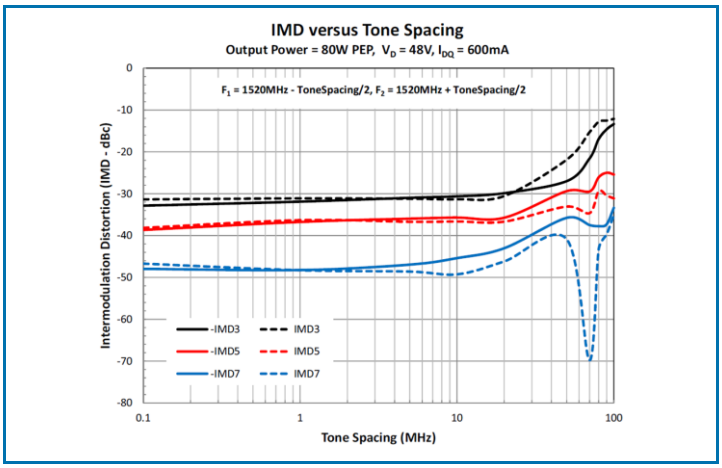


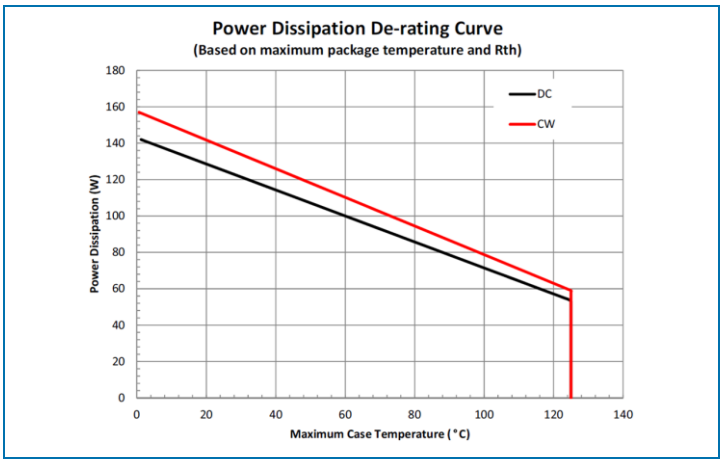
Typical Performance in Fixed Tuned Test Fixture: (T = 25°C unless noted) (continued)



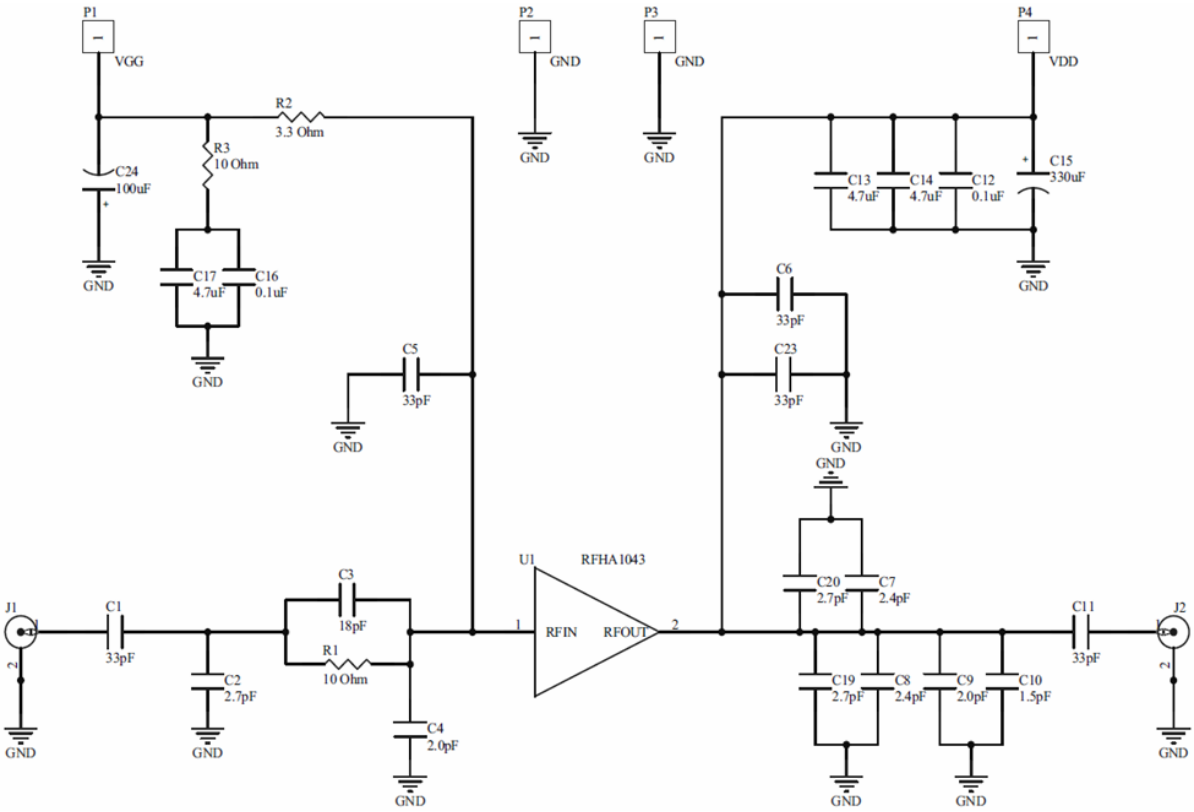








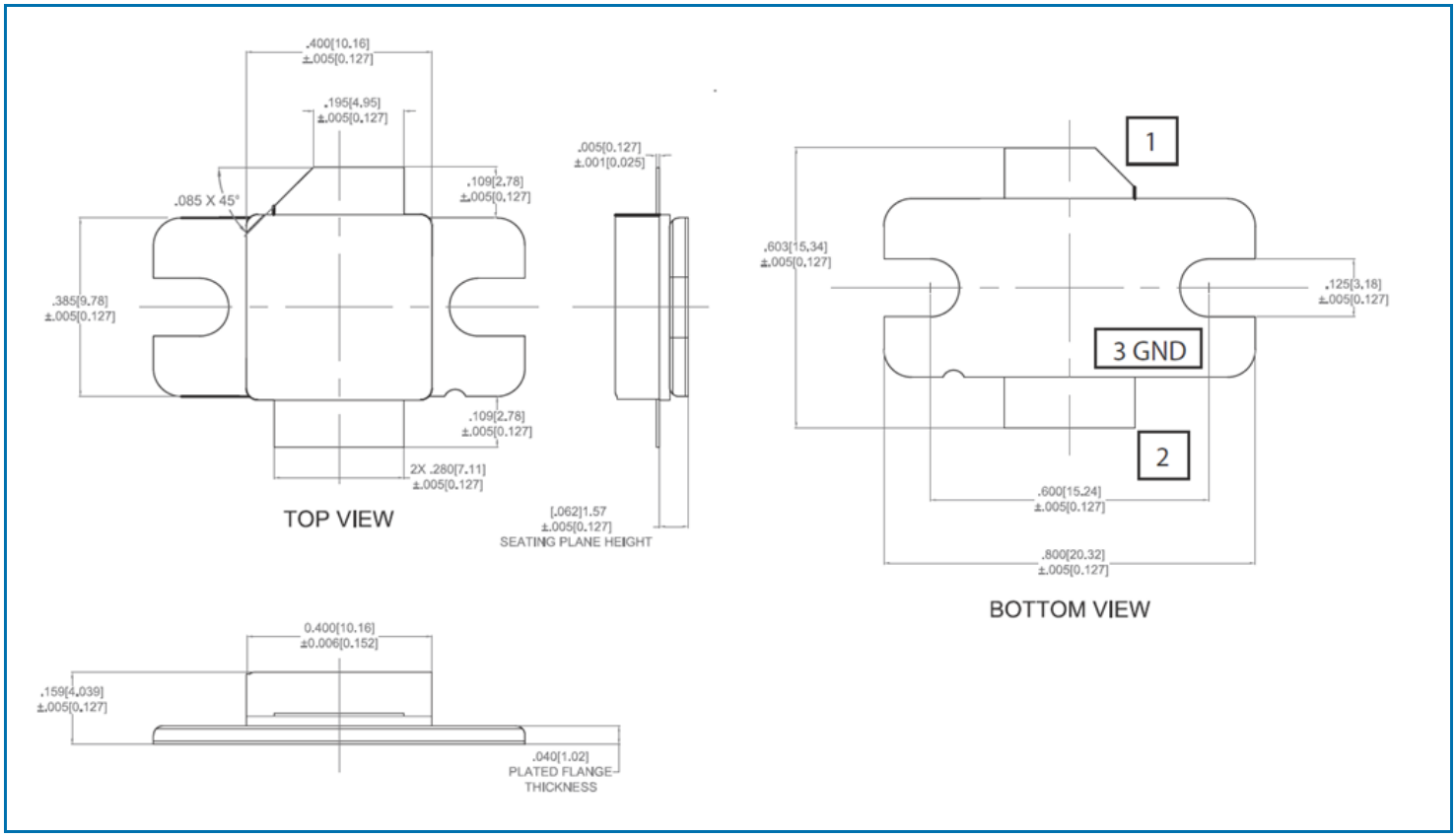
Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)

Quantity	Item	Description	Manufacturer	Manufacturer's P/N
5	C1, C5, C6, C11, C23	CAP, 33pF, 5%, 500V, HI-Q, ATC-B	American Technical Ceramics	800B330JT500XT
1	C3	CAP, 18pF, 5%, 500V, HI-Q, ATC-B	American Technical Ceramics	800B180JT500XT
2	C4, C9	CAP, 2.0pF, +/-0.1pF, 500V, C0G, ATC-B	American Technical Ceramics	800B2R0BT500X
2	C7, C8	CAP, 2.4pF, +/-0.1pF, 500V, C0G, ATC-B	American Technical Ceramics	800B2R4BT500X
1	C10	CAP, 1.5pF, +/-0.1pF, 500V, C0G, ATC-B	American Technical Ceramics	800B1R5BT500X
3	C2, C19, C20	CAP, 2.7pF, +/-0.1pF, 500V, C0G, ATC-B	American Technical Ceramics	800B2R7BT500X
2	C12, C16	CAP, 0.1µF, 10%, 100V, X7R, 1210	Murata Electronics	GRM32NR72A104KA01L
3	C13, C14, C17	CAP, 4.7µF, 10%, 100V, X7R, 2220	Murata Electronics	GRM55ER72A475KA01L
1	C24	CAP, 100µF, 20%, 50V, AL ELEC, SMD	PANASONIC INDUSTRIAL CO	ECE-V1HA101UP
1	C15	CAP, 330µF, +/-20%, 100V, FC, RAD	PANASONIC INDUSTRIAL CO	EEU-FC2A331
2	R1, R3	RES, 10Ω, 5%, 1/4W, 1206	PANASONIC INDUSTRIAL CO	ERJ-8GEYJ100V
1	R2	RES, 3.3Ω, 5%, 1/4W, 1206	PANASONIC INDUSTRIAL CO	ERJ-8GEYJ3R3V

Package Drawing (Dimensions in millimeters)



NOTE: PLATING: 35 – 55 µ" Au OVER 100 µ" NI MIN. ON METAL AND METALLIZATION AREAS

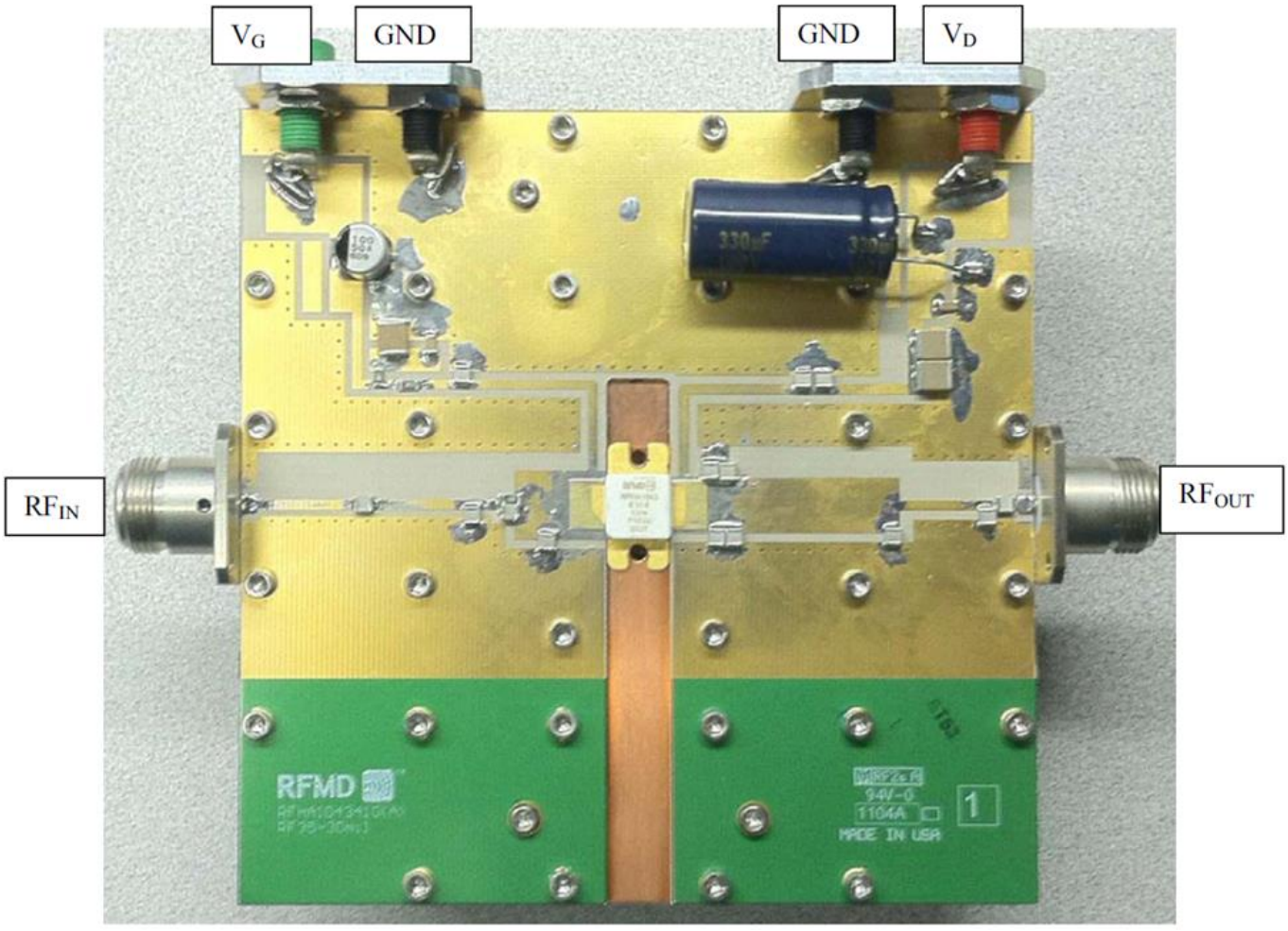
Pin Names and Descriptions

Pin	Name	Description
1	GATE	V_{GQ} RF Input
2	DRAIN	V_{DQ} RF Output
3	SOURCE	Ground Base

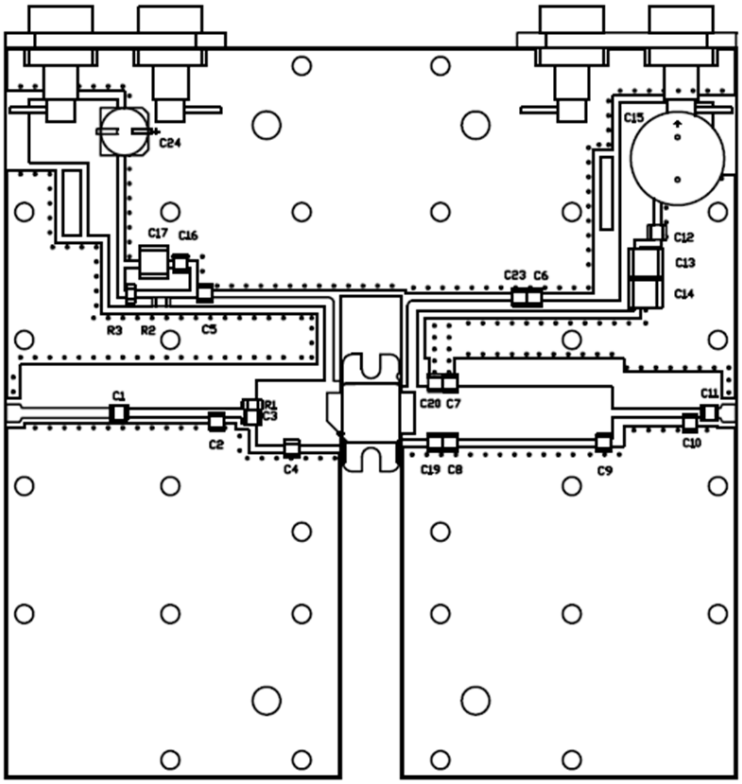
Bias Instruction for RFHA1043 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
Evaluation board requires additional external fan cooling.
Connect all supplies before powering evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -5V to VG.
4. Apply 48V to VD.
5. Increase V_G until drain current reaches 600mA or desired bias point.
6. Turn on the RF input.



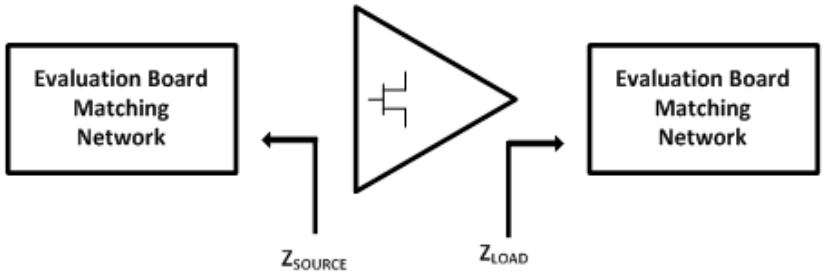
Evaluation Board Layout



Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
1200	4.25 - j4.8	5.34 + j1.5
1400	4.1 - j2.2	5.1 + j1.48
1600	5.3 + j0.06	4.8 + j1.9
1850	9.2 + j0.6	3.1 + j1.75

NOTE: Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



Device Handling/Environmental Conditions

RFMD does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.