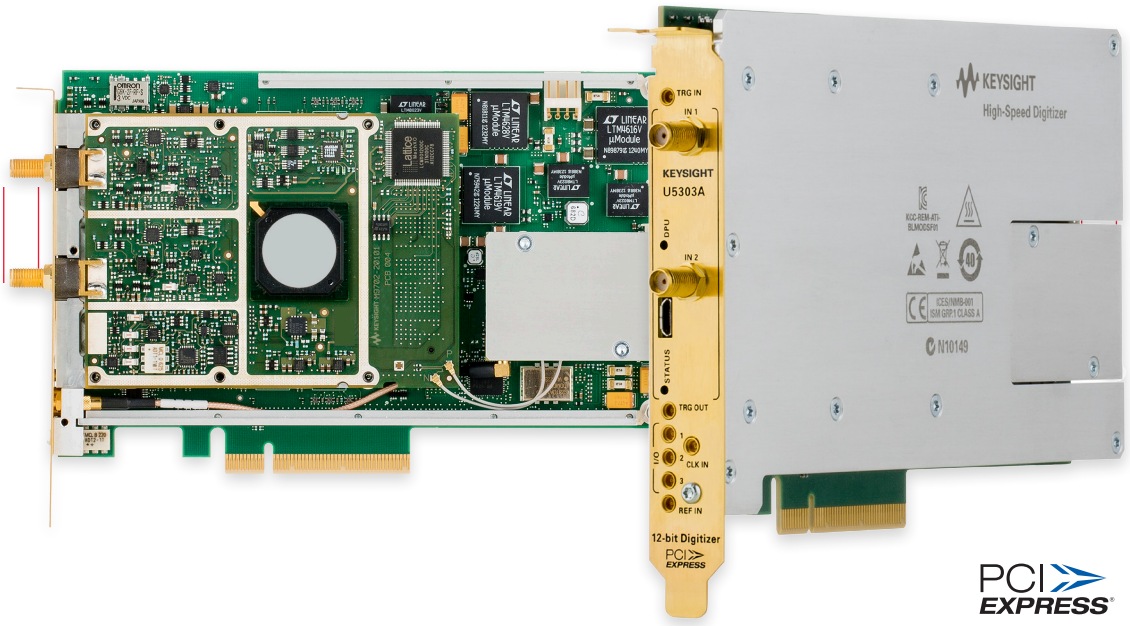
Keysight U5303A

PCIe High-Speed Digitizer with On-Board Processing

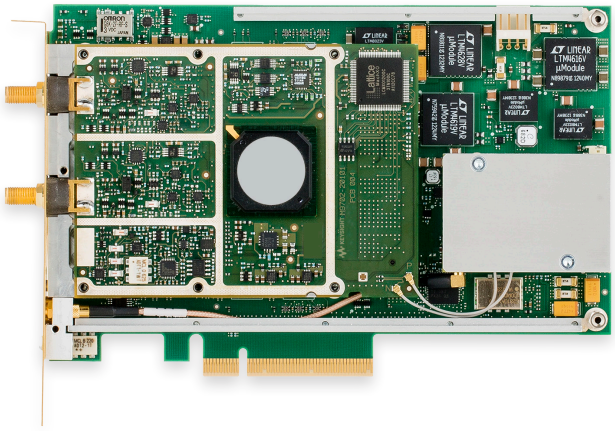
2 channels, 12-bit, up to 3.2 GS/s, DC up to 2 GHz bandwidth with custom firmware support

Data Sheet



KEYSIGHT TECHNOLOGIES

Overview



Introduction

The U5303A is a fast 12-bit PCIe® digitizer with programmable on-board processing, making it ideal for biotechnology, semiconductors, and physics. The U5303A is particularly suited for OEM applications with its fast PCI Express 2.0 eight lanes connection.

Product description

The U5303A ADC card occupies a single full-length PCIe slot of the host PC. Featuring sample rates of 1.6 GS/s per channel, up to 3.2 GS/s in interleaved mode, along with an analog bandwidth of up to 2 GHz and DDR3 acquisition memory options up to 4 GB, the U5303A includes a Xilinx Virtex-6 FPGA allowing implementation of custom real-time processing algorithms using the available FPGA development kit.

The digitizer firmware included allows signal acquisition to the on-board memory and subsequent transfer to the host PC via the PCIe bus.

For information on other firmware options please contact Keysight Technologies, Inc.: **digitizers@keysight.com**

Example applications

- Medical research instrumentation (e.g. OCT)
- Environmental monitoring (Laser and Lidar)
- Analytical time-of-flight (TOF)
- Ultrasonic non-destructive testing (NDT)
- Semiconductor test

Product features

- 1 channel with 12-bit resolution up to 3.2 GS/s sampling rate with interleaving enabled
- 2 channels up to 1.6 GS/s simultaneous sampling rate per channel
- DC up to 2 GHz bandwidth
- 50 Ω input impedance, DC coupled
- Selectable 1 V or 2 V full scale range (FSR)
- ±200 fs channel-to-channel skew stability
- 15 ps RMS trigger time interpolator (TTI) precision
- Up to 4 GB DDR3 on-board memory
- On-board data processing unit using a Xilinx Virtex-6 FPGA
- Support for loading custom real-time processing
- PCI Express 2.0 eight lanes (x8)
- Real-time averaging and peak detection options

Uncompromising values

- Dual channel
- Fast PCIe 12-bit digitizer with on-board processing
- Capture wide bandwidth signals
- High dynamic range acquisition for better measurement fidelity
- Accurate measurement
- Large on-board memory
- Custom firmware implementation
- Capable of switching between multiple firmware programs
- Very high digitized data throughput
- Software support including multiple programmable interfaces for easy integration into existing environments
- Reduced development time, fast time to market
- Self-trigger mode for unequaled synchronous noise reduction
- Continuous data streaming
- Window and Linux support

Hardware platform

Product overview

Benefitting from the very high data transfer rates of the PCIe 2.0 interface, and occupying a single x8 slot in a host PC, the U5303A offers high performance in a small footprint, making it an ideal platform for many commercial, industrial and aerospace & defense embedded systems.

On-board real-time processing

At the heart of the U5303A ADC card is a data processing unit (DPU) based on the powerful Xilinx Virtex-6 FPGA. This DPU is responsible for controlling the module functionality, data flow and real-time signal processing. This powerful feature allows data reduction and storage to be carried out at the digitizer level, minimizing transfer volumes and speeding-up analysis.

Block diagram

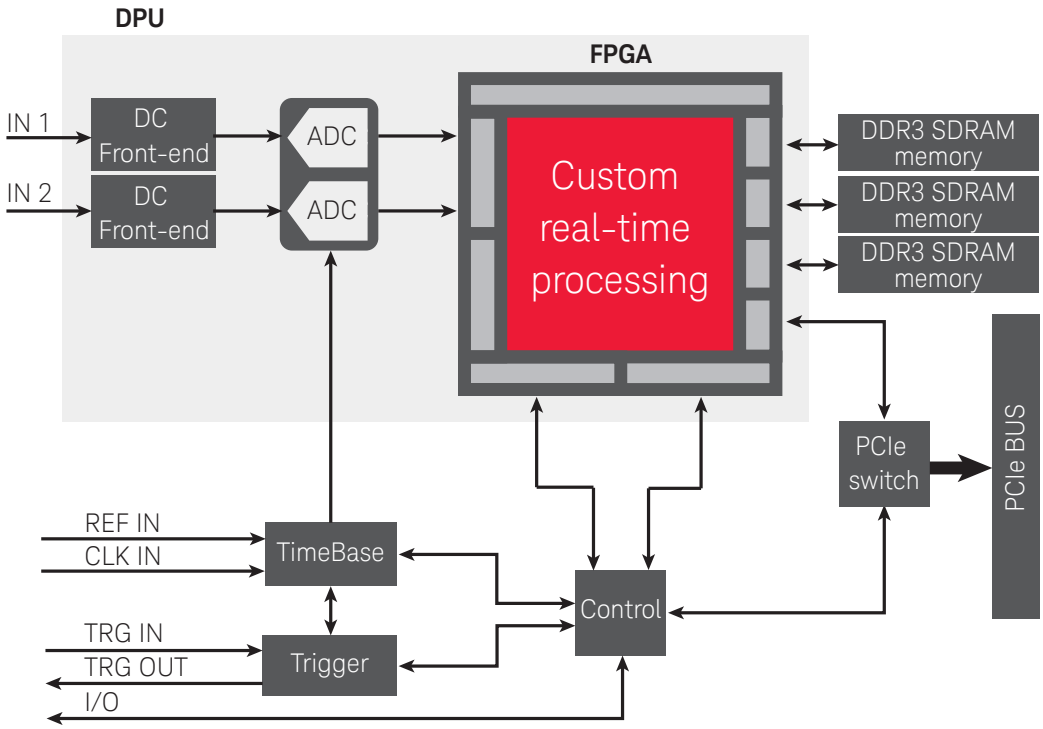


Figure 1. Simplified block diagram of the U5303A PCIe high-speed digitizer with on-board processing.

Some of the awards earned by the Keysight U5303A PCIe high-speed digitizer:

BEST IN TEST 2014 WINNER

ACE AWARDS 2014 WINNER EETimes EDN

ECN iMPACT 2014 Winner Awards

Software Platform

Keysight Software Suite

Keysight IO Libraries Suite offers FAST and EASY access to the U5303A using a standardized interface and ensuring compatibility and upgradability of the software applications.

Drivers

The module comes with the Keysight MD2 IVI-COM and IVI-C standard software drivers that work in the most popular development environments including Visual C/C++, C#, VB.NET, MATLAB, and LabVIEW. Linux is also supported using the IVI-C driver.

Easy software integration

To help you get started and complete complex tasks quickly, the U5303A digitizer is supplied with a comprehensive portfolio of module drivers, documentation, examples, and software tools to help you quickly develop test systems with your software platform of choice.

Compliance

The U5303A is compliant with PCI Express 2.0 standard. Designed to benefit from fast data interfaces, the product can be integrated into PCI Express slots.

Calibration

The U5303A is factory calibrated and shipped with a certificate of calibration.

Figure 2. U5303A front panel with analog inputs and multiple I/O signals.

Figure 3. The Keysight U5303A PCIe 12-bit digitizer with on-board processing offers a small size for easy integration.

Firmware Development

U5340A - FPGA Development Kit[1]

The FPGA development kit is primarily intended to open the design of the FPGA to specific user requirements by providing a development framework that interfaces to the underlying hardware.

The FPGA development kit combines capabilities to:

- Achieve multi GS/s real-time processing on a full digitizer framework by leveraging the full density and speed of the FPGA.
- Shorten time-to-market with turn-key, easy-to-use development flow and debug.

There are several rationales to consider developing custom signal processing such as:

- Data throughput optimization
- Real time processing
- Implementation of custom IP and OEM technical know-how
- Re-usability and upgradability.

The FPGA development kit includes everything you need: source code, ready-to-use base design, a set of cores to easily interface to the underlying hardware, a test-bench environment for design and simulation, and automated building script.

For more information:
Keysight U5340A - FPGA Development Kit for High-Speed Digitizers
Keysight product brochure 5991-2424EN
http://literature.cdn.keysight.com/litweb/pdf/5991-2424EN.pdf

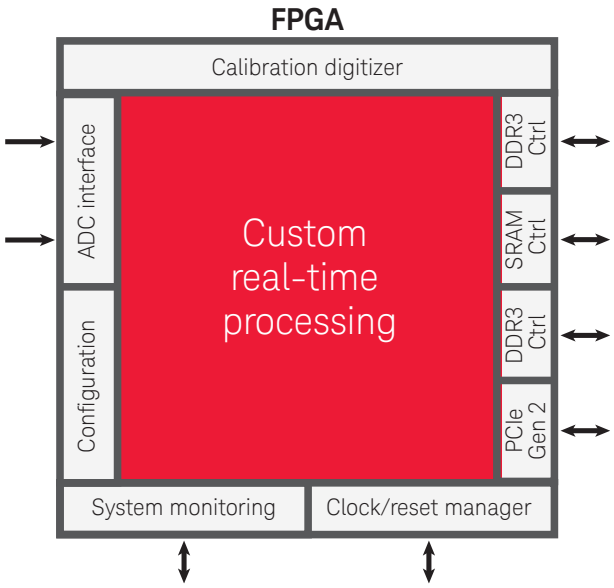


Figure 2. Enlarged block diagram of the FPGA Xilinx Virtex-6

Predefined Keysight IP cores

Custom real-time processing (using the FPGA development kit)

1. This standalone software package must be acquired separately.

Firmware Options

The U5303A PCIe high-speed digitizer provides several firmware options:

- **DGT**[1]: Digitizer firmware
- **INT**: Interleaved channel sampling functionality
- **FDK**[2]: Custom firmware capablility (required to load FPGA firmware created with U5340A)
- **AVG**[2]: Firmware for real-time sampling and averaging
- **PKD**[2]: Firmware for real-time signal peak detection
- **TSR**[3]: Triggered simultaneous acquisition and readout
- **CSR**[3]: Continuous simultaneous acquisition and readout

Table 1. Firmware options versus sampling rate.

	Sampling rate		
Firmware	**-SR0**	**-SR1**	**-SR2**
-DGT	✓	✓	✓
-INT	✓	✓	✓
-FDK	✓	✓	✓
-AVG	–	✓	✓
-PKD	–	✓	✓
-TSR	–	✓	✓
-CSR	–	✓	✓

Easy firmware switch

A simple call to the configuration function will enable to switch to the required option.

DGT digitizer firmware

The digitizer firmware:

- Allows standard data acquisition, including: digitizer initialization, setting of the acquisition and clocking modes, management of channel triggering for best synchronization, storing data in the internal memory and/or transferring them through the backplane bus.
- Implements multi-record acquisition functionality.
- Supports fixed internal clocking frequency with internal or external reference, and variable frequency external clock.
- Programmable binary decimation available with SR1 and SR2 option to lower the sample rate by a factor of 2^n where n is defined in the range of 1 to 10 for single record.
  e.g. for a U5303A-SR2 you can select from 3.2 GS/s (with interleaving) down to 3.125 MS/s.

INT interleaved channel sampling functionality

This interleave option allows two channels to be combined and to reach 3.2 GS/s (SR2 option) in one channel acquisition mode.

FDK custom firmware capability

This option enables loading of custom firmware created with the U5340A FPGA development kit.

1. Not available with SS1 and BB1 options.
2. A calibration digitizer function is available with each firmware.
3. Only available with DGT option.

Firmware Options *(continued)*

AVG firmware for real-time sampling and averaging

Averaging signals reduces random noise effects, improving the signal-to-noise ratio, as well as increasing resolution and dynamic range.

Synchronous real-time sampling and accumulation up to 3.2 GS/s on single-channel and dual-channel with:

- Accumulation of 1 up to 520,000 triggers in steps of 8 triggers[1].
- Effective acquisition length of up to 480 KSamples in single channel or 240 KSamples per channel in dual-channel.
- Noise suppressed accumulation (NSA).
- Self-trigger mode for minimal synchronous noise.
- Baseline stabilization algorithm and digital offset.

PKD firmware for real-time signal peak detection

The peak detection firmware allows real-time acquisition and peak detection with the possibility to generate a histogram of peak versus time for successive acquisitions.
Synchronous real-time sampling and peak detection up to 3.2 GS/s on single-channel and dual-channel with:

- Accumulation of 1 up to 520,000 triggers in steps of 8 triggers[1].
- Effective acquisition length of up to 480 KSamples in single channel or 240 KSamples per channel in dual-channel.
- Self-trigger mode for minimal synchronous noise.
- Baseline stabilization algorithm and digital offset.

TSR triggered simultaneous acquisition and readout

The triggered simultaneous acquisition and readout concept guarantees no lost triggers at high repetition rate for specific configuration[2]:

- Larger memory size increases the maximum margin for host PC processing time, and allows for short to very long record size.
- The architecture allows to continuously acquire new records while reading previous ones.
- PCIe 2.0 with 8 lanes allows fast data throughput.
- High precision integrated time to digital converter can be used to increase time measurement accuracy.

CSR continuous simultaneous acquisition and readout

The continuous simultaneous acquisition and readout implements a firmware function and a software API which allows the user to readout multiple streams while the acquisition is still running. A stream is defined as a sequence of data elements made available over time. The data elements can be samples, timestamps information, real time measurements, etc. Each stream can be read independently and in a time multiplexed manner allowing a fine tuning of the system and application performance.

The acquisition data rate is adapted to the target application by several mechanisms:

- Downsampling: Allows to reduce the acquisition sample rate by performing a binary decimation.
- Truncation and Compression: It truncates the samples on fewer bits and pack them continuously to reduce total volume.
- External clock: Allows a fine tuning of the incoming sample rate.

The data rate that can be sustained gapless without overflow is limited by the PCIe sustained throughput on the target system. When an overflow occurs the writing to the stream buffers are disabled and the already acquired data is still valid and can be read-out.

1. Expected for 8 first triggers.
2. Please contact Keysight to find out the repetition rate that can be achieved in your application.

Applications Options[1]

For specific applications the U5303A PCIe high-speed digitizer can be configured with specific options:

- **CB0**:Digitizer streaming
- **CB1**: Digital down-converter streaming
- **SS1**[2]: Swept source laser for OCT application
- **BB1**[2]: High fidelity digitizer

CB0 digitizer streaming

CB0 is a turnkey reference bundle, based on the CSR architecture for continuous gapless acquisition, implementing a real time digitizer data recorder. It includes a command line application ensuring recording performance of up to 1 GB/s in a specific qualified system. An easy to use data viewer application is also provided.

This continuous simultaneous acquisition and readout with bundled applications provides:

- Guaranteed recording specification.
- Various recording speed controlled by application.

This option is using a U5303A pre-configured version composed:

- 2 channels version (-CH2)
- 1 GS/s sampling rate (-SR1)
- Full bandwidth (-F10)
- 4 GB acquisition memory (-M40)
- LX195T DPU FPGA (-LX2)
- Digitizer firmware (-DGT)

The digitizer data streamer application is an intuitive command line application which allows to control the U5303A and adapt its data rate to the target application.

The data viewer is a simple graphical user interface (GUI) application which allows to read, display, select and export the data stored.

CB1 digital down-converter streaming

CB1 is a turnkey reference bundle, based on the CSR architecture for continuous gapless acquisition, implementing a real time digital down-converter data recorder. It includes a command line application ensuring recording performance of up to 180 MHz in a specific qualified system. An easy to use data viewer application is also provided.

This continuous simultaneous acquisition and readout with bundled applications provides the same functionality as CB0 adding:

– Digital down-converter functionality in real time.

1. Application options are delivered on the high-speed digitizer applications DVD.
2. DGT option not available with these applications options.

Applications Options *(continued)*

SS1 swept source OCT application

The swept source optical coherence tomography (OCT) option is a bundle designed for customers who want best-in-class swept source OCT performance, by integrating all OCT processing in the on-board FPGA for real-time computation.

This option is using a U5303A pre-configured version composed of:

- 2 channels version (-CH2)
- 500 MS/s sampling rate (-SR0)
- 650 MHz bandwidth (-F05)
- 256 MB acquisition memory (-M02)
- LX195T DPU FPGA (-LX2)
- Card retainer (U5300A-001)

The third party OCT dedicated firmware and companion software are included in this bundle in the high-speed digitizer software application DVD.

BB1 high fidelity digitizer

This high fidelity digitizer option is a bundle providing enhanced performance by:

- compensating the ADC and front-end distortion,
- minimizing interleave spurs, and
- reducing the overall noise bandwidth.

This results in highly improved and uniform measurement fidelity across the useful bandwidth, which greatly benefits RF and wireless frequency domain measurements. The digitizer's post processing compensation also delivers better spurious-free dynamic range (SFDR) and intermodulation product (IMx) specifications.

This application option pre-configures the U5303A PCIe high-speed digitizer with the following options:
U5303A-CH2, -SR2, -F05, -M02, -LX2, -BB1 and U5300A-001.

It allows the following usage as high fidelity digitizer:

- 1.6 GS/s with 650 MHz bandwidth, up to 64 MSamples/ch.
- 800 MS/s with 400 MHz bandwidth, up to 32 MSamples/ch.
- 400 MS/s with 200 MHz bandwidth, up to 16 MSamples/ch.
- 200 MS/s with 100 MHz bandwidth, up to 8 MSamples/ch.
- 100 MS/s with 50 MHz bandwidth, up to 4 MSamples/ch.

Technical Specifications and Characteristics

Analog input (IN1 and IN2 SMA connectors)			
Number of channels			2 (without INT option), 2 or 1 (with INT option)
Impedance			50 Ω ±2 %
Coupling			DC
Full scale ranges (FSR)			1 V and 2 V
Maximum input voltage			1V FSR: 3 V RMS, ± 3.6 Vpk 2V FSR: 4.3 V RMS, ± 6.3 Vpk
Input voltage offset			–2xFSR to +2xFSR
Input frequency range (-3 dB bandwidth)			See table below
DC gain accuracy			± 0.5% *(typical)* in 1V FSR ± 0.7% *(typical)* in 2V FSR
Offset accuracy			± 0.5% in 1V FSR ± 1.5% in 2V FSR
Time skew[1]	Skew between channels[2]		± 50 ps *(nominal)*
	Channel-to-channel skew stability[3]		± 200 fs pk *(nominal)* 75 fs RMS *(nominal)*[2]
Bandwidth limit filters (BWL)			650 MHz *(nominal)* for -SR1 and -SR2, no BWL for -SR0
Effective bits (ENOB)[4]		-SR0	@ 100 MHz 9.0 (9.3 *typical)*
		-SR1 & -SR2	@ 410 MHz 8.7 (9.1 *typical)*
Signal to noise distortion (SNR)[4]		-SR0	@ 100 MHz 56 dB (58 dB *typical*)
		-SR1 & -SR2	@ 410 MHz 55 dB (57 dB *typical*)
Spurious free dynamic range (SFDR)[4]		-SR0	@ 100 MHz 55 dBc (63 dBc *typical*)
		-SR1 & -SR2	@ 410 MHz 56 dBc (64 dBc *typical*)
		-BB1	@ 410 MHz 65 dBc (71 dBc *typical*)
Total harmonic distortion (THD)[4]		-SR0	@ 100 MHz –55 dB (–63 dB *typical*)
		-SR1 & -SR2	@ 410 MHz –56 dB (–64 dB *typical*)
		-BB1	@ 410 MHz –65 dB (–68 dB *typical*)

Table 2. Input frequency range versus options and full scale range.

			Input frequency range	
Options			**1 V FSR**	**2 V FSR**
-F05	-SR0	-	DC to 400 MHz *(typical)*	
		-INT		
	-SR1/-SR2	-	DC to 650 MHz *(typical)*	
		-INT		
-F10	-SR1/-SR2	-	DC to 1.9 GHz *(typical)*	DC to 2.0 GHz *(typical)*
		-INT	DC to 1.3 GHz *(typical)*	

1. The channel-to-channel skew is defined as the magnitude of time delay difference between two digitized channel inputs, granted the same signal is provided to each channel at the exact same time.
2. The measurement represents the maximum time skew between 2 channels of a single unit, measured with a Sinefit method on 100 k samples, for a sinusoid signal at 400 MHz and averaged 10 times.
3. Skew and offset stability are measured at 25 °C in a climatic chamber. The skew and offset between channels are measured every 5 minutes over 12 hours and after 1 hour stabilization time and the values represent the dispersion of the measurements.
4. Measured for a –1 dBFS input signal in internal clock mode with option -F10 at 1.6 GS/s (option -SR2) and 1 GS/s (option -SR1), and with option -F05 at 500 MS/s (option -SR0).

Technical Specifications and Characteristics *(continued)*

Digital conversion		
Resolution		12 bits
Acquisition memory (total)	-M02 -M10 -M40	256 MB (64 MSamples/ch) 1 GB (256 MSamples/ch) 4 GB (1 GSamples/ch)
Sample clock sources		Internal or external
Internal clock source		Internal, external reference
Real-time sampling rates		See the table below
Sampling jitter		225 fs *(nominal)*[1]
Clock accuracy		±1.5 ppm
External clock source (CLK IN MMCX connector)		
Impedance		50 Ω *(nominal)*
Frequency range[2]	-SR0 -SR1 -SR2	From 500 MHz to 1 GHz From 1.8 GHz to 2 GHz From 2 GHz to 3.2 GHz
Signal level		+5 dBm to +15 dBm *(nominal)*, 0 V DC
Coupling		AC
External reference clock (REF IN MMCX connector)		
Impedance		50 Ω *(nominal)*
Frequency range		100 MHz ±1 kHz *(nominal)*
Signal level		–3 dBm to +3 dBm *(nominal)*
Coupling		AC
Acquisition modes (depends on firmware options)		Single shot, sequence[3], continuous

Table 3. Real-time sampling rates with internal clock source.

	Max sampling rate		
Channel configuration	**-SR0**	**-SR1**	**-SR2**
-CH2	0.5 GS/s	1 GS/s	1.6 GS/s
-CH2 and -INT	1 GS/s	2 GS/s	3.2 GS/s

1. Jitter figure based on phase noise integration from 100 Hz to 1600 MHz.
2. The sampling rate corresponds to half of the external clock frequency in 2-channel mode (non interleaved channels). In interleaved mode (only available with the INT option), the sampling rate corresponds to the frequency of the external clock signal.
3. Up to 131072 records. Record maximum length = memory size/number of channels.

Technical Specifications and Characteristics *(continued)*

Trigger		
Trigger modes		Edge (positive, negative), level
Trigger sources		External, Software, Channel
Channel trigger frequency range		DC to 250 MHz
External trigger (TRG IN MMCX connector)		
Coupling		DC
Impedance		50 Ω *(nominal)*
Level range		± 5 V *(nominal)*
Minimum amplitude		0.5 V pk-pk
Frequency range		DC to 2 GHz *(nominal)*
Maximum time stamp duration		See the table below
Trigger time interpolator resolution		See the table below
Trigger time interpolator precision		See the table below
Rearm time (deadtime)	-SR0 & -SR1 -SR2	800 ns *(nominal)* 500 ns *(nominal)*
Trigger out (TRG OUT MMCX connector)[1]		1 (programmable), 50 Ω source
Signal level		0.8 Vpp ±2.5 Voffset *(nominal)* into high impedance
Control IO (I/O 1 and 2 MMCX connectors)[2]		
Output functions		Acquisition active Trigger is armed Trigger accept resynchronization 100 MHz reference clock divided by 2[3] Sampling clock divided by 32[3] Low level High level FPGA synchronization
Input/output function		FPGA programmable I/O

Table 4. Trigger time parameters.

	Sampling rate		
Mode	**-SR0**	**-SR1**	**-SR2**
Maximum time stamp duration	32 days	32 days	52 days
Trigger time interpolator resolution	10.15 ps *(nominal)*	10.50 ps *(nominal)*	6.25 ps *(nominal)*
Trigger time interpolator precision	19.75 ps RMS *(nominal)*	20.25 ps RMS *(nominal)*	15 ps RMS *(nominal)*

1. At 10 MHz on a 50 Ω load.
2. I/O 3 reserved for future use.
3. Only on I/O 1.

Technical Specifications and Characteristics *(continued)*

Environmental and physical[1]			
Temperature range	Operating		0 to +50 °C (sea-level to 10,000 feet)[2] 0 to +45 °C (10,000 to 15,000 feet)[2]
	Non-operating		–40 to +70 °C
Altitude			Up to 15,000 feet (4'572 meters)
EMC			Complies with European EMC Directive 2004/108/EC – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A – AS/NZS CISPR 11 – ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme à la norme NMB-001 du Canada.
Acoustic			European Machinery Directive 2002/42/EC, 1.7.4.2u Acoustic noise emission LpA < 70 dB Operator position Normal operation mode
Power dissipation[3]			
+ 3.3 V	+ 3.3 V_{AUX}	+ 12 V	Power on PCIe edge connector
0.8 A *(typical)*	0.2 A *(typical)*	2.3 A *(typical)*	31 W *(typical)*
+ 5 V		+ 12 V	Power on additional power cable[3]
1.5 A *(typical)*		1.5 A *(typical)*	26 W *(typical)*
Mechanical characteristics			
Form Factor			PCIe x8 standard (full length with fan)
Size		Without fan	17.6 W x 126.3 H x 169.5 D mm[4]
		With fan	40.6 W x 126.3 H x 252.1 D mm[5]
Weight			0.68 kg (1.49 lbs)

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.
2. PC internal ambient temperature at intake of the digitizer's fan.
3. Additional power cable mandatory to ensure adequate power distribution as per PCIe standard.
4. 60 m³/h airflow is required. The unit must be operated with the included fan.
5. Additional rail guide is included to stabilize the PCIe card in the PC.

Technical Specifications and Characteristics *(continued)*

System requirements (contact us at digitizers@keysight.com for a list of recommended host computers)		
Topic	**Windows**	**Linux**
Operating systems	Windows 7 (32-bit and 64-bit), All versions Windows 8.1 (32-bit and 64-bit), All versions Note: If using high-speed digitizer applications DVD, Windows 7 (64-bit) is supported.	Linux Kernel 2.6 or higher (32 or 64-bit), Debian 7.0, CentOS 6
Processor speed	1 GHz 32-bit (x86), 1 GHz 64-bit (x64), no support for Itanium 64	As per the minimum requirements of the chosen distribution
Available memory	1 GB minimum	As per the minimum requirements of the chosen distribution
Available disk space[1]	1.5 GB available hard disk space, includes: – 1 GB available for Microsoft .NET Framework 3.5 SP1 – 100 MB for Keysight IO Libraries Suite Note: 400 MB for high-speed digitizer applications.	100 MB
Video	Support for DirectX 9 graphics with 128 MB graphics memory recommended (Super VGA graphics is supported)	No graphics required (for headless system), or X Windows
Browser	Microsoft Internet Explorer 7 or greater	Distribution supplied browser

Definitions for specifications

Specifications describe the warranted performance of calibrated cards that have been stored for a minimum of 2 hours within the operating temperature range of 0 to 50 °C, unless otherwise stated, and after a 45 minute warm-up period. Data represented in this document are specifications unless otherwise noted.

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics are often referred to as Typical or Nominal values.

- ***Typical*** describes characteristic performance, which 80% of cards will meet when operated over a 20 to 30 °C temperature range. Typical performance is not warranted.
- ***Nominal*** describes representative performance that is useful in the application of the product when operated over a 20 to 30 °C temperature range. Nominal performance is not warranted.

Note: All graphs contain measured data from several units at room temperature unless otherwise noted.

1. Because of the installation procedure, less disk space may be required for operation than is required for installation. The amount of space listed above is required for installation.

Configuration and Ordering Information

Software information

Supported operating systems and host computers	See system requirements
Standard compliant drivers	IVI-COM, IVI-C, MATLAB
Supported application development environments (ADE)	VisualStudio (VB.NET, C#, C/C++), VEE, LabVIEW, LabWindows/CVI, MATLAB

Related products

Model	Description
U5340A	FPGA Development Kit for High-Speed Digitizers
Advantage services: calibration and warranty	
Keysight Advantage Services is committed to your success throughout your equipment's lifetime.	
Included	3-year warranty (return to Keysight), standard
R-51B-001-5Z	5-year return to Keysight assurance plan

Accessories

Model	Description
U1092A-CB0	MMCX to SMA cable, 1m
U1092A-CB1	MMCX to BNC cable, 1m

Please contact Keysight for other options not shown:
digitizers@keysight.com

Ordering information

Model	Description
U5303A	PCIe 12-bit Digitizer with on-board processing Includes: - Software, example programs and product information on CD - MMCX to BNC cable, 1 m (qty 1) - Additional power supply cables - Fan assembled on module - Return to Keysight Warranty extended to 3 years
Configurable options	
Sampling rate	
U5303A-SR0	500 MS/s sampling rate version (1 GS/s sampling rate with -INT option)
U5303A-SR1	1 GS/s sampling rate version (2 GS/s sampling rate with -INT option)
✓ U5303A-SR2	1.6 GS/s sampling rate version (3.2 GS/s sampling rate with -INT option)
Bandwidth	
✓ U5303A-F05	Bandwidth, 650 MHz maximum (-SR2/-SR1) or 400 MHz (-SR0)
U5303A-F10	Full bandwidth
Memory	
U5303A-M02	256 MB (64 MS/ch) acquisition memory
✓ U5303A-M10	1 GB (256 MS/ch) acquisition memory
U5303A-M40	4 GB (1 GS/ch) acquisition memory
Data processing unit	
✓ U5303A-LX2	DPU FPGA: LX195T
Firmware	
✓ U5303A-DGT	Digitizer firmware
U5303A-INT	Interleaved channel sampling functionality
U5303A-FDK	Custom firmware capability (required to load FPGA firmware created with U5340A)
U5303A-AVG	Real-time averager firmware
U5303A-PKD	Real-time peak detection firmware
U5303A-TSR	Triggered simultaneous acquisition and readout
U5303A-CSR	Continuous simultaneous acquisition and readout
Applications	
U5303A-CB0	Digitizer streaming
U5303A-CB1	Digital down-converter streaming
U5303A-SS1	Swept source for laser OCT application
U5303A-BB1	High fidelity digitizer
Card retainer	
✓ U5300A-001	With card retainer
U5300A-002	No card retainer
U5300A-003	Short card retainer

✓ These options represent the standard configuration

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