

EDPLO - 3000

INTERNALLY REFERENCED

APPLICATION

- Commercial
- Military
- Airborne
- Space
- Missile Guidance
- Cable TV Links (CATV)
- Satellite Communications
- Local Area Networks (LAN)
- Global Positioning Systems (GPS)
- Up / Down Converters
- Transmitters & Receivers
- Traffic Sign Post
- Test Equipment
- Digital Radios
- Point to Point Relay
- LMDS



FEATURES

- Dielectric Resonator Technology
- Internal Crystal Oscillator Reference
- Phase Lock Indicator Alarm
- Ultra Low Phase Noise
- MIC and SMT Fabrication
- Ultra Low Microphonics
- Low Power Consumption
- Up To +25 dBm Output Power
- Available From 1 – 40 GHz
- Operating Range -55° to +105°C
- Vibration/ Shock Upgrade
- RoHS Compliant

DESCRIPTION

EDPLO-3000 series Phase Locked Dielectric Resonator Oscillator (PLDRO) utilizes advanced MIC and SMT technology to generate crystal stability at microwave and mm-wave bands up to 40 GHz. The low profile and rugged construction provide excellent durability against harsh environmental conditions such as Shock/ Vibration, Temperature and Humidity.

EDPLO-3000 series oscillator is designed using an ultra-low noise amplifier with series feedback at source and Dielectric Resonator at the gate. High gain, low noise devices are biased and matched precisely to ensure minimum phase noise. The device is carefully matched for maximum power, minimum phase noise and Voltage Standing Wave Ratio (VSWR). The oscillator is compensated for maximum temperature stability, optimum negative resistance and lowest phase noise possible.

EDPLO-3000 series oscillator is buffered by cascaded low noise driver and power amplifiers for minimum load pulling, maximum isolation and power. Transistor devices, and all chip components, are directly attached to gold plated Kovar carriers to minimize shear effect and maximize device heat transfer. Kovar carriers are mounted to the chassis to provide an efficient thermal junction and a stable structure for reduction of microphonics. To ensure oscillator stability over the full temperature range, the tuning elements are precisely designed and positioned to compensate for temperature drift by a factor of three.

EDPLO-3000 series proprietary Phase Lock Loop and Crystal Reference circuitry is designed and fabricated using SMT Technology. The input reference frequency is multiplied and sampled to the output frequency to produce compensating voltage to correct any frequency drift due to temperature variations. A Hi-Frequency Wein-Bridge Oscillator is integrated to provide the necessary sweep voltage to an ultra Hi-Q tuning varactor diode for the purpose of compensation and phase locking. The unique construction of phase lock loop sub-assembly provides excellent temperature stability and minimum solder joints for maximum reliability.

EDPLO-3000 series is internally voltage regulated to avoid reverse bias, frequency pushing, bias modulation and voltage transients. A phase lock indicator alarm of TTL type is provided as a feature. The EDPLO-3000 series are internally reference locked and factory tuned to specified frequency. Mechanical frequency adjustment is provided for optimum phase voltage setting. Buffered Reference Monitor and adjustment are standard features of this Hi-Tech oscillator. The unit may also be externally locked to a reference crystal oscillator.

“Engineering the Dynamics of Technology”

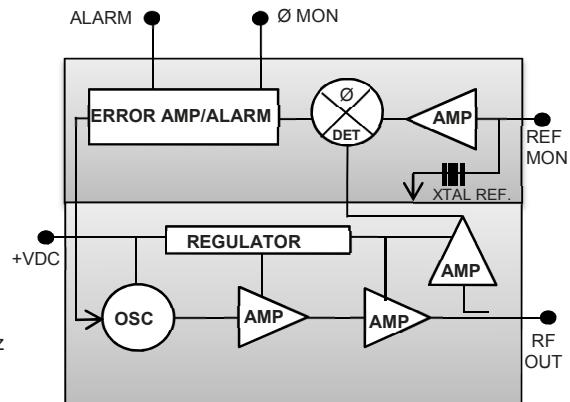
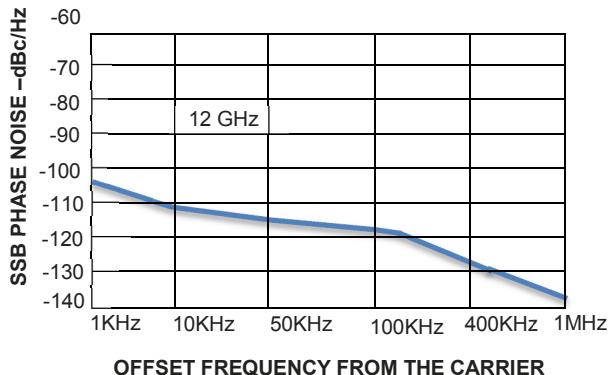


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SPECIFICATIONS

Model Number	EDPLO-3000-XX.XX (Where XX.XX is freq. in GHz)
Single Frequency	1 to 40 GHz
Mechanical Tuning Range	100 MHz
Power Output	+13 dBm, up to +25 dBm Optional
Load VSWR, Maximum	2.0 : 1.0
Power Requirements	+12, +15 VDC, 300 mA
Reference Frequency	50 to 150 MHz
Frequency Stability	+/- 5 PPM @ 0° to 50°C, +/- .5 PPM Optional
Phase Noise	See Phase Noise Envelope (Fig A)
Spurious	-80 dBc
Harmonics	-25 dBc
Alarm	TTL
Operating Temperature	-55° to +105°C Optional, 0-50°C Standard
Storage Temperature	-55° to +125°C
Connectors	SMA Female or 2.92 mm
Size	2.25" x 2.25" x 1.25"
Finish	Nickel

PHASE NOISE ENVELOPE



BLOCK DIAGRAM

OUTLINE DRAWING

