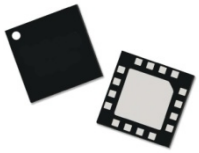
ECP100D

1Watt, High Linearity InGaP HBT Amplifier

Applications

- Final stage amplifiers for Repeaters
- Mobile Infrastructure
- Defense / Homeland Security

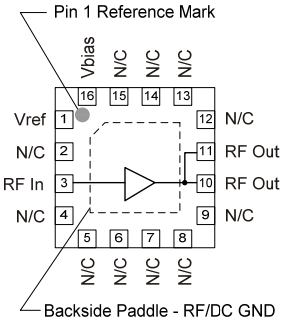


16 Pin 4mm QFN Package

Product Features

- 400 – 2300 MHz
- 18 dB Gain @ 900 MHz
- +31.5 dBm P1dB
- +46 dBm Output IP3
- +5V Single Positive Supply
- Lead-free/green/RoHS-compliant Package

Functional Block Diagram



General Description

The ECP100D is a high dynamic range driver amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve superior performance for various narrowband-tuned application circuits with up to +46 dBm OIP3 and +31.5 dBm of compressed 1-dB power. The part is housed in a lead-free/green/RoHS-compliant SOIC-8 package. All devices are 100% RF and DC tested.

The product is targeted for use as driver amplifier for various current and next generation wireless technologies such as CDMA, W-CDMA, and LTE where high linearity and high power is required. The internal active bias allows the ECP100D to maintain high linearity over temperature and operate directly off a +5 V supply.

Pin Configuration

Pin #	Symbol
1	Vref
2, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15	N/C
3	RF_In
10, 11	RF_Out
16	Vbias
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
ECP100D-G	1 Watt, High IP3 InGaP HBT Amp
ECP100D-PCB900	900 MHz Evaluation Board
ECP100D-PCB1960	1960 MHz Evaluation Board
ECP100D-PCB2140	2140 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65°C to +150°C
RF Input Power (continuous)	+26 dBm
Device Voltage	+8 V
Device Current	900 mA
Device Power	5 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}	+4.75	+5	+5.25	V
I_{cq}		450		mA
T_J (for >10^6 hours MTTF)			200	°C
Operational Temperature	-40		+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

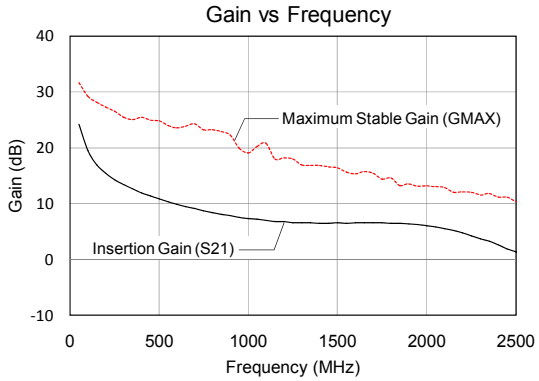
Test conditions unless otherwise noted: V_{cc} = +5 V, I_{cq} = 450 mA, T = 25 °C, F= 2140 MHz, in a tuned applications circuit.

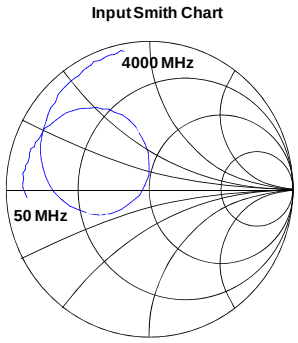
Parameter	Conditions	Min	Typical	Max	Units
Operational Bandwidth		400		2300	MHz
Test Frequency			2140		MHz
Gain		10	11		dB
Input Return Loss			18		dB
Output Return Loss			8		dB
Output P1dB		+29	+31.5		dBm
Output IP3 (at Pout=+15 dBm per tone, 1 MHz spacing)	See Note 1.	+43.8	+45		dBm
Noise Figure			6.3		dB
WCDMA Channel Power (at -45 dBc ACPR)			+23		dBm
Quiescent Current (Icq)	See Note 2.	400	450	500	mA
Reference Voltage Current (Iref)	See Note 3.		11		mA
Total Operating Current at P1dB	See Note 4.		551		mA
Thermal Resistance, junction to case, θ_{jc}				33	°C / W

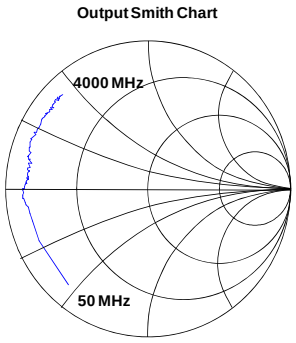
Notes:

1. The suppression on the largest IM3 product is used to calculate OIP3 using a 2:1 rule.
2. Sum of the bias currents into pins 10, 11, and 16 under small-signal conditions.
3. Pin 1 (Vref) is used as a reference voltage for the internal biasing circuitry. It is expected that Pin 1 will draw 11 mA of current when used with a series bias resistor of R1=51 Ω; therefore, total small signal device current will typically be 461 mA.
4. Total bias current into Pins 10, 11, and 16 will typically increase by 90 mA at P1dB; therefore, total device operating current (including Iref) will typically be 551 mA.

Device Characterization Data







Notes:

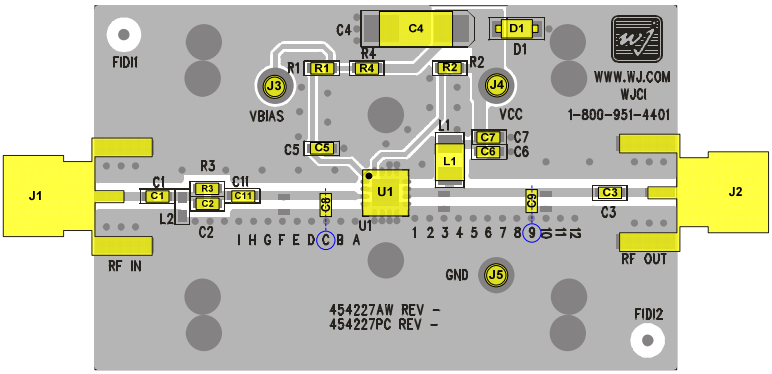
Insertion Gain (S21) is for the unmatched device in a 50 ohm system. In a circuit tuned for a particular frequency band, higher gain can be achieved up to the Maximum Stable Gain (GMAX).

S-Parameter Data

V_{cc} = +5 V, I_{cq} = 450 mA, T = 25 °C, unmatched 50 Ohm system, calibrated to device leads

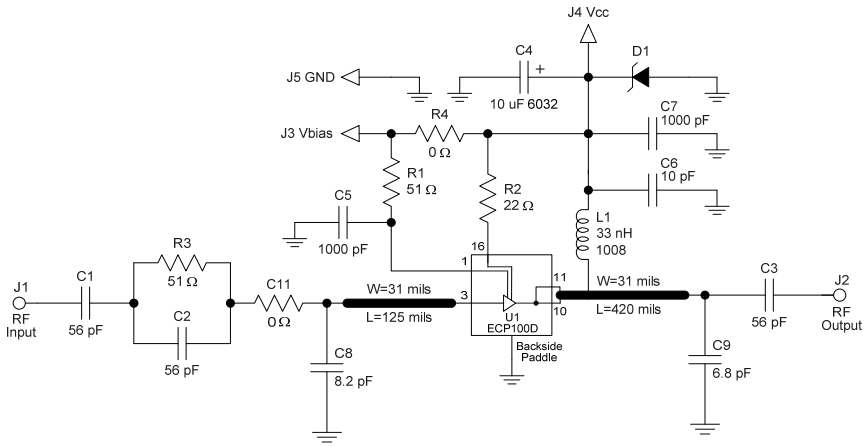
Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-1.35	-176.77	24.16	120.86	-39.11	18.98	-0.87	-131.71
100	-1.11	179.08	19.50	115.85	-38.95	8.44	-1.00	-154.54
200	-1.09	174.88	15.39	113.56	-39.17	8.30	-1.02	-167.00
400	-1.24	167.79	11.91	103.30	-39.00	-4.09	-0.72	-173.95
600	-1.36	159.88	9.93	92.23	-37.15	-12.20	-0.75	-177.40
800	-1.51	152.29	8.39	81.19	-38.07	-10.64	-0.87	-178.56
1000	-1.88	144.07	7.37	70.82	-38.22	-7.28	-1.00	179.90
1200	-2.45	135.03	6.77	59.35	-36.33	-22.70	-1.02	177.51
1400	-3.52	124.13	6.49	45.92	-35.42	-38.76	-1.07	176.63
1600	-5.37	110.92	6.54	30.31	-34.81	-55.67	-1.15	174.49
1800	-9.94	96.35	6.46	9.32	-33.63	-73.80	-1.01	171.25
2000	-26.16	134.17	6.08	-13.70	-33.50	-93.59	-1.00	169.44
2200	-10.08	-149.55	4.75	-39.92	-35.80	-116.52	-0.92	165.85
2400	-4.89	-169.19	2.58	-63.31	-36.84	-156.32	-0.88	161.06
2600	-2.68	172.75	0.02	-82.87	-37.99	-159.31	-1.01	157.31
2800	-1.73	158.17	-2.72	-98.11	-40.80	148.39	-0.96	151.44
3000	-1.22	144.56	-5.32	-111.57	-43.97	152.56	-1.08	148.03

Reference Design 869-960 MHz (ECP100D-PCB900)



Notes:

1. The primary RF microstrip line is 50 Ω.
2. All passive components are 0603 size unless otherwise specified.
3. Observe component value tolerances when specified.
4. Zero ohm jumpers may be replaced with metal trace in user applications.
5. Place component C8 at marker 'C' on the PC Board or 125 mils from the center of C8 to left edge of U1; Electrical length: 6.2 deg. at 900 MHz.
6. Place component C9 at marker "9" on the PC Board or 420 mils from the center of C9 to right edge of U1; Electrical length: 21 deg. at 900 MHz.
7. Vbias is connected to Vcc by R4 for convenience. Remove R4 to apply Vbias independently.

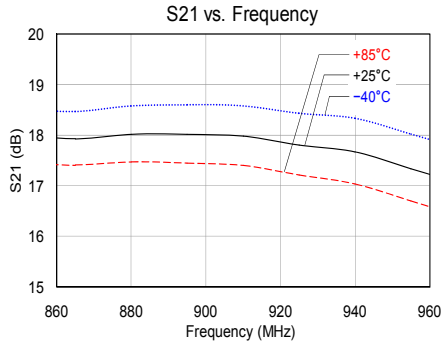


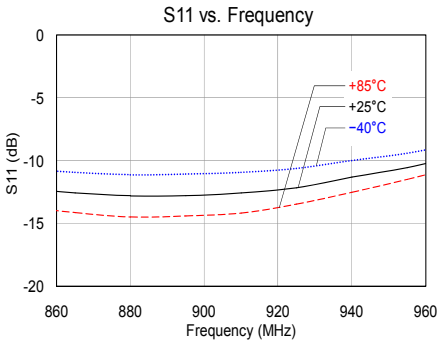
Bill of Material

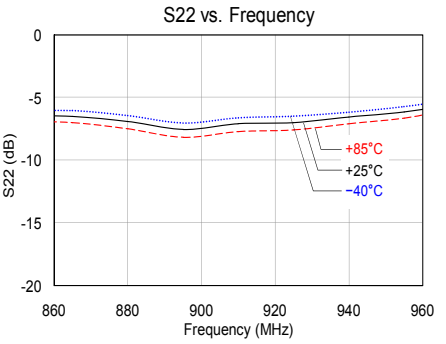
Ref Des	Value	Description	Manufacturer	Part Number
U1	N/A	1 Watt High Linearity InGaP Amp	TriQuint	ECP100D
C1, C2, C3	56 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C4	10 µF	Cap, Chip, 6032, 25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, 50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C8	8.2 pF	Cap, Chip, 0603, 50 V, ±0.1 pF, Accu-P	AVX	06035J8R2BBSTR
C9	6.8 pF	Cap, Chip, 0603, 50 V, ±0.1 pF, Accu-P	AVX	06035J6R8BBSTR
L1	33 nH	Ind, Coil Wound, 1008, 5%, Ceramic Core	Coilcraft	1008HQ-33NXJLC
R1	51 Ω	Res, Chip, 0603, 1%, 1/16 W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R4, C11	0 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
D1	N/A	5.6 V Zener Diode	various	

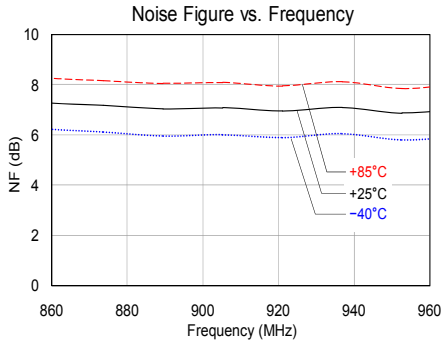
Typical Performance 869-960 MHz (ECP100D-PCB900)

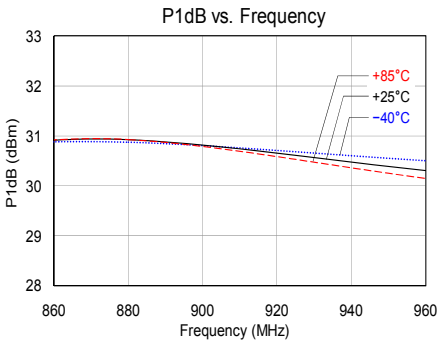
Frequency	MHz	869	900	960
Gain	dB	18	18	17.5
Input Return Loss	dB	13	13	10
Output Return Loss	dB	7	7	6
Output P1dB	dBm	+31	+31	+30
Output IP3 +15 dBm / tone, 1 MHz spacing	dBm	+46	+46	+47
Channel Power @-45 dBc ACPR, IS-95 9 channels fwd	dBm	+25.5	+25.5	+25.5
Noise Figure	dB	7.0	7.0	7.0
Quiescent Current, Icq	mA		450	
Device / Supply Voltage	V		+5	

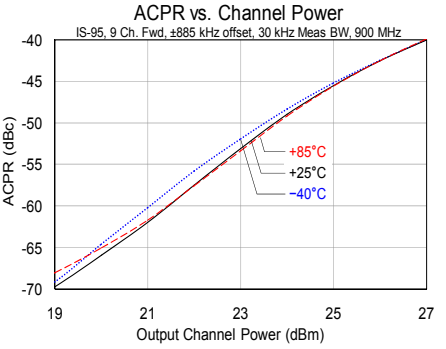


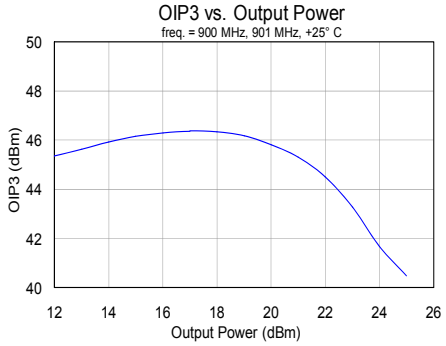


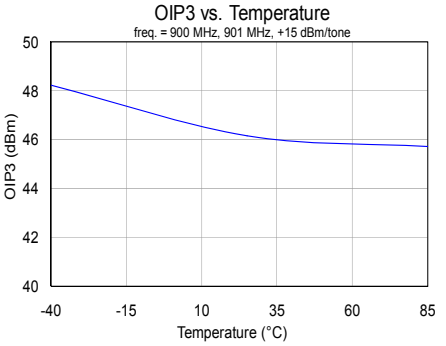


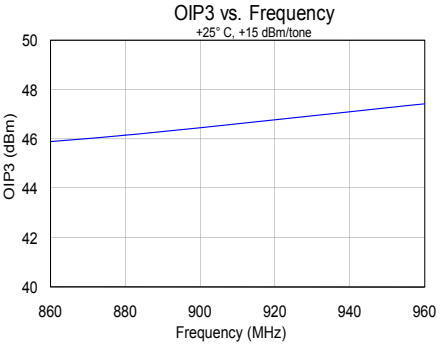




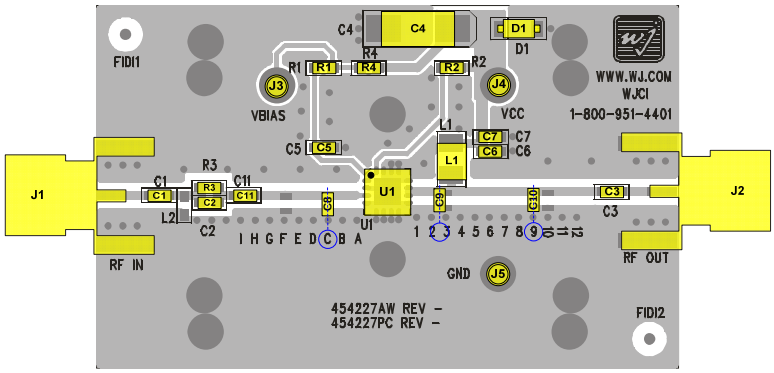






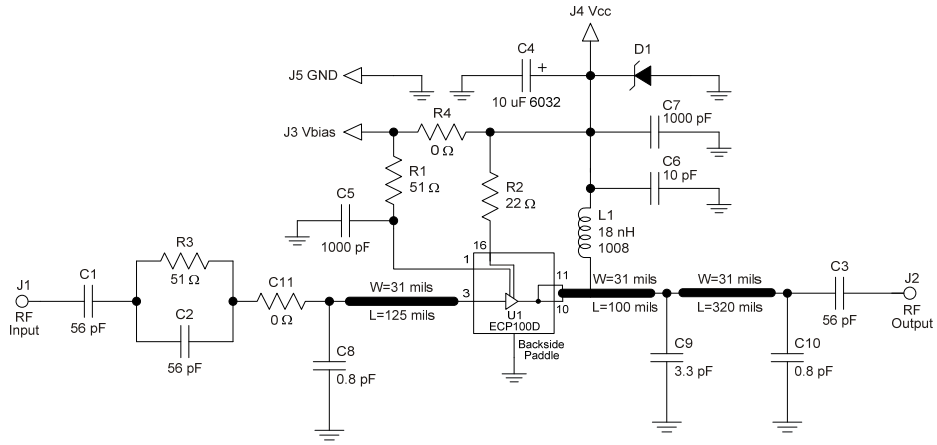


Reference Design 1930-1990 MHz (ECP100D-PCB1960)



Notes:

1. The primary RF microstrip line is 50 Ω.
2. All passive components are 0603 size unless otherwise specified.
3. Observe component value tolerances when specified.
4. Zero ohm jumpers may be replaced with metal trace in user applications.
5. Place component C8 at marker 'C' on the PC board or 125 mils from the center of C8 to left edge of U1. Electrical length; 13.6 deg. at 1.96 GHz.
6. Place component C9 between markers '2' and "3" on the PC board or 100 mils from the center of C9 to the right edge of U1. Electrical length; 10.9 deg. at 1.96 GHz.
7. Place component C10 at marker '9' on the PC board or 420 miles from the center of C10 to the right edge of U1. Electrical length; 45 deg. at 1.96 GHz.
8. Vbias is connected to Vcc by R4 for convenience. Remove R4 to apply Vbias independently.

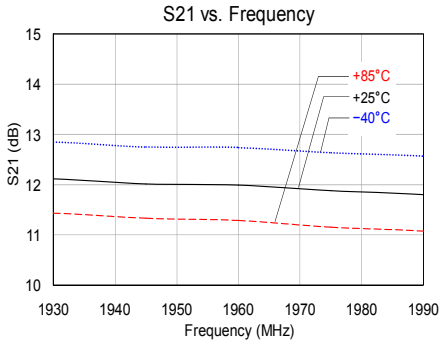


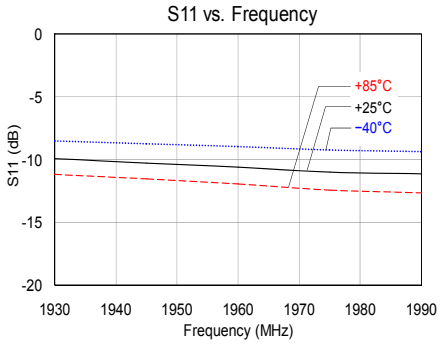
Bill of Material

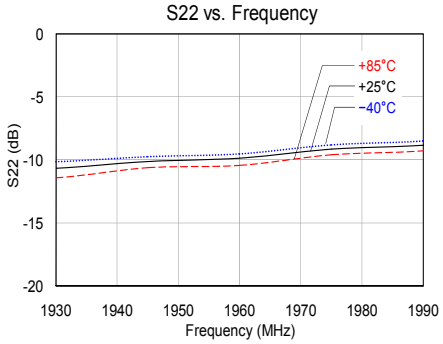
Ref Des	Value	Description	Manufacturer	Part Number
U1	N/A	1 Watt High Linearity InGaP Amp	TriQuint	ECP100D
C1, C2, C3	56 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C4	10 µF	Cap, Chip, 6032, 25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, 50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C8, C10	0.8 pF	Cap, Chip, 0603, 50 V, ±0.05 pF, Accu-P	AVX	06035J0R8ABSTR
C9	3.3 pF	Cap, Chip, 0603, 50 V, ±0.05 pF, Accu-P	AVX	06035J3R3ABSTR
L1	18 nH	Ind, Coil Wound, 1008, 5%, Ceramic Core	Coilcraft	1008HQ-18NXJLC
R1	51 Ω	Res, Chip, 0603, 1%, 1/16 W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R4, C11	0 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
D1	N/A	5.6 V Zener Diode	various	

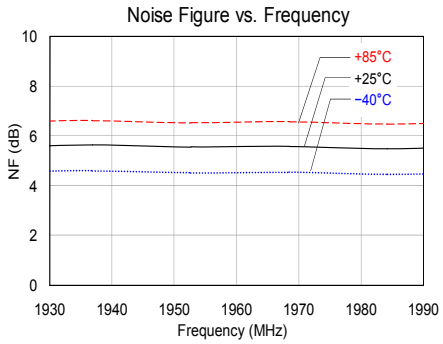
Typical Performance 1930-1990 MHz (ECP100D-PCB1960)

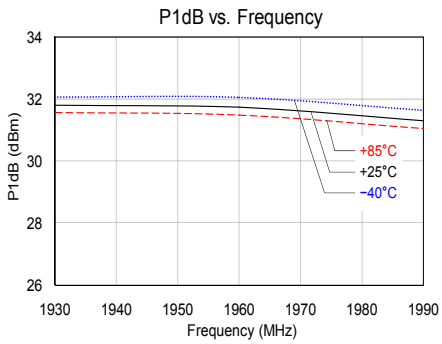
Frequency	MHz	1930	1960	1990
Gain	dB	12.1	12	11.8
Input Return Loss	dB	10	11	11
Output Return Loss	dB	11	10	9
Output P1dB	dBm	+32	+32	+31.5
Output IP3 +15 dBm / tone, 1 MHz spacing	dBm	+46	+46	+46
Channel Power @-45 dBc ACPR, IS-95 9 channels fwd	dBm	+25.5	+25.5	+25.5
Noise Figure	dB	5.5	5.5	5.5
Quiescent Current, Icq	mA	450		
Device / Supply Voltage	V	+5		

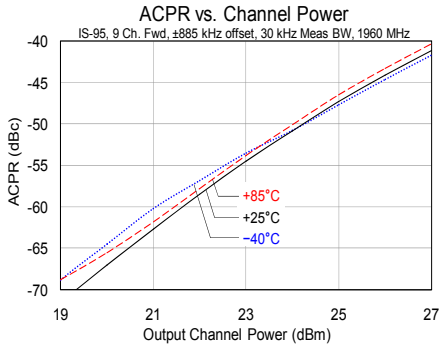


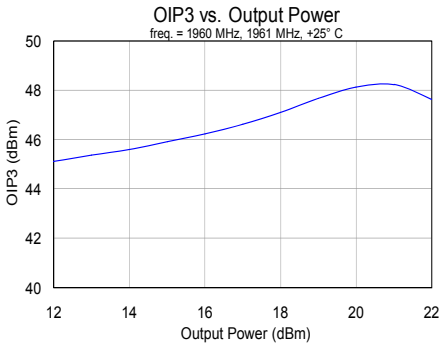


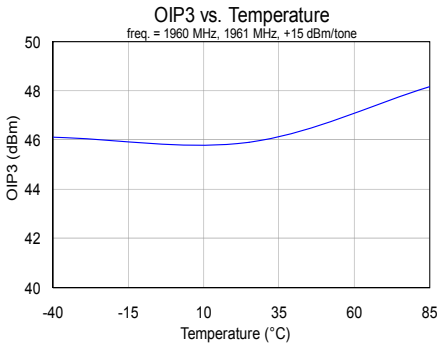


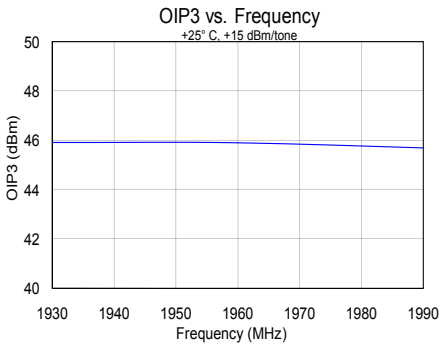




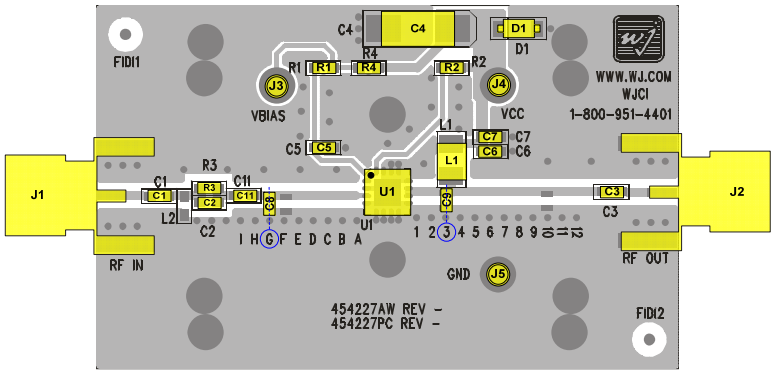






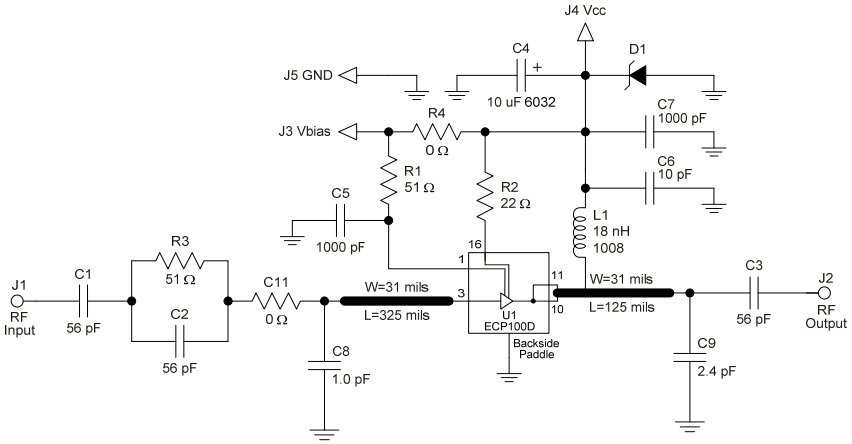


Reference Design 2110-2170 MHz (ECP100D-PCB2140)



Notes:

1. The primary RF microstrip line is 50 Ω.
2. All passive components are 0603 size unless otherwise specified.
3. Observe component value tolerances when specified.
4. Zero ohm jumpers may be replaced with metal trace in user applications.
5. Place component C8 at marker 'G' on the PC Board or 325 mils from the center of C8 to the left edge of U1. Electrical length; 38.5 deg. at 2.14 GHz.
6. Place component C9 at marker "3" on the PC Board or 125 mils from the center of C9 to the right edge of U1. Electrical length; 14.8 deg. at 2.14 GHz.
7. Vbias is connected to Vcc by R4 for convenience. Remove R4 to apply Vbias independently.

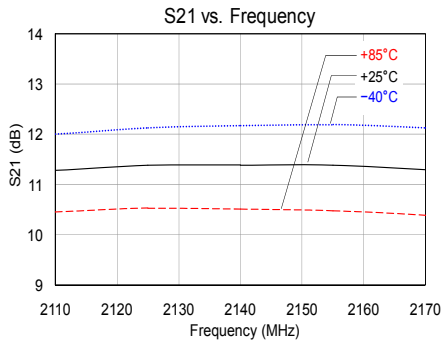


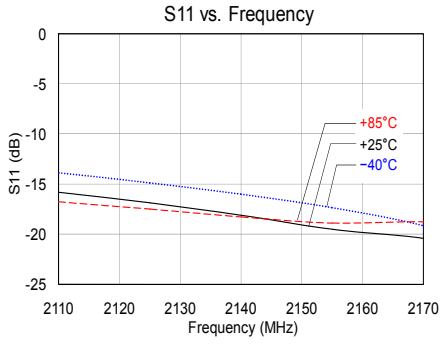
Bill of Material

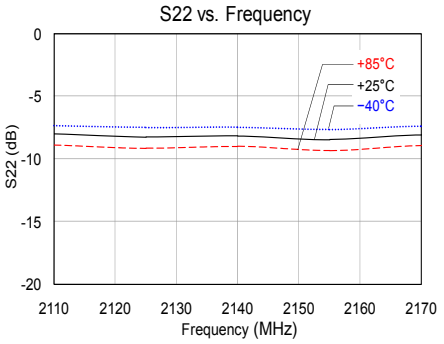
Ref Des	Value	Description	Manufacturer	Part Number
U1	N/A	1 Watt High Linearity InGaP Amp	TriQuint	ECP100D
C1, C2, C3	56 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C4	10 µF	Cap, Chip, 6032, 25 V, 20%, TANT	various	
C5, C7	1000 pF	Cap, Chip, 0603, 50 V, 5%, X7R	various	
C6	10 pF	Cap, Chip, 0603, 50 V, 5%, NPO/COG	various	
C8	1.0 pF	Cap, Chip, 0603, 50 V, ±0.05 pF, Accu-P	AVX	06035J1R0ABSTR
C9	2.4 pF	Cap, Chip, 0603, 50 V, ±0.05 pF, Accu-P	AVX	06035J2R4ABSTR
L1	18 nH	Ind, Coil Wound, 1008, 5%, Ceramic Core	Coilcraft	1008HQ-18NXJLC
R1	51 Ω	Res, Chip, 0603, 1%, 1/16 W	various	
R2	22 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R3	51 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
R4, C11	0 Ω	Res, Chip, 0603, 5%, 1/16 W	various	
D1	N/A	5.6 V Zener Diode	various	

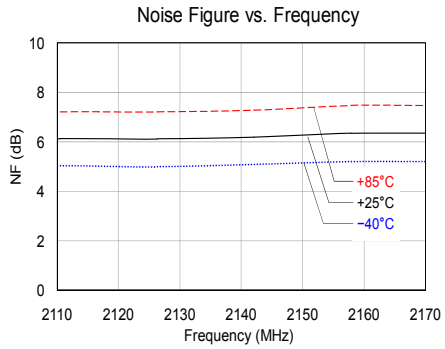
Typical Performance 2110-2170 MHz (ECP100D-PCB2140)

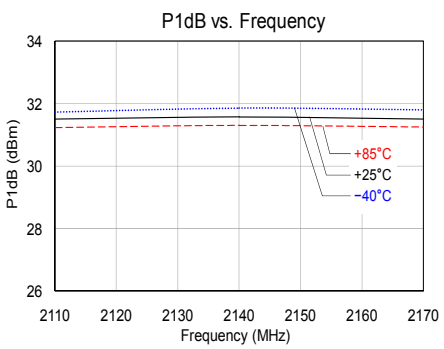
Frequency	MHz	2110	2140	2170
Gain	dB	11.3	11.4	11.3
Input Return Loss	dB	16	18	20
Output Return Loss	dB	8	8	8
Output P1dB	dBm	+31.5	+31.5	+31.5
Output IP3 +15 dBm / tone, 1 MHz spacing	dBm	+45.5	+45	+45
Channel Power @-45 dBc ACPR, IS-95 9 channels fwd	dBm	+23	+23	+23
Noise Figure	dB	6.1	6.2	6.3
Quiescent Current, Icq	mA	450		
Device / Supply Voltage	V	+5		

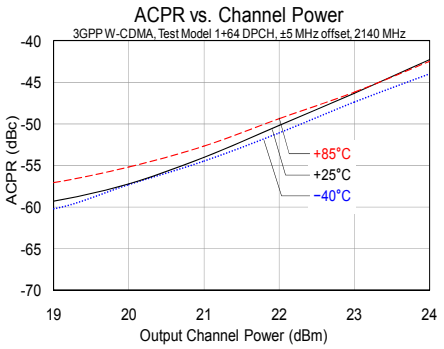


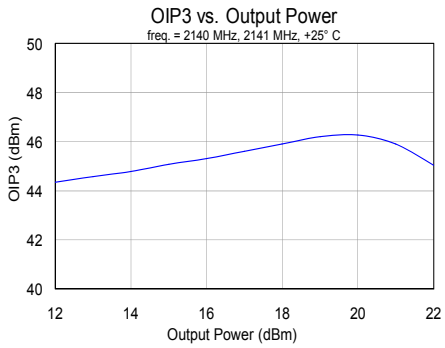


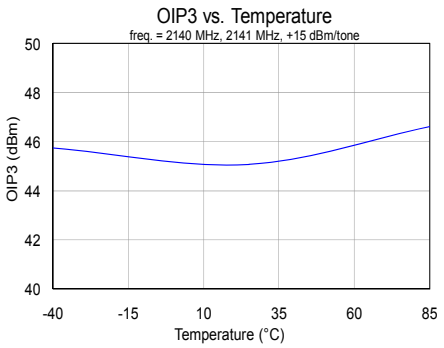


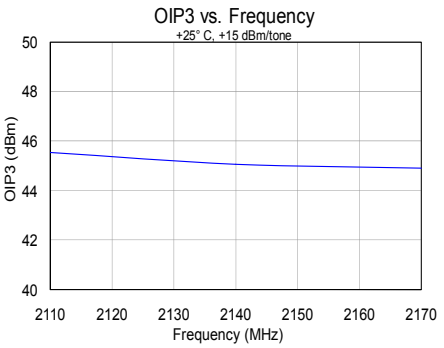










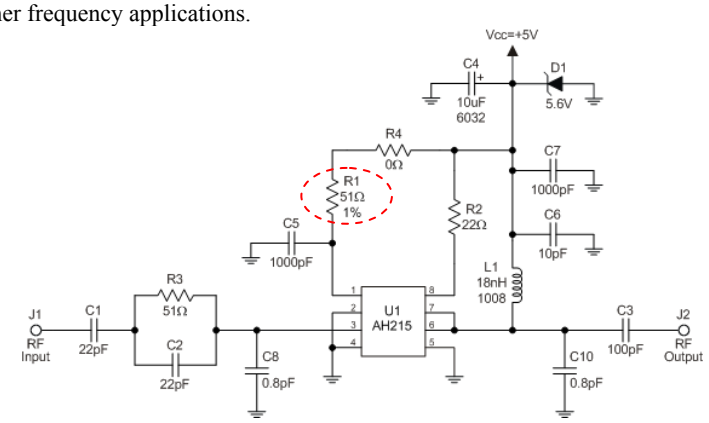


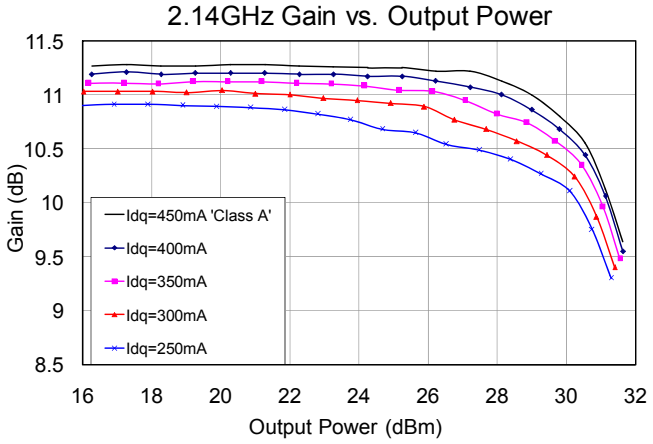
Applications Note: Reduced Bias Configurations

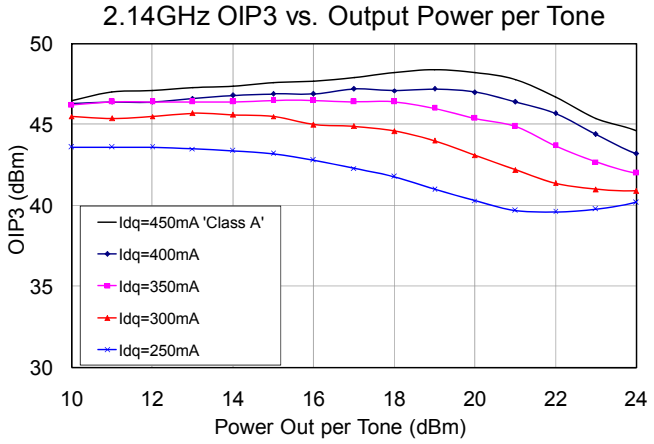
The ECP100D, like the AH215-S8, can be configured to operate with lower bias current by varying the bias-adjust resistor – R1. The recommended circuit configurations shown previously in this datasheet have the device operating in Class A operation. Lowering the current has little effect on the gain, OIP3, and P1dB performance of the device, but will slightly lower the ACLR/ACPR performance of the device as shown below. Presented below is AH215-S8PCB2140 RF performance as a function of bias current. Similar RF performance variation is expected for the ECP100D at 2140 MHz and at other frequency applications.

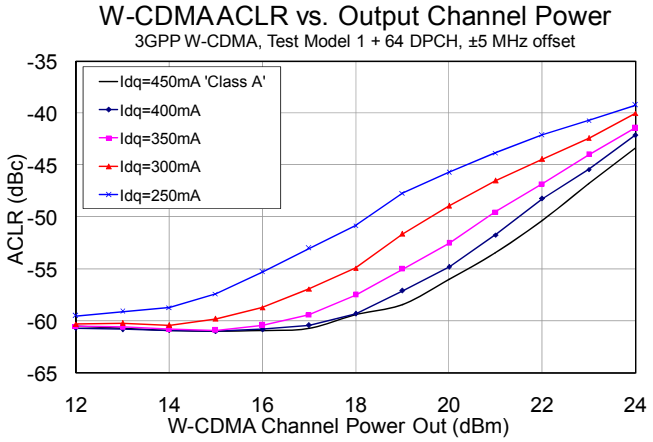
AH215-S8PCB2140 Performance Data

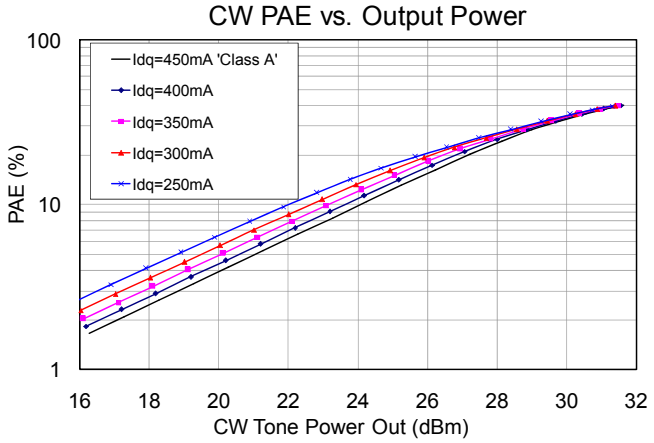
R1 (ohms)	Icq (mA)	Pdiss (W)	P1dB (dBm)	OIP3 (dBm)
51	450	2.25	+31.0	+47.1
68	400	2.00	+30.9	+46.4
100	350	1.75	+30.8	+46.4
130	300	1.50	+30.6	+45.5
180	250	1.25	+30.5	+43.6



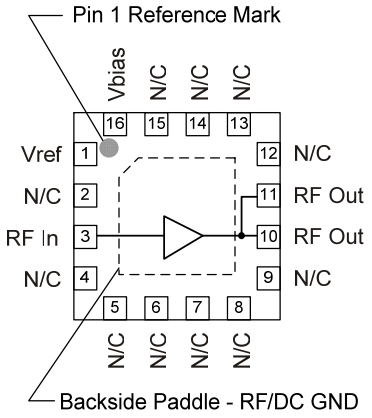








Pin Description



Pin	Symbol	Description
1	Vref	Sets reference current
2, 4, 5, 6, 7, 8, 9, 12, 13, 14, 15	N/C	No internal connection. These pins can be grounded or N/C on PCB. Land pads should be provided for PCB mounting integrity.
3	Input	RF Input. DC Voltage present, blocking cap required
10, 11	Output	RF Output. DC Voltage present, blocking cap required
16	Vbias	Voltage supply for active bias for the amp. Connect to same supply voltage as Vcc.
Backside Paddle	RF/DC GND	Use recommended via pattern shown on page 12 and ensure good solder attach for optimum thermal and electrical performance.

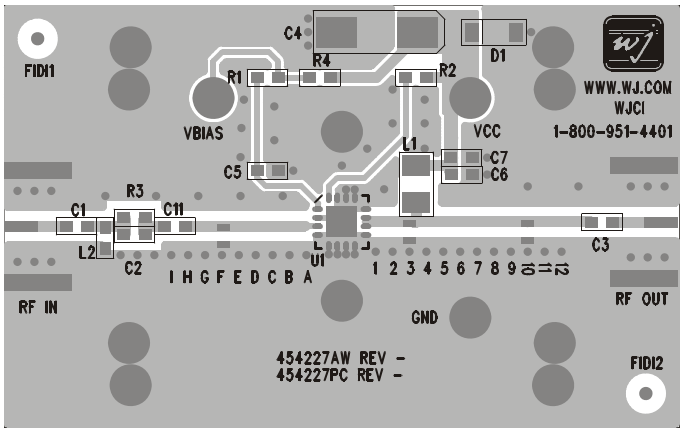
Applications Information

PC Board Layout

Circuit Board Material: Top RF layer is .014” Getek, 4 total layers (0.062” thick) for mechanical rigidity
1 oz copper, Microstrip line details: width = .026”, spacing = .026”

The silk screen markers ‘A’, ‘B’, ‘C’, etc. and ‘1’, ‘2’, ‘3’, etc. are used as place markers for the input and output tuning shunt capacitors – C8 and C9. The markers and vias are spaced in .050” increments.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



For further technical information, Refer to http://www.triquint.com/prodserv/more_info/default.aspx?prod_id=ECP100D

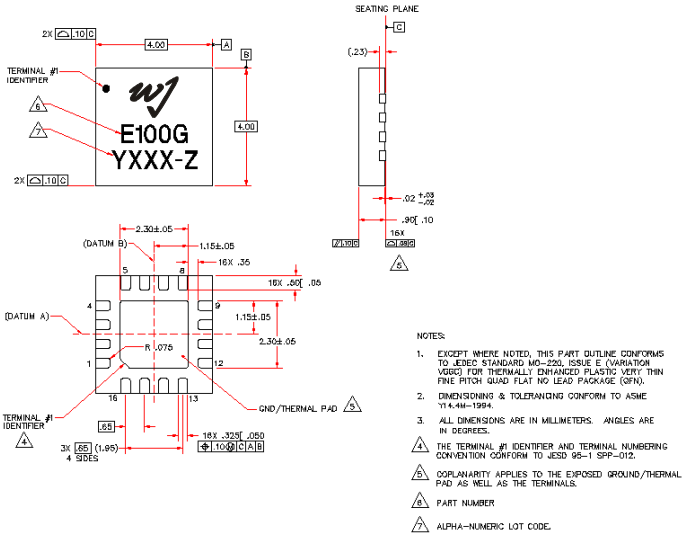
Mechanical Information

Package Information and Dimensions

This package is Lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes. The plating material on the pins is annealed matte tin over copper.

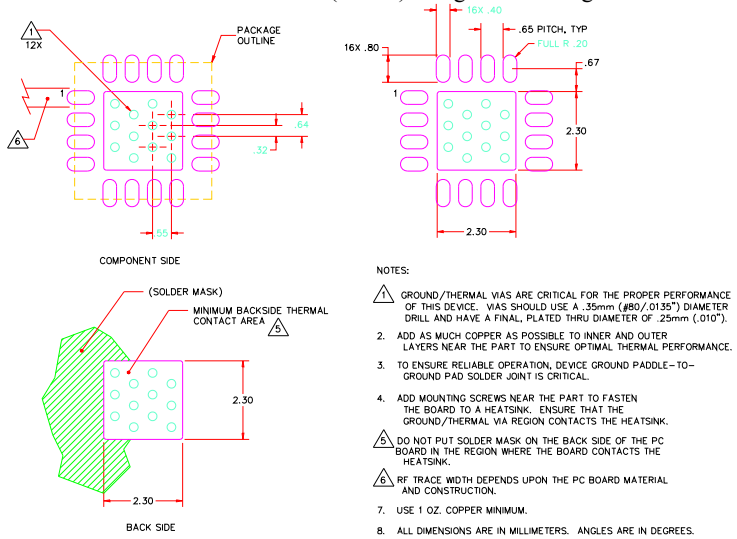
The ECP100D will be marked with an "E100G" designator with a with a lot code marked below the part designator. The "Y" represents the last digit of the year the part was manufactured, the "XXX" is an auto-generated number, and "Z" refers to a wafer number in a lot batch.

Tape and reel specifications for this part are located on the website in the "Application Notes" section.



Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. A heatsink underneath the area of the PCB for the mounted device is recommended for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1B
Value:	Passes ≥ 500 V to < 1000 V.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

Moisture Sensitivity

MSL Rating: Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcpplications.engineering@tqs.com

Important Notice

The information contained herein is believed to be reliable. TriQuint makes no warranties regarding the information contained herein. TriQuint assumes no responsibility or liability whatsoever for any of the information contained herein. TriQuint assumes no responsibility or liability whatsoever for the use of the information contained herein. The information contained herein is provided "AS IS, WHERE IS" and with all faults, and the entire risk associated with such information is entirely with the user. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for TriQuint products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information.
TriQuint products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.