
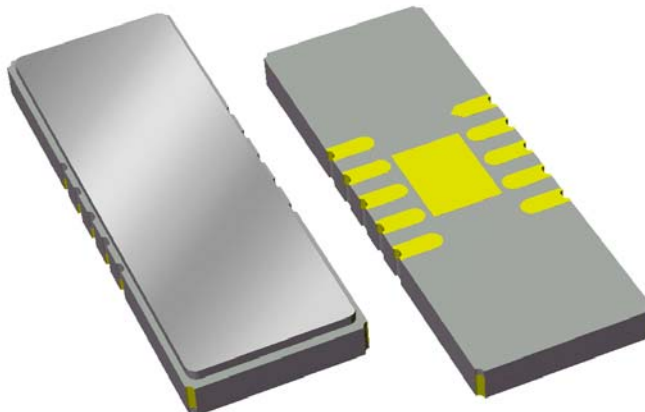


# Data Sheet

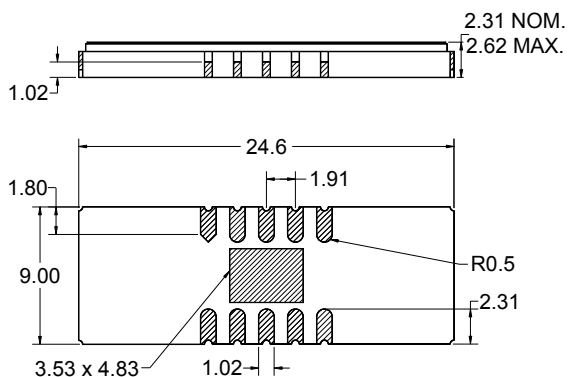
## Features

- For broadband applications
- Typical 3dB bandwidth of 1 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851545 (BW 3dB=1.5 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



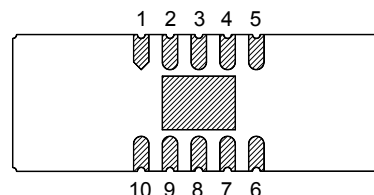
## Package

Surface Mount 24.60 x 9.00 x 2.31 mm



## Pin Configuration

Bottom View



Pin No.	Description
5	Output
10	Input
1,2,3,4	Case Ground
6,7,8,9	Case Ground

Dimensions shown are nominal in millimeters  
 All tolerances are  $\pm 0.15$ mm except overall  
 length  $\pm 0.20$ mm and width  $+0.13/-0.20$ mm

Body:  $Al_2O_3$  ceramic  
 Lid: Kovar, Ni plated  
 Terminations: Au plating 0.5 - 1.0 $\mu$ m,  
 over a 2 - 6 $\mu$ m Ni plating

# Data Sheet

## Electrical Specifications <sup>(1)</sup>

Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C

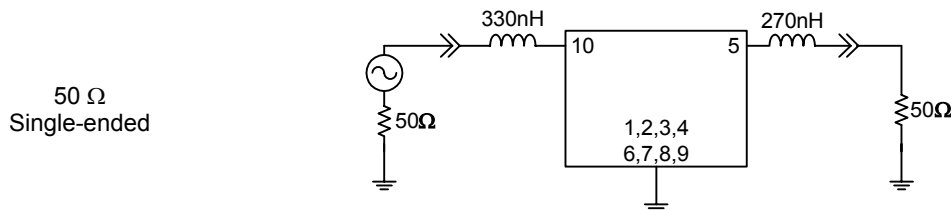
Parameter <sup>(3)</sup>	Minimum	Typical	Maximum	Unit
<b>Center Frequency</b>	-	70	-	MHz
<b>Minimum Insertion Loss</b>	-	21.6	23	dB
<b>Lower 1 dB Bandedge <sup>(4)</sup></b>	-	69.30	69.35	MHz
<b>Upper 1 dB Bandedge</b>	70.65	70.70	-	MHz
<b>Lower 3 dB Bandedge <sup>(4)</sup></b>	-	69.18	69.22	MHz
<b>Upper 3 dB Bandedge</b>	70.78	70.81	-	MHz
<b>Lower 40 dB Bandedge <sup>(4)</sup></b>	68.71	68.74	-	MHz
<b>Upper 40 dB Bandedge</b>	-	71.26	71.29	MHz
<b>Amplitude Variation</b> 69.35 - 70.65 MHz	-	0.64	1	dB p-p
<b>Phase Linearity</b> 69.35 - 70.65 MHz	-	2.4	5	deg p-p
<b>Group Delay Variation</b> 69.35 - 70.65 MHz	-	97	200	nsec
<b>Relative Attenuation <sup>(4)</sup></b>				
10 - 68 MHz	50	64	-	dB
72 - 110 MHz	50	60	-	dB
110 - 118 MHz	30	35	-	dB
118 - 124 MHz	50	66	-	dB
124 - 133 MHz	30	37	-	dB
133 - 200 MHz	50	66	-	dB
<b>Source Impedance <sup>(5)</sup></b>	-	50	-	Ω
<b>Load Impedance <sup>(5)</sup></b>	-	50	-	Ω
<b>Substrate Material</b>	-	Quartz	-	-

### Notes:

1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. All attenuation measurements are measured relative to minimum insertion loss
5. This is the optimum impedance in order to achieve the performance shown

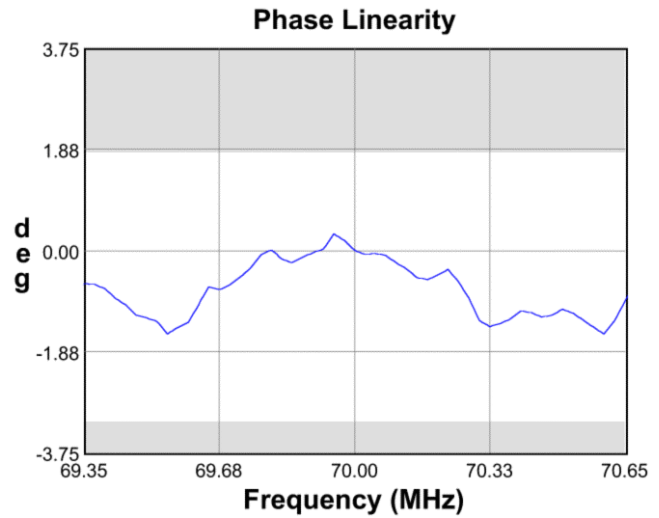
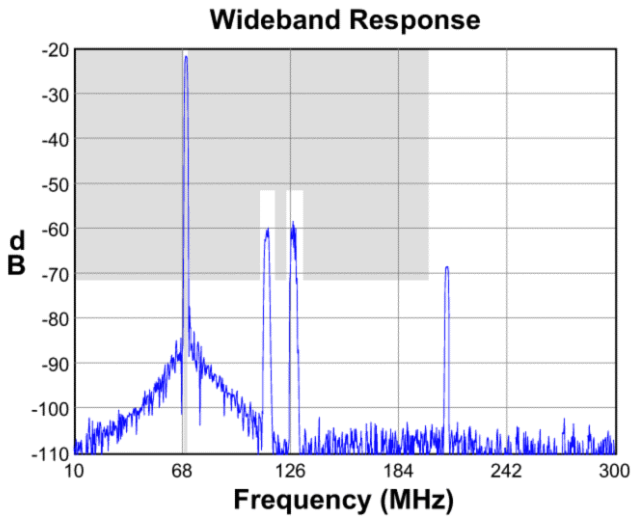
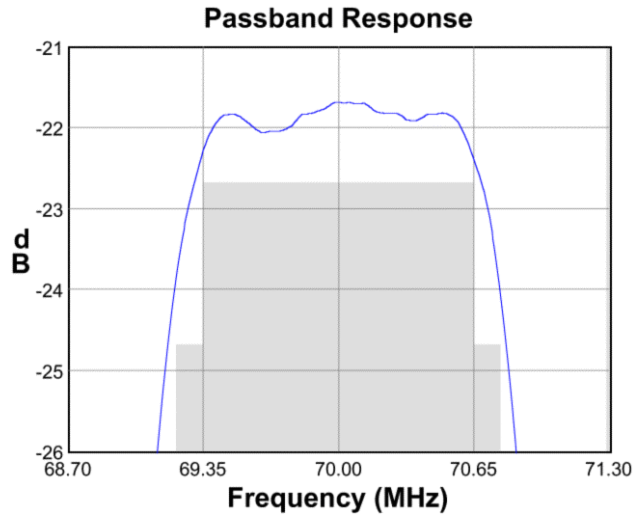
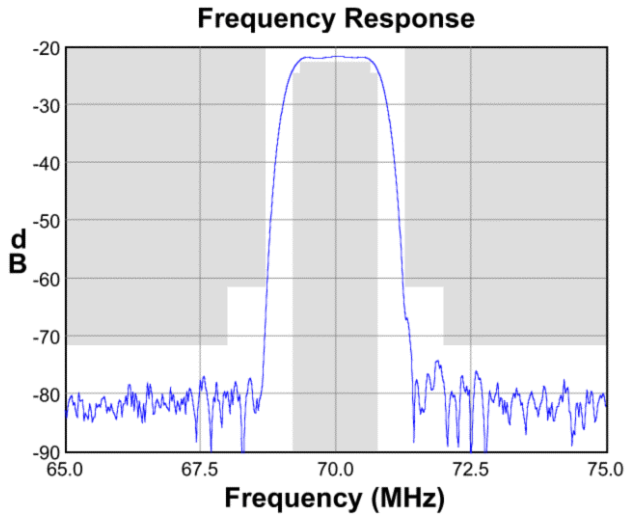
### Test Circuit:

Actual matching values may vary due to PCB layout and parasitics

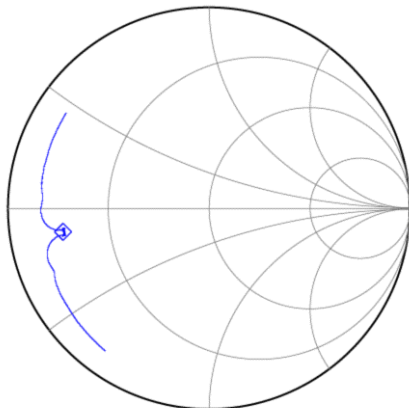


**Data Sheet**

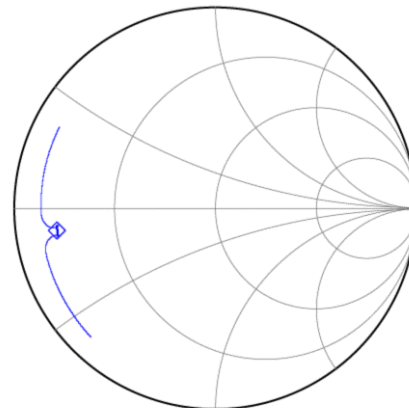
**Typical Performance (at +25°C)**



**Input Smith Chart**

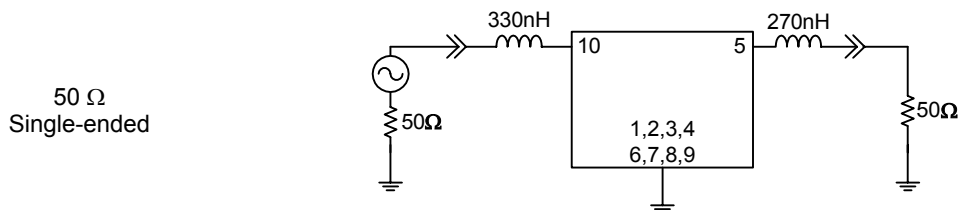


**Output Smith Chart**

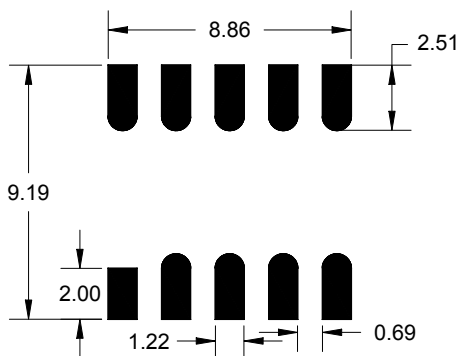
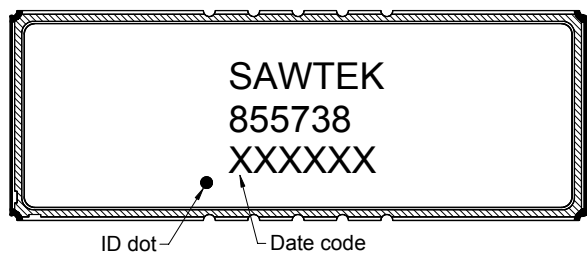


**Data Sheet**

**Matching Schematics**



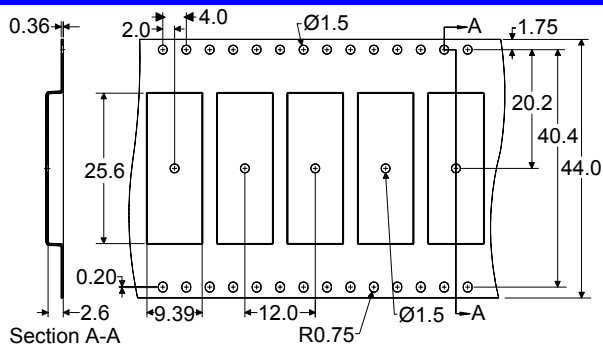
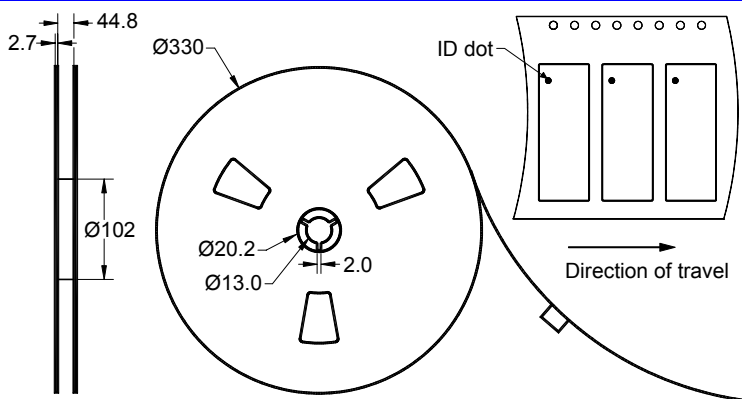
**Marking** **PCB Footprint**



Date code is the day of the current year in Julian format, last digit of the year, and hour of the day

This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**



Dimensions shown are nominal in millimeters  
Packaging quantity: 1000 units/reel


# Data Sheet

## Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	0	+70	°C
Storage Temperature Range	T <sub>stg</sub>	-40	+85	°C

## Important Notes

### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

### Solderability

- Compatible with JEDEC J-STD-020C **Pb-free** process, **260°C** peak reflow temperature ([see soldering profile](#))

## Links to Additional Technical Information

[PCB Layout Tips](#)
[Qualification Flowchart](#)
[Soldering Profile](#)
[S-Parameters](#)
[RoHS Information](#)
[Other Technical Information](#)

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