Product Specification

PE95421

Rad-Hard UltraCMOS® SPDT RF Switch Hermetically Sealed Ceramic Package 1 – 8500 MHz

Product Description

The PE95421 is an RF SPDT switch available in a hermetically sealed ceramic package and also available in die. It covers a broad range of applications from 1 to 8500 MHz and has been designed for use in various High Reliability (Hi-Rel) industries and applications requiring broadband performance. The PE95421 uses Peregrine's UltraCMOS® process and features HaRP™ technology enhancements to deliver high linearity and exceptional harmonics performance. HaRP technology is an innovative feature of the UltraCMOS® process providing upgraded linearity performance.

The PE95421 is an absorptive/non-reflective switch design which is an ideal termination method for RF elements in a system design. A single-pin 3.3V CMOS logic control in a single chip solution reduces the number of control lines.

Typical Industries

- Medical
- Automotive
- Telecom infrastructure
- Test instrumentation
- Down-hole oil/gas
- Military
- Space applications

Features

- HaRP™ technology enhanced
  - Eliminates gate and phase lag
  - No insertion loss or phase drift
- High linearity: 60 dBm IIP3
- Low insertion loss
  - 0.77 dB @ 100 MHz
  - 1.00 dB @ 3000 MHz
  - 1.15 dB @ 6000 MHz
  - 1.38 dB @ 8500 MHz
- High isolation (RF1-RF2)
  - 86.5 dB @ 100 MHz
  - 48.2 dB @ 3000 MHz
  - 36.6 dB @ 6000 MHz
  - 27.8 dB @ 8500 MHz
- Fast switching time
  - 700 ns RF ON
  - 700 ns RF OFF
- Low power consumption: 3.3 μW @ 3.3V
- 1 dB compression point of +33 dBm
- Single-pin 3.3V CMOS logic control
- ESD tolerant to 1000V HBM
- Absorptive/non-reflective
- Offered in a 7-lead hermetic CQFP surface-mount package and in DIE form

Figure 1. Functional Diagram

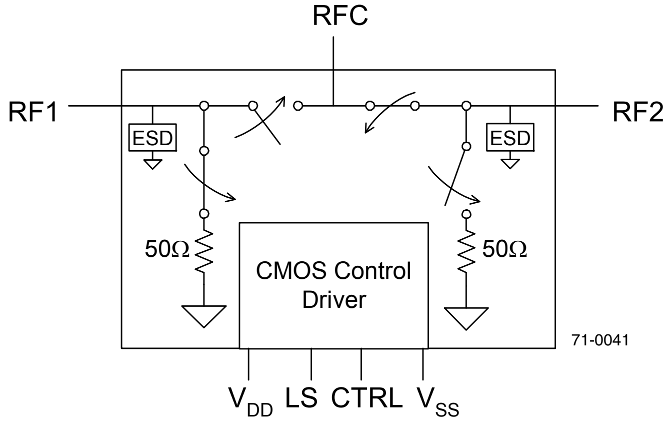


Figure 2. Package Type
7-lead CQFP

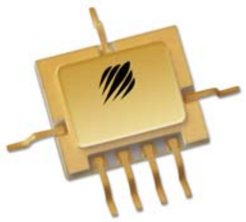


Table 1. Electrical Specifications @ -40°C $\leq$ T $\leq$ 85°C, 3.0V $\leq V_{DD} \leq$ 3.6V and -3.0V $\leq V_{SS} \leq$ -3.6V

Parameter	Condition	Min	Typ	Max	Unit
Operational frequency		1		8500	MHz
Insertion loss	100 MHz		0.77	0.95	dB
	3000 MHz		1	1.28	dB
	6000 MHz		1.15	1.42	dB
	8500 MHz		1.38	1.72	dB
Isolation – RFC to RF1	100 MHz	74	75.6		dB
	3000 MHz	46	47.4		dB
	6000 MHz	43.8	48		dB
	8500 MHz[2]	31	38		dB
Isolation – RFC to RF2	100 MHz	73.7	75.4		dB
	3000 MHz	46.8	48.3		dB
	6000 MHz	45	52.1		dB
	8500 MHz[2]	31	38		dB
Isolation – RF1 to RF2	100 MHz		86.5		dB
	3000 MHz		48.2		dB
	6000 MHz		36.6		dB
	8500 MHz		27.8		dB
Return loss active port – ON state	100 MHz		21		dB
	3000 MHz		33		dB
	6000 MHz		20		dB
	8500 MHz		15		dB
Return loss active port – OFF state	100 MHz		20		dB
	3000 MHz		18		dB
	6000 MHz		15		dB
	8500 MHz		8		dB
Input 1 dB compression[1]	100 – 8500 MHz		33		dBm
Input IP3	100 – 8500 MHz, 18 dBm input power/tone		60		dBm
Switching time	50% CTRL to 90% of final value when RF ON		700		ns
	50% CTRL to 10% of final value when RF OFF		700		ns

Notes: 1. Please note maximum operating P_{IN} (50Ω) of +24 dBm in *Table 4*
2. Guaranteed but not tested

Figure 3. Pin Layout (Top View)

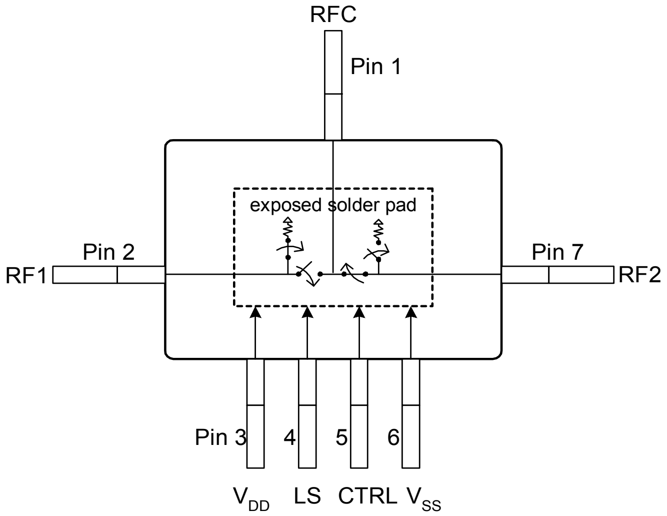


Table 2. Pin Descriptions

Pin #	Pin Name	Description
1	RFC[1]	RF common
2	RF1[1]	RF port
3	V_{DD}	Supply voltage (nominal 3.3V)
4	LS	Selects the RF1 to RFC path or RF2 to RFC (See *Table 6*)
5	CTRL	Unused (See *Table 6*)
6	V_{SS}	Negative power supply. Apply nominal – 3.3V supply
7	RF2[1]	RF port
Pad	GND[2]	Exposed pad: Grounded for proper operation

Notes: 1. All RF pins must be DC blocked with an external series capacitor or held at 0V DC
2. Must be soldered to PCB RF ground for proper operation

Table 3. Operating Ranges

Symbol	Parameter/Condition	Min	Typ	Max	Unit
V_{DD}	Positive supply voltage	3.0	3.3	3.6	V
V_{SS}	Negative supply voltage	-3.6	-3.3	-3.0	V
I_{DD}	Supply current (V_{DD} = 3.3V, LS or CTRL = 3.3V)		1		µA
I_{SS}	Supply current (V_{SS} = -3.3V)		1		µA
	Control voltage high	0.7xV_{DD}			V
	Control voltage low			0.3xV_{DD}	V
T_{OP}	Operating temperature range	-40		85	°C
P_{IN}	RF Power In (50Ω): 1 MHz $\le$ 8.5 GHz			24	dBm

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	-0.3	4.0	V
V_{C1}	Voltage on LS input	-0.3	V_{DD}+ 0.3	V
V_{C2}	Voltage on CTRL input	-0.3	V_{DD}+ 0.3	V
Θ_{JC}	Theta JC		24	°C/W
T_{ST}	Storage temperature range	-65	150	°C
V_{ESD}	ESD voltage HBM[1], all pins		1000	V

Note 1: Human Body Model (MIL-STD-883 Method 3015)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified.

Latch-Up Immunity

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Table 5. Truth Table

LS	CTRL	RFC–RF1	RFC–RF2	Logic State
0	X	off	on	RF2 active
1	X	on	off	RF1 active

Switching Frequency

The PE95421 has a maximum 25 kHz switching rate.

Table 6. Post Radiation Table

Total Dose	Parameter	Min	Max	Unit
Post 100 kRAD	I_{DD} Positive supply current		10	µA
	I_{SS} Negative supply current	-10		µA

Table 7. Single Event Effects

SEE Mode	Effective linear energy transfer (LET)
SEL/SEB/SEGR	90 MeV•mg/cm^2
SEFI	90 MeV•mg/cm^2
SEU	90 MeV•mg/cm^2
SET	90 MeV•mg/cm^2

SEL, SEB, SEGR, SEFI, SEU: None observed, Au/60 degrees
SET: No events exceeding ± 10 mV transient observed

ELDRS

UltraCMOS® devices do not include bipolar minority carrier elements and; therefore, do not exhibit enhanced low-dose-rate sensitivity.

Typical Performance Data

Figure 4. Insertion Loss: RF1 @ $V_{DD} = -V_{SS} = 3.3V$

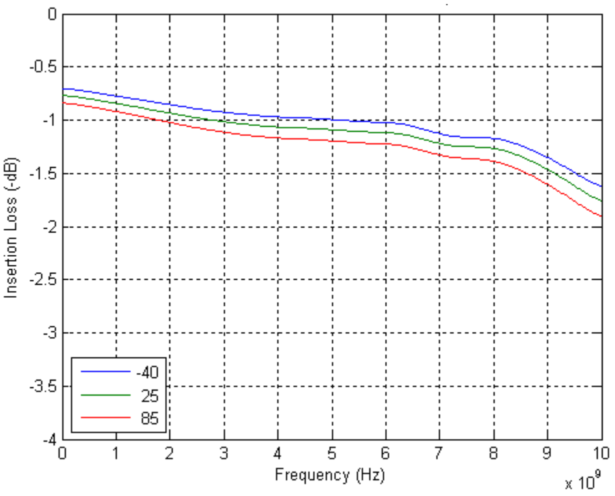


Figure 5. Insertion Loss: RF1 @ 25°C

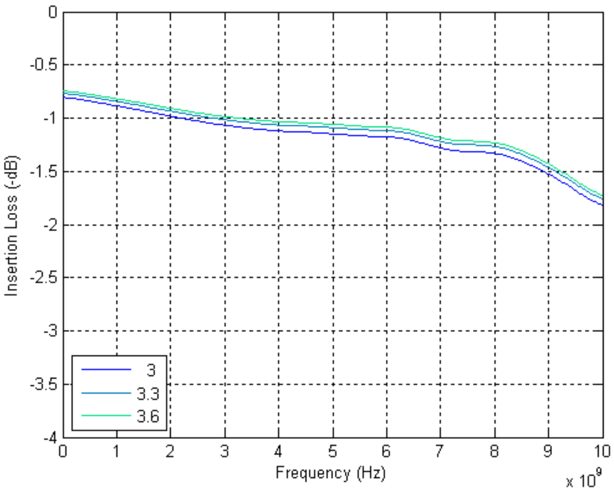


Figure 6. Insertion Loss: RF2 @ $V_{DD} = -V_{SS} = 3.3V$

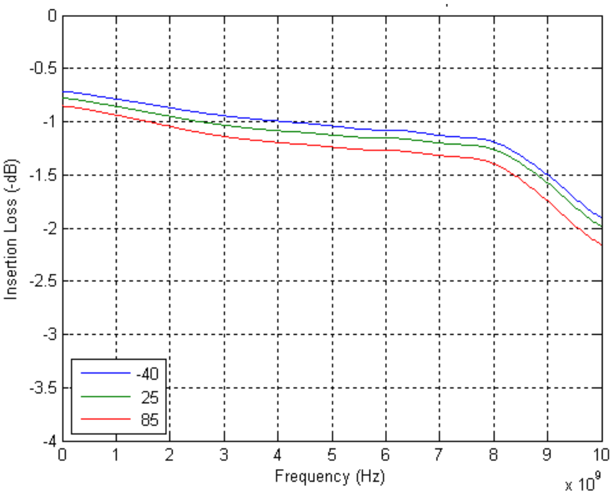
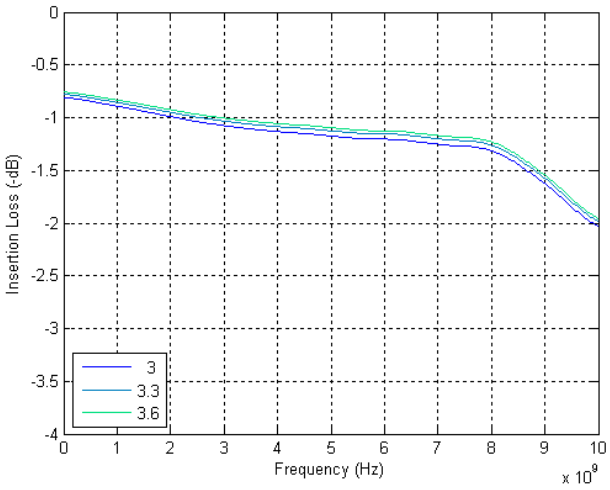


Figure 7. Insertion Loss: RF2 @ 25°C



Typical Performance Data (continued)

Figure 8. Isolation: RF1–RF2, RF1 Active @ V_{DD} = -V_{SS} = 3.3V

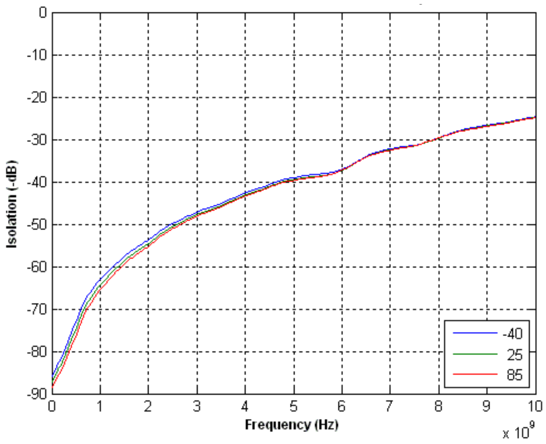


Figure 9. Isolation: RF2–RF1, RF2 Active @ V_{DD} = -V_{SS} = 3.3V

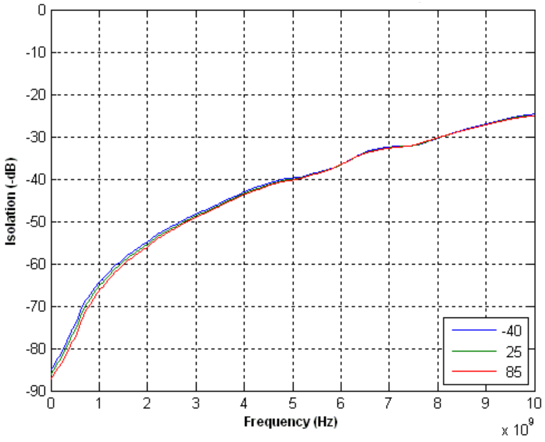


Figure 10. Isolation: RF1–RF2, RF1 Active @ 25°C

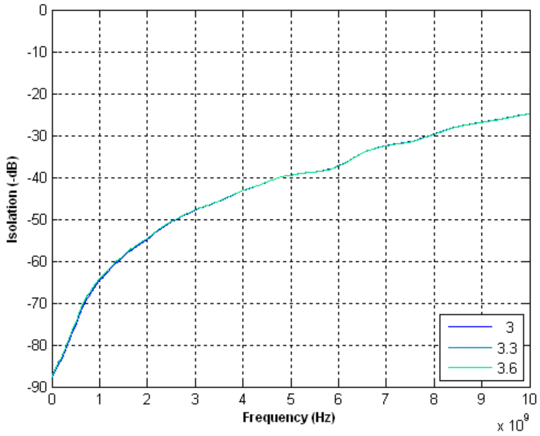


Figure 11. Isolation: RF2–RF1, RF2 Active @ 25°C

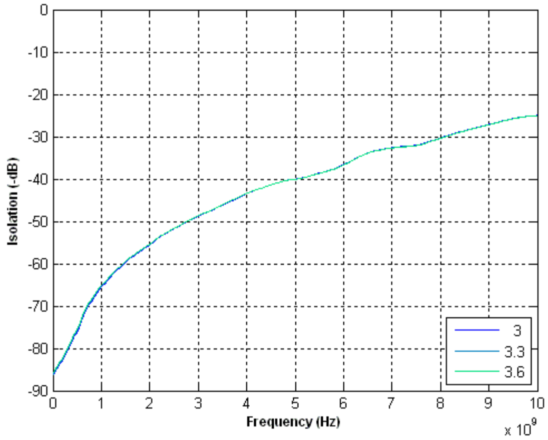


Figure 12. Isolation: RFC–RF1, RF2 Active @ V_{DD} = -V_{SS} = 3.3V

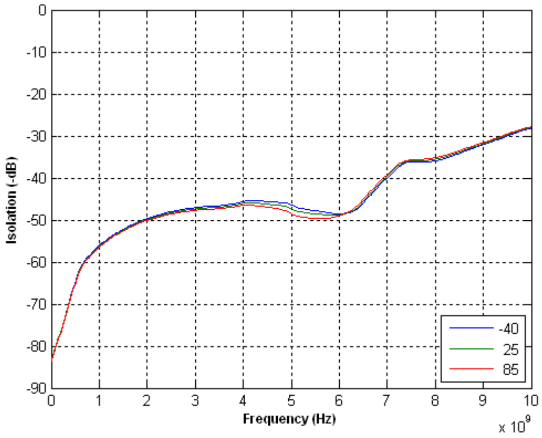
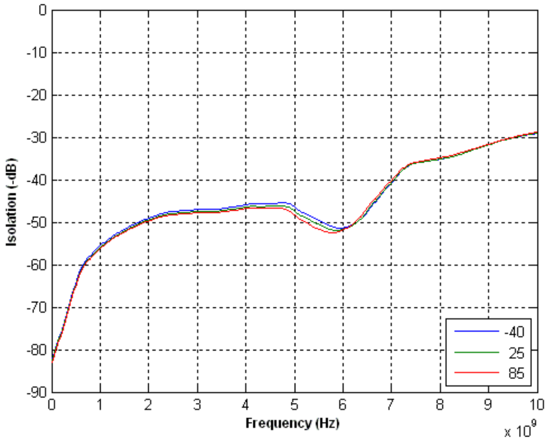


Figure 13. Isolation: RFC–RF2, RF1 Active @ V_{DD} = -V_{SS} = 3.3V



Typical Performance Data (continued)

Figure 14. Isolation: RFC–RF1, RF2 Active @ 25°C

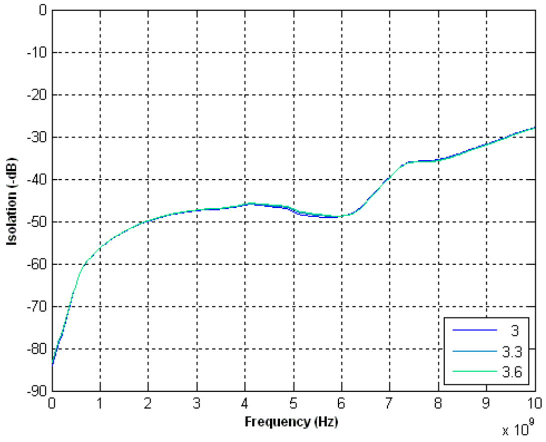


Figure 15. Isolation: RFC–RF2, RF1 Active @ 25°C

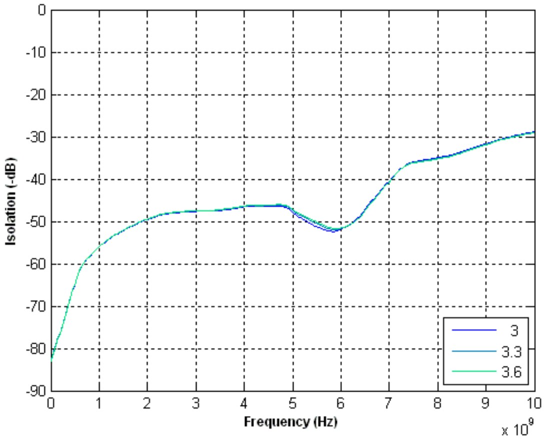


Figure 16. Isolation: RFC–RF1, OFF state @ V_{DD} = -V_{SS} = 3.3V

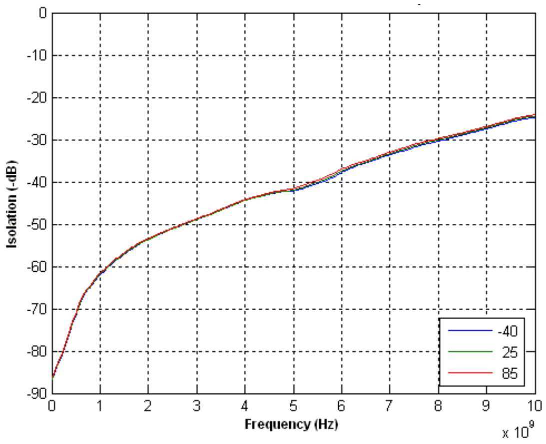


Figure 17. Isolation: RFC–RF2, OFF state @ V_{DD} = -V_{SS} = 3.3V

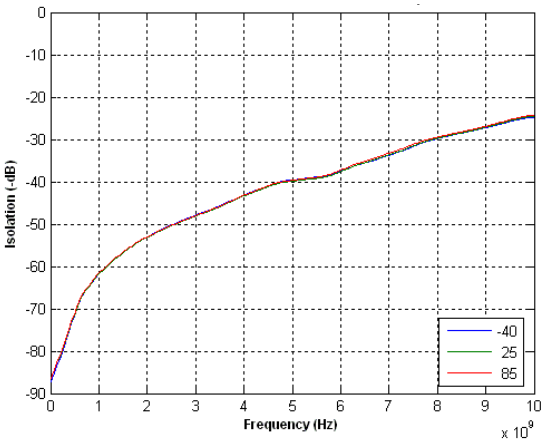


Figure 18. Isolation: RFC–RF1, OFF state @ 25°C

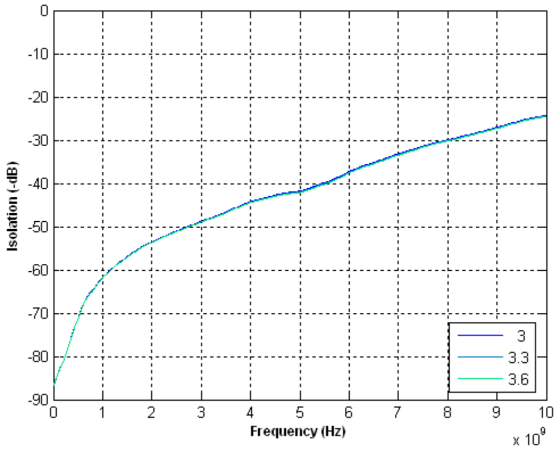
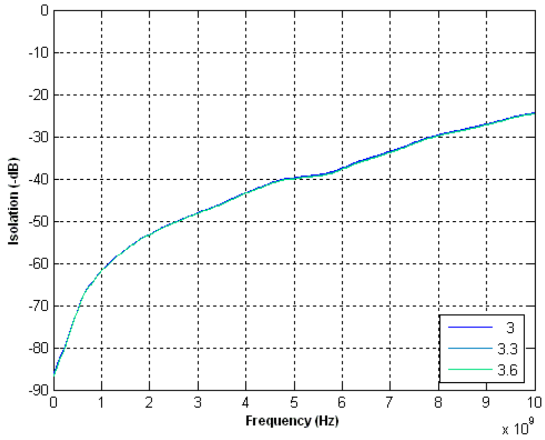


Figure 19. Isolation: RFC–RF2, OFF state @ 25°C



Typical Performance Data (continued)

Figure 20. Return Loss: RF1 @ $V_{DD} = -V_{SS} = 3.3V$

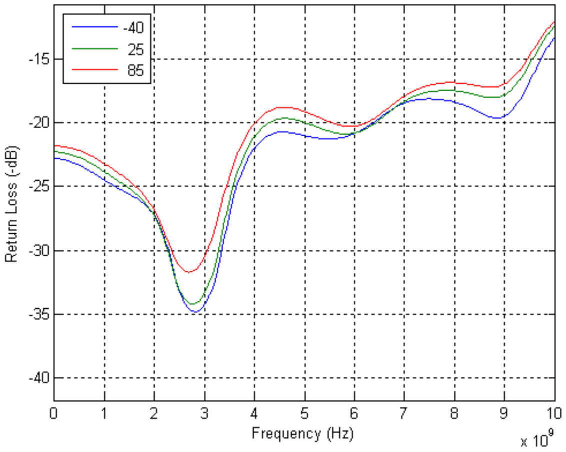


Figure 21. Return Loss: RF2 @ $V_{DD} = -V_{SS} = 3.3V$

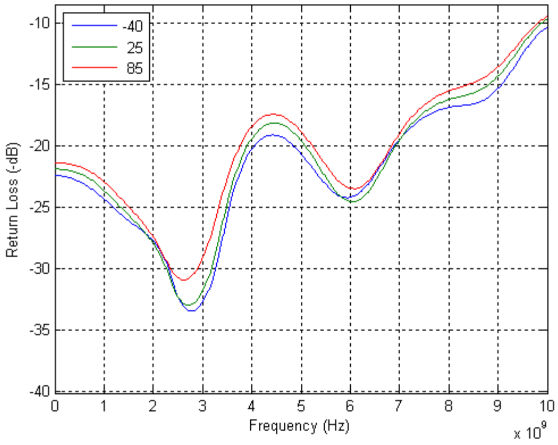


Figure 22. Return Loss: RF1 @ 25°C

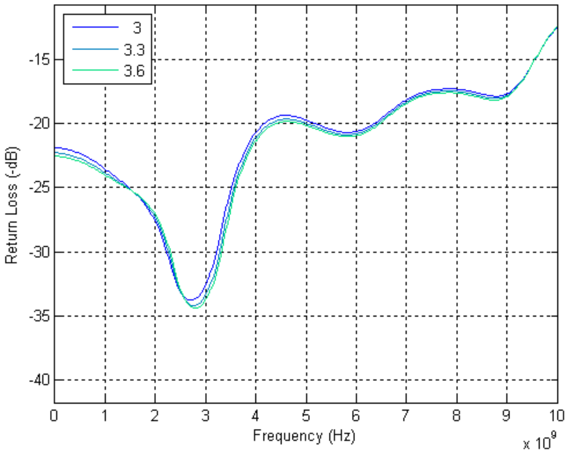
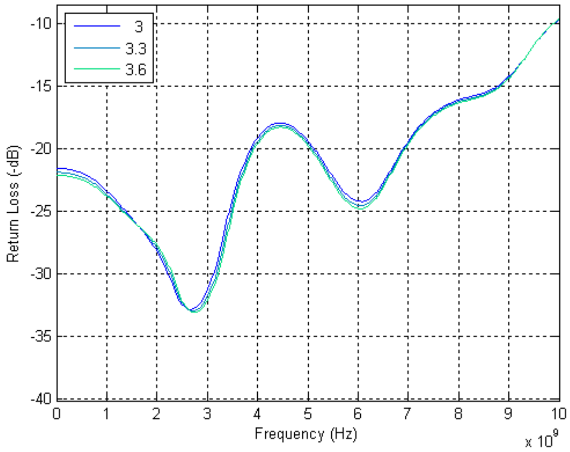


Figure 23. Return Loss: RF2 @ 25°C

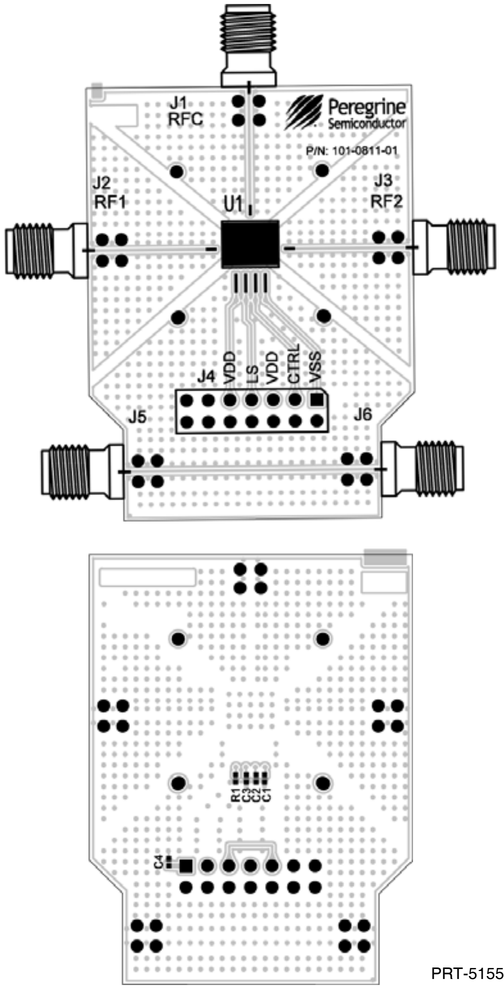


Evaluation Board

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE95421. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

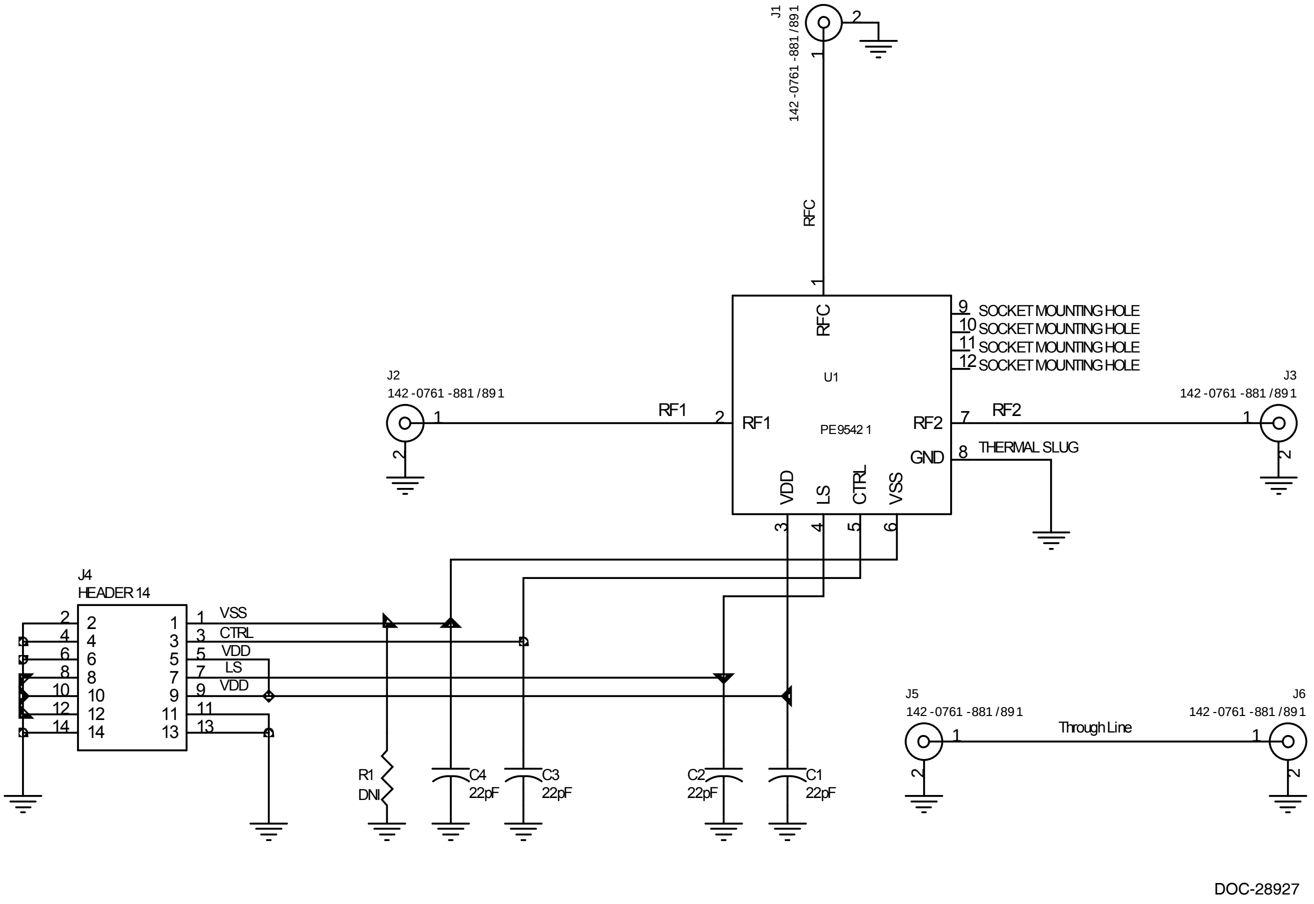
The evaluation kit board is constructed of four metal layers. The dual clad top RF layer is Rogers RO4003 material with an 8 mil RF core and er = 3.55. The other two dielectric layers are FR4 for DC control and overall board strength with an cumulative board thickness of 62 mils. The RF transmission lines were designed using a Grounded co-planar waveguide with a linewidth of 15 mils and gap of 7 mils.

Figure 24. Evaluation Board Layout



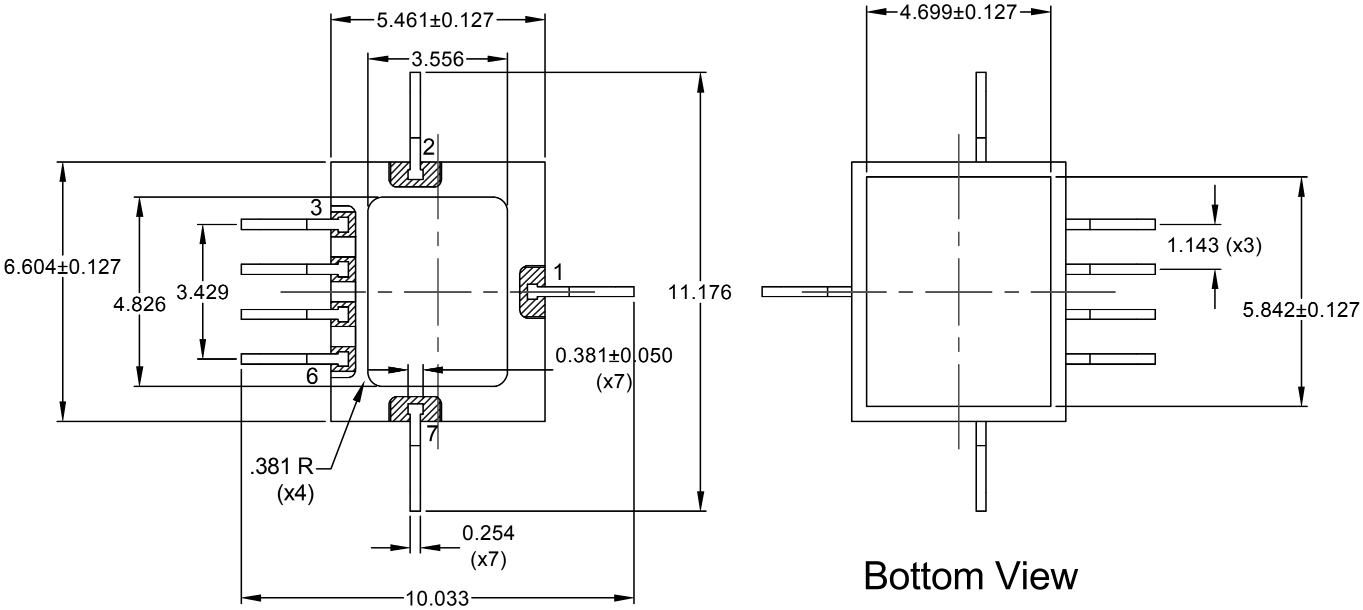
PRT-51554

Figure 25. Evaluation Kit Schematic



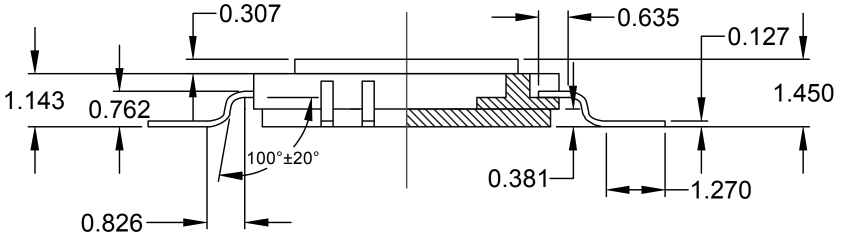
Notes:
1. Use PRT-51554 PCB
2. Caution: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD)
3. All transmission lines are 15 mil width, 7 mil gaps, 8 mil core dielectric

Figure 26. Package Drawing
7-lead CQFP



Bottom View

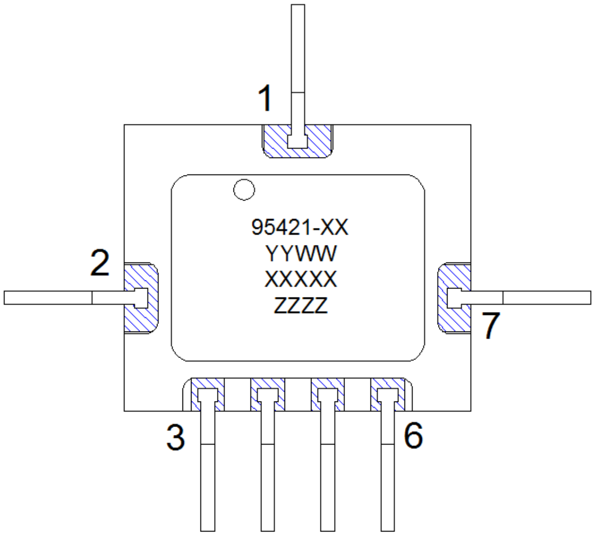
Top View



Side View

DOC-50612

Figure 27. Top Marking Specification



○ = Pin 1 indicator
95421-XX = Part number (XX will be specified by the PO and/or the assembly instructions)
YYWW = Date code, last two digits of the year and work week
XXXXX = Lot code (up to seven digits)
ZZZZ = Serial number (up to six digits)

PRT-24929

Table 8. Ordering Information

Order Code	Description	Package	Shipping Method
95421-01[1]	Engineering samples	7-lead CQFP	18 Units / tray
95421-11	Flight units	7-lead CQFP	18 Units / tray
95421-99[2]	Flight die	Die	400 Units / waffle pack
95421-00	Evaluation kit	Evaluation board	1 / Box

Notes: 1. The PE95421-01 devices are ES (Engineering Sample) prototype units intended for use as initial evaluation units for customers of the PE95421-11 flight units. The PE95421-01 device provides the same functionality and footprint as the space qualified device, and intended for engineering evaluation only. They are tested at 25°C only and processed to a non-compliant flow (e.g. No burn-In, etc.). These units are not suitable for qualification, production, radiation testing or flight use.
2. For all die products, limited electrical testing performed. Contact sales@psemi.com before ordering.

Sales Contact and Information

For sales and contact information please visit www.psemi.com.

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