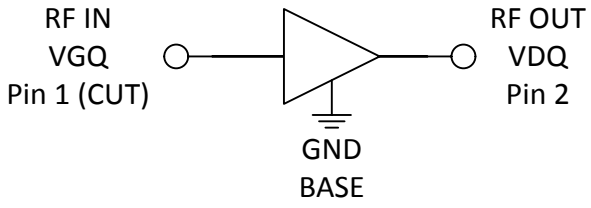
RFG1M20180

180W GaN Power Amplifier
1.8GHz to 2.2GHz

The RFG1M20180 is optimized for commercial infrastructure applications in the 1.8GHz to 2.2GHz frequency band, ideal for WCDMA and LTE applications. Using an advanced 48V high power density gallium nitride (GaN) semiconductor process optimized for high peak to average ratio applications, these high-performance amplifiers achieve high efficiency and flat gain over a broad frequency range in a single amplifier design. The RFG1M20180 is an input matched GaN transistor packaged in an air cavity ceramic package, which provides excellent thermal stability. Ease of integration is accomplished through the incorporation of simple, optimized matching networks external to the package that provide wideband gain, efficiency, and linearizable performance in a single amplifier.



Functional Block Diagram

Package: Flanged Ceramic, 2-Pin, RF400-2

Features

- Advanced GaN HEMT Technology
- Typical Peak Modulated Power >180W
- Advanced Heat-Sink Technology
- Single Circuit for 1.8GHz to 2.2GHz
- 48V Operation Typical Performance
  - P_{OUT} = 45.5dBm
  - Gain = 15dB
  - Drain Efficiency = 31%
  - ACP = -38dBc
  - Linearizable to -55dBc with DPD
- -25°C to 85°C Operating Temperature
- Optimized for Video Bandwidth and Minimized Memory Effects
- RF Tested for 3GPP Performance
- RF Tested for Peak Power Using IS95
- Large Signal Models Available

Applications

- Commercial Wireless Infrastructure
- High Efficiency Doherty
- High Efficiency Envelope Tracking

Ordering Information

RFG1M20180S2	Sample bag with 2 pieces
RFG1M20180SB	Bag with 5 pieces
RFG1M20180SQ	Bag with 25 pieces
RFG1M20180SR	Short Reel with 50 pieces
RFG1M20180TR13	13” Reel with 300 pieces
RFG1M20180PCBA-410	Evaluation Board

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS130822

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to +2	V
Gate Current (I_G)	108.5	mA
Operational Voltage	48	V
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-65 to +125	°C
Operating Temperature Range (T_L)	-25 to 85	°C
Operating Junction Temperature (T_J)	200	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C, 95% Confidence Limits)*	3E + 06	Hours
Thermal Resistance, R_{TH} (junction to case) measured at T_C = 85°C, DC bias only	1.4	°C/W

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

* MTTF – Median time to failure as determined by the process technology wear-out failure mode. Refer to product qualification report for FIT (random) failure rate.

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table below.

Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C) / R_{TH\ J-C}$ and $T_C = T_{CASE}$

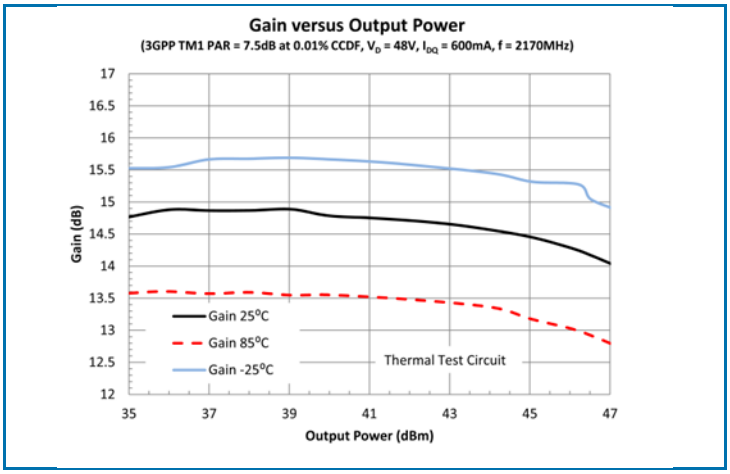
Nominal Operating Parameters

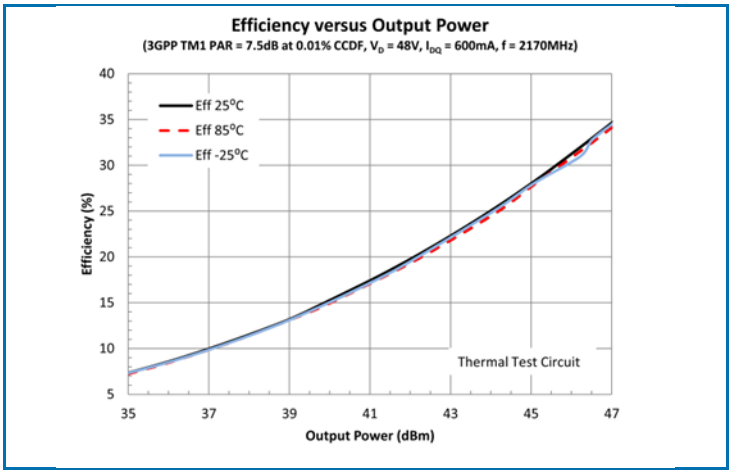
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})	28		48	V	
Gate Voltage (V_{GSQ})	-3.5	-3	-2.5	V	
Drain Bias Current		600		mA	
Frequency of Operation	1.8		2.2	GHz	
Capacitance					
C_{RSS}		9.6		pF	V_G = -8V, V_D = 0V
C_{ISS}		125		pF	
C_{OSS}		28.5		pF	
DC Functional Tests					
$I_{G\ (OFF)}$ - Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D\ (OFF)}$ - Drain Leakage, Operation Voltage			7	mA	V_G = -8V, V_D = 48V
$I_{D\ (OFF)}$ - Drain Leakage, High Voltage			7	mA	V_G = -8V, V_D = 175V
$V_{GS\ (TH)}$ - Threshold Voltage		-3.7		V	V_D = 48V, I_D = 14mA

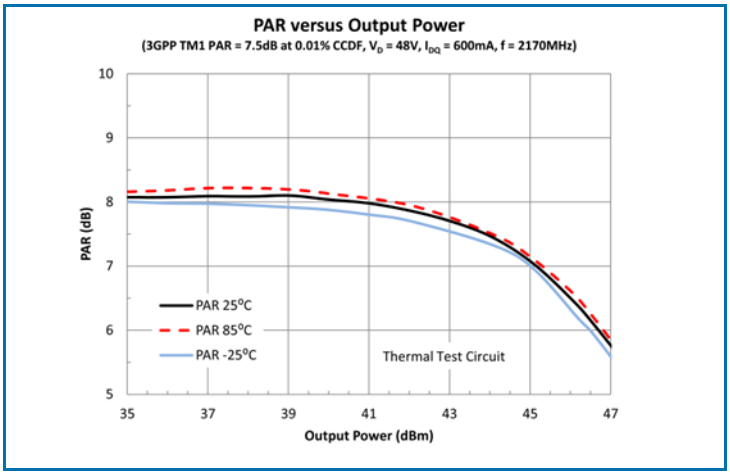
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
RF Functional Test					**[1],[2]**
$V_{GS\ (Q)}$		-3.5		V	V_D = 48V, I_D = 600mA
Gain	14.0	15.0		dB	3GPP (TM1, 7.5dB PAR at 0.01% CCDF), P_{OUT} = 45.5dBm, f = 2170MHz
Drain Efficiency	28	31.2		%	
Input Return Loss		-17.3	-8	dB	
Output PAR (CCDF at 0.01%)	5.9	6.62		dB	
Adjacent Channel Power		-37.9	-34	dBc	
Gain	13.5	14.37		dB	IS95 (9-channel model, 9.8dB PAR at 0.01% CCDF), P_{OUT} = 46.5dBm, f = 2170MHz
Drain Efficiency	32	35.84		%	
Output PAR (CCDF at 0.01%)	5.5	6.41		dB	

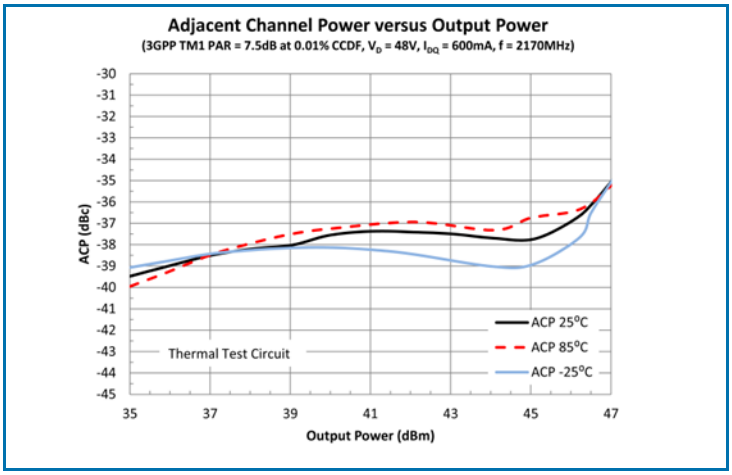
[1] Test Conditions: V_{DSQ} = 48V, I_{DQ} = 600mA, T = 25°C
[2] Performance in a standard tuned test fixture

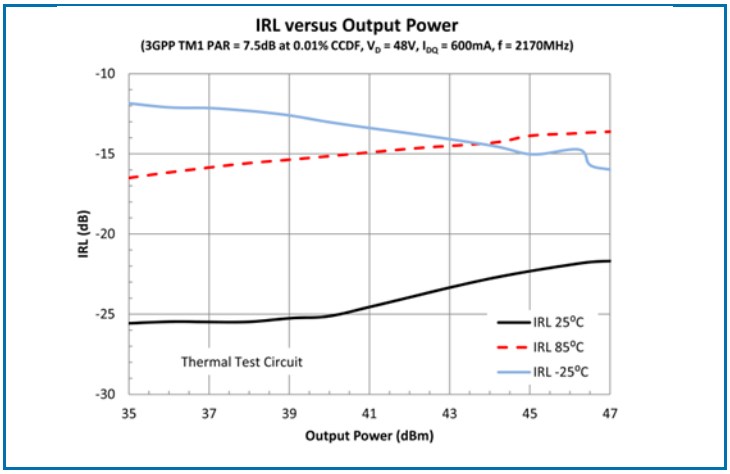
Typical Performance in standard fixed tuned test fixture
(T = 25°C, unless noted)

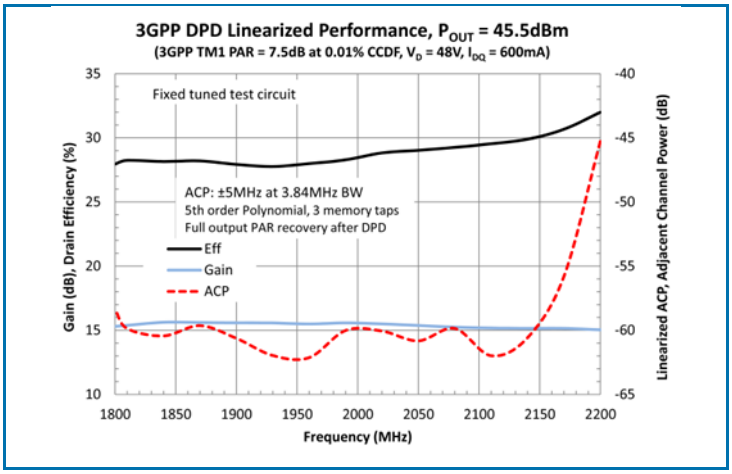




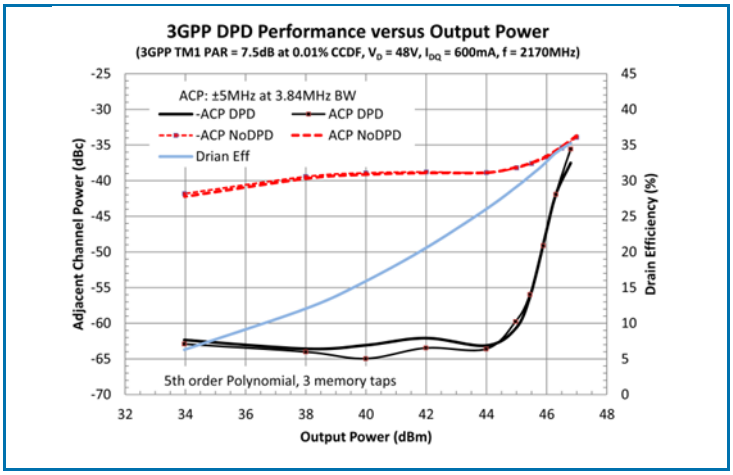


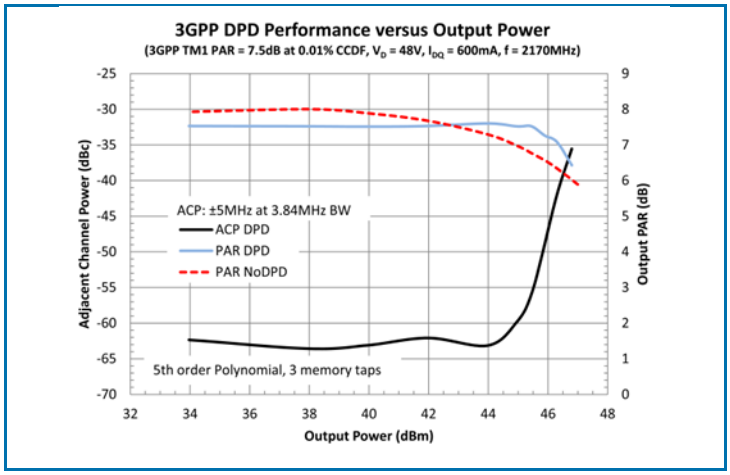


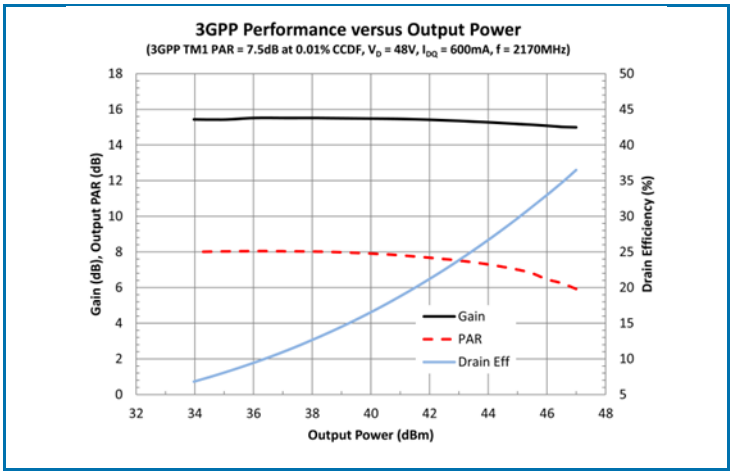


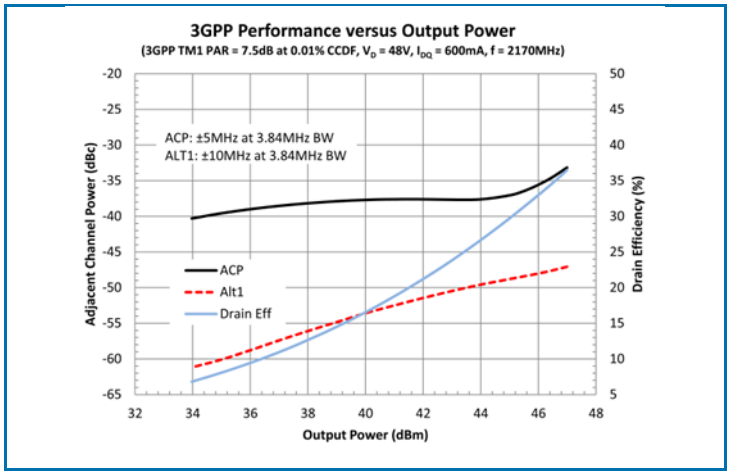


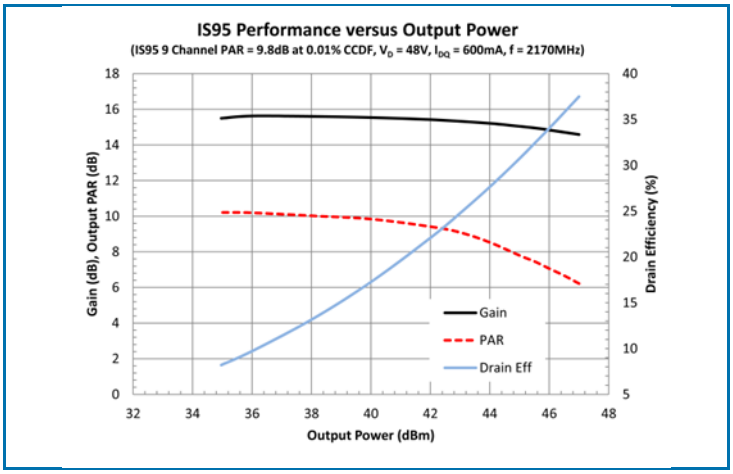
Typical Performance (Cont'd)

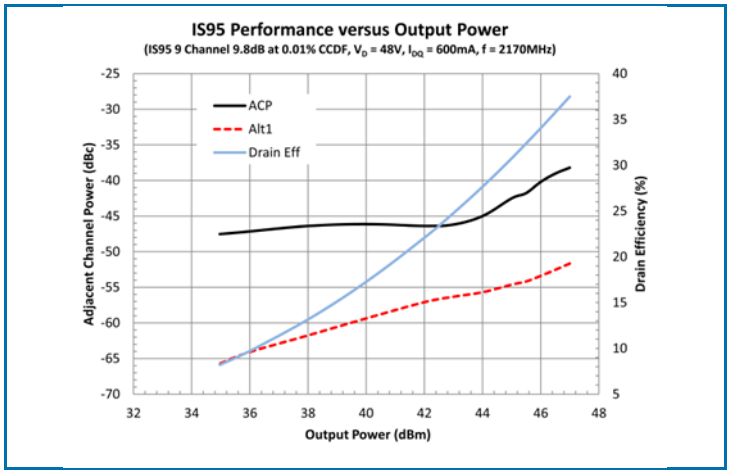




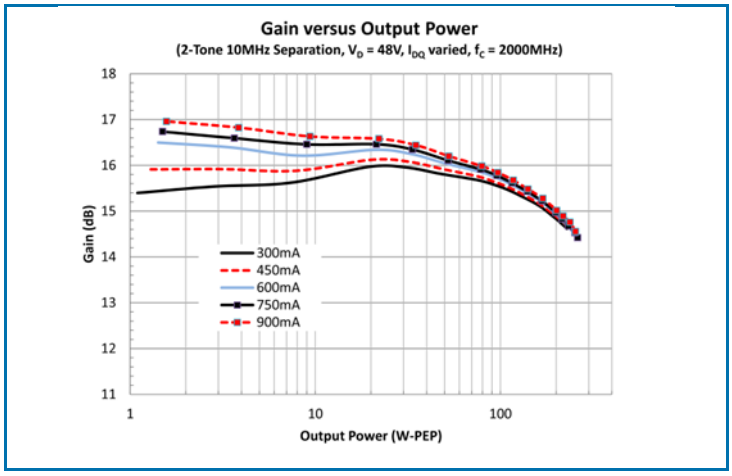


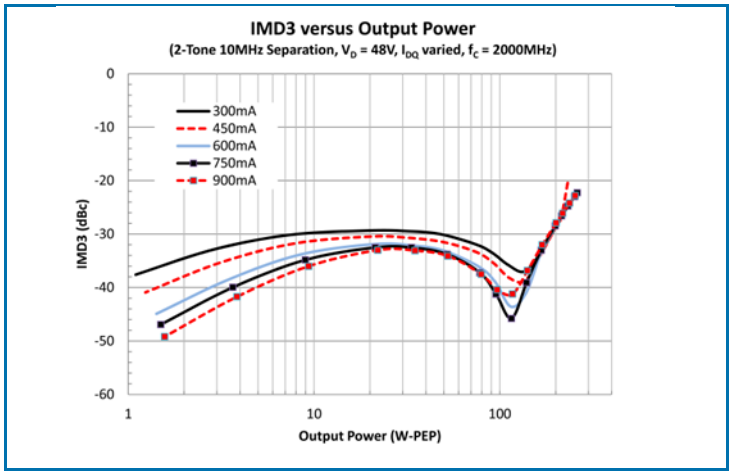


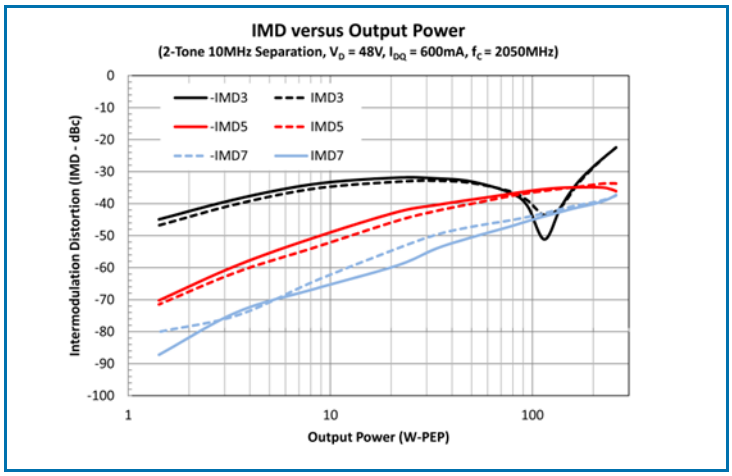


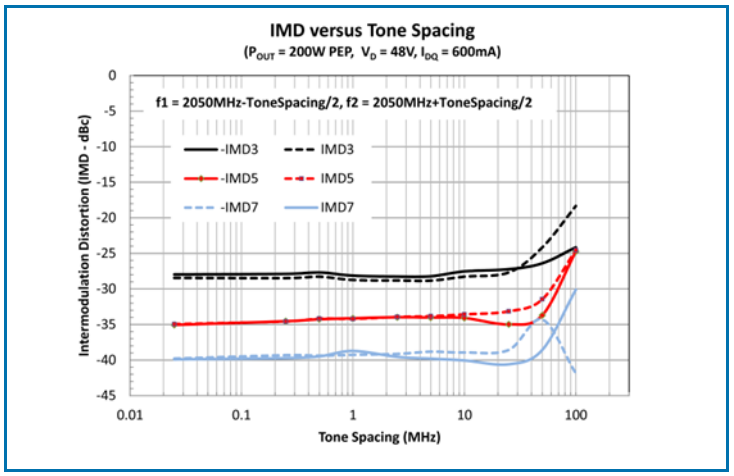


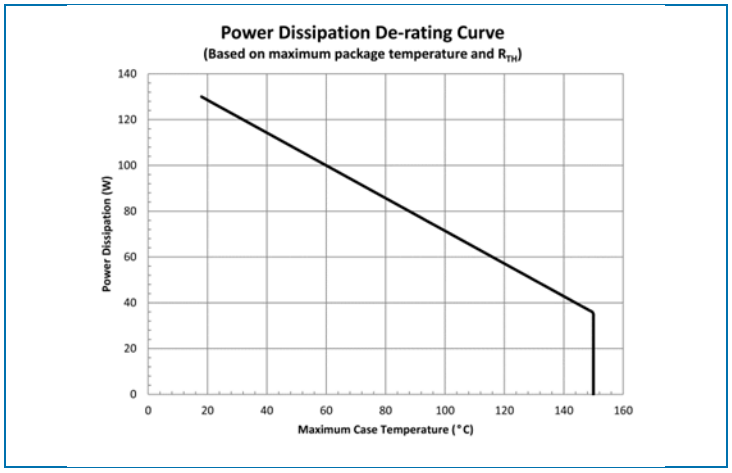
Typical Performance (Cont'd)



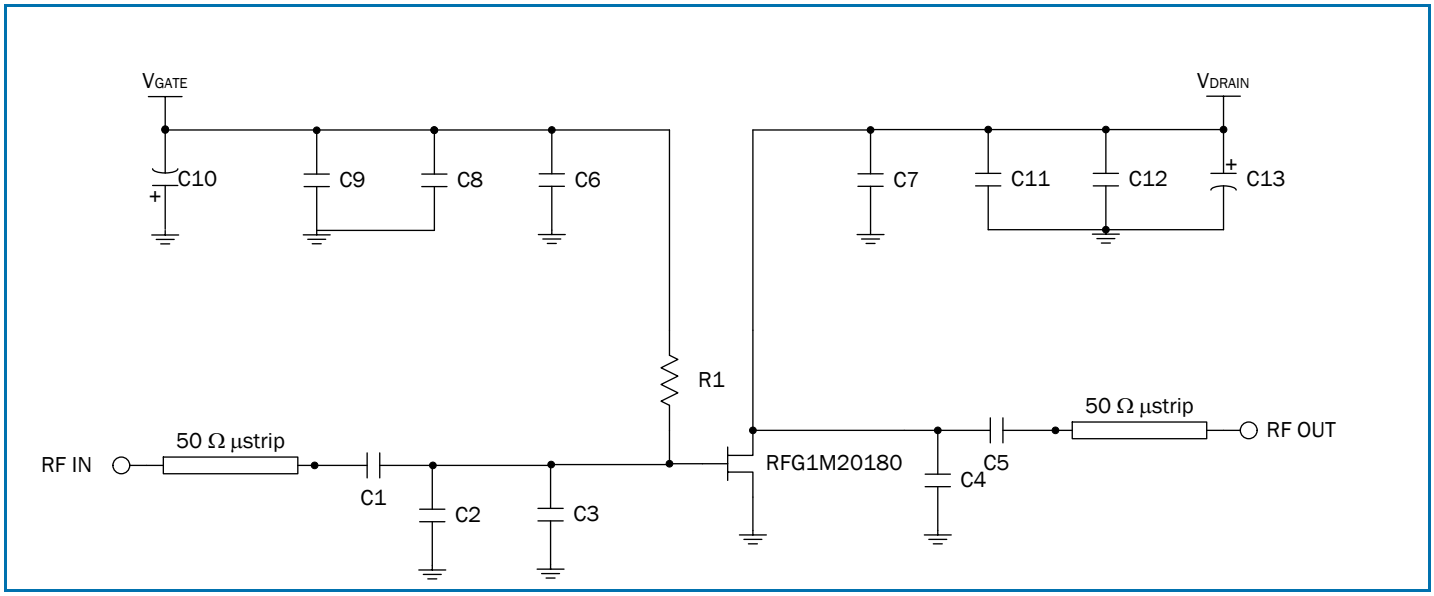








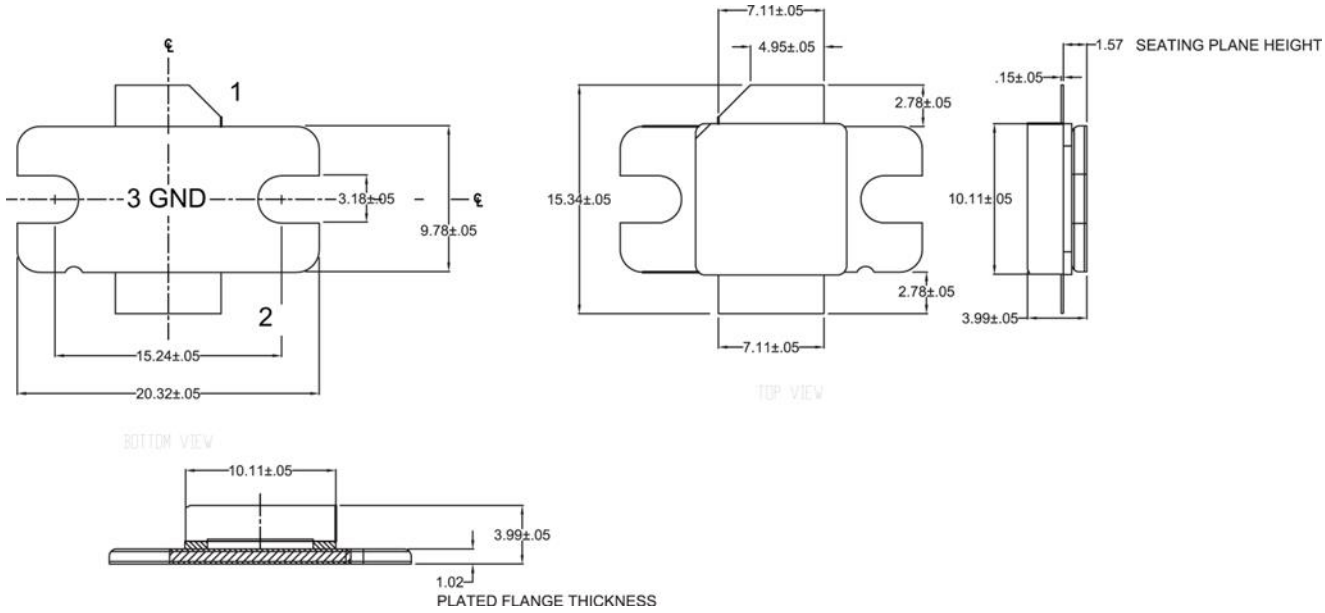
1.93GHz to 2.17GHz Evaluation Board Schematic



1.93GHz to 2.17GHz Evaluation Board Bill of Materials (BOM)

Item	Value	Manufacturer	Manufacturer's P/N
C1, C5, C6, C7	8.2pF	ATC	ATC100B8R2CT
C2, C3	1.5pF	ATC	ATC100B1R5JT
C4	2.2pF	ATC	ATC100B2R2JT
C8, C11	0.1µF	Murata	GRM32NR72A104KA01L
C9, C12	4.7µF	Murata	GRM55ER72A475KA01L
C10	100µF	Panasonic	ECE-V1HA101UP
C13	330µF	Panasonic	EEU-FC2A331
R1	10Ω	Panasonic	ERJ-8GEYJ100V
PCB	RF35, 0.020" thick dielectric	Taconic	-

Package Drawing (Package Style: Flanged Ceramic, all dimensions in mm)



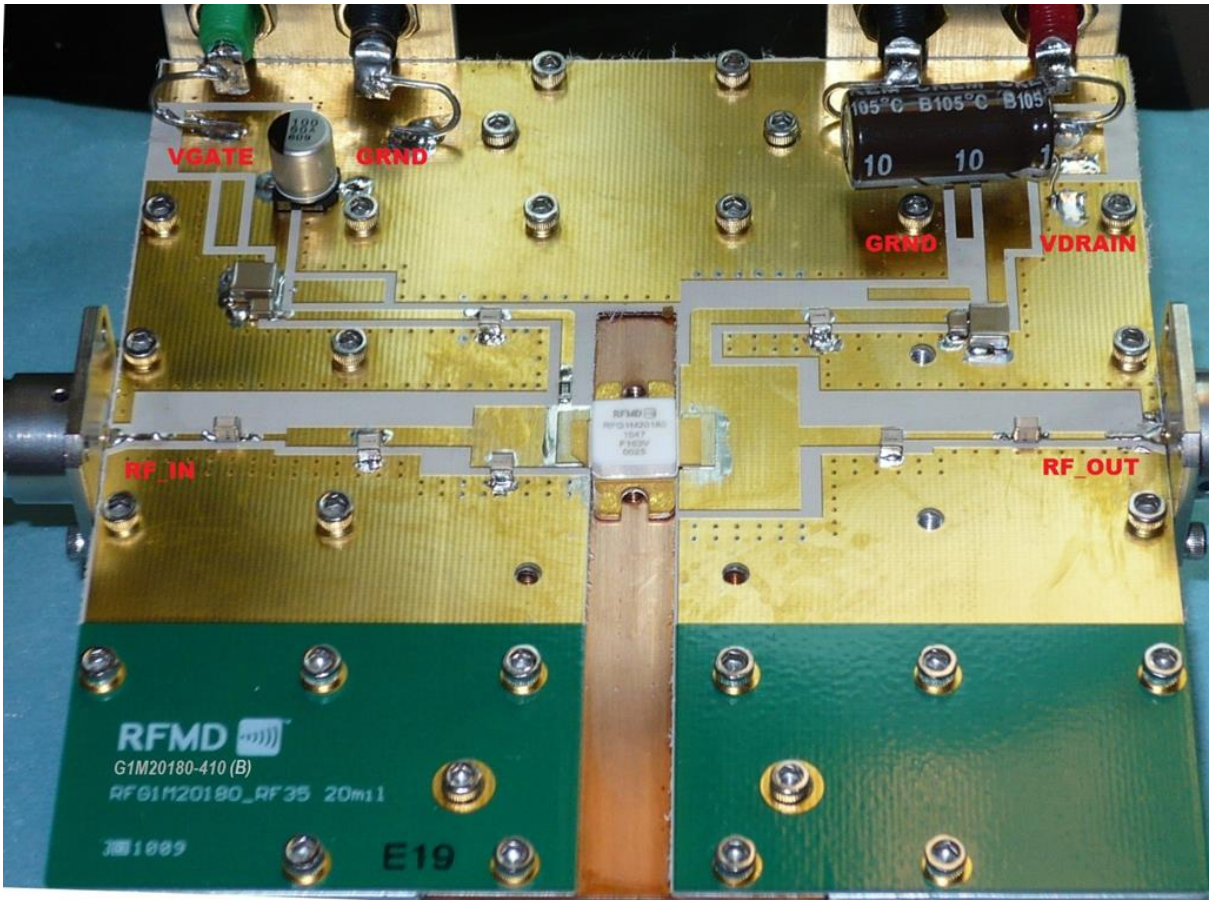
Pin Names and Descriptions

Pin	Name	Description
1	RF IN VGQ	Gate - V_{GQ} RF Input
2	RF OUT VDQ	Drain - V_{DQ} RF Output
3	GND BASE	Source - Ground Base

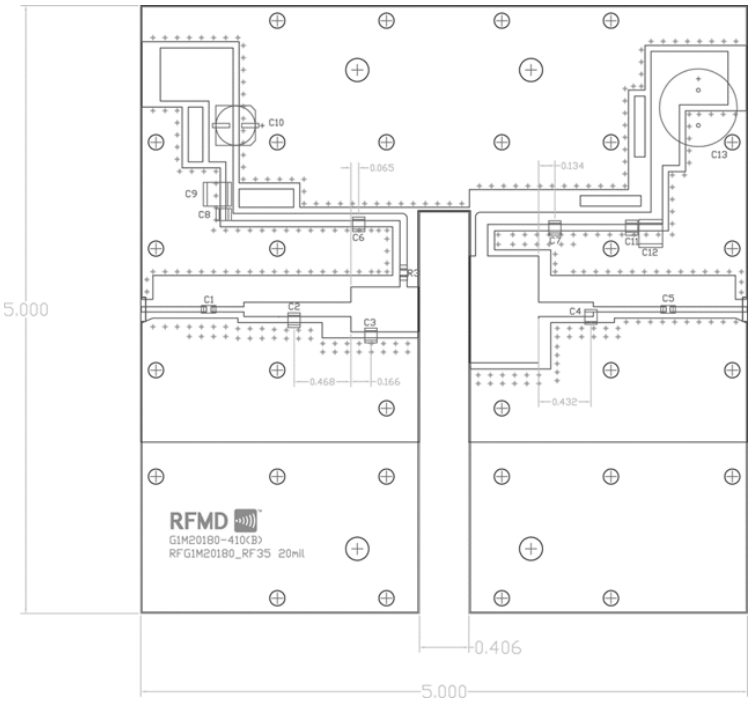
Bias Instruction for RFG1M20180 1.93GHz to 2.17GHz Evaluation Board

- ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board.
- Evaluation board requires additional external fan cooling.
- Connect all supplies before powering up the evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -5V to VG.
4. Apply 48V to VD.
5. Increase V_G until drain current reaches desired 600mA bias point.
6. Turn on RF input.



1.93GHz to 2.17GHz Evaluation Board Layout

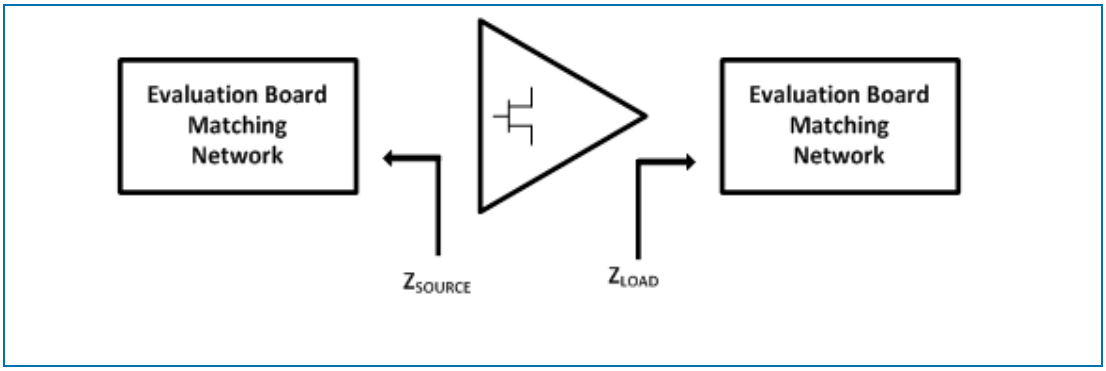


Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
1800*	9.6 – j3.3	3.5 – j0.2
1930	7.6 – j4.0	3.6 – j0.4
1990	6.6 – j4.0	3.5 – j0.5
2110	4.9 – j3.5	2.9 – j0.6
2170	4.3 – j3.3	2.5 – j0.5

Note: Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of efficiency, peak power, and linearity performance across the entire frequency bandwidth.

*1800MHz impedances are based on loadpull measurements; all other impedances are the measured evaluation board impedances.



Device Handling/Environmental Conditions

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance trade-offs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heat-sink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heat-sinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.