33510005

LVPECL VCXO @ 155.52 MHz

FEATURES

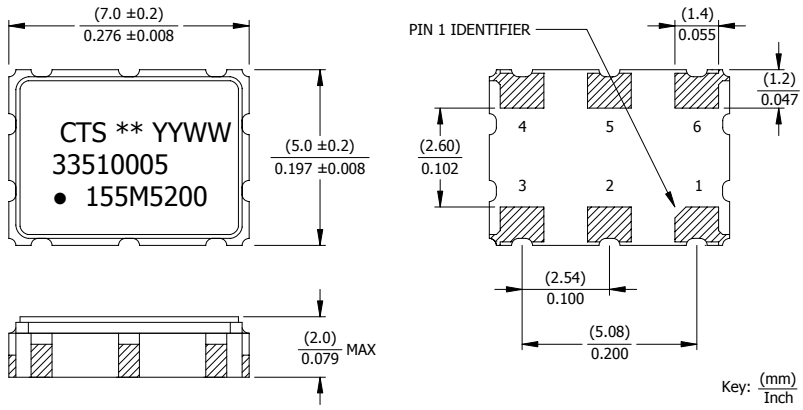
- 7.0mmx5.0mm Ceramic SM Package
- **High Frequency Fundamental Crystal Design**
- Differential LVPECL Outputs
- Frequency 155.52 MHz
- Low Phase Jitter
- Operating Temperature -40°C to +85°C
- Supply Voltage 3.3V
- Tape & Reel Packaging
- **RoHS/Green Compliant (6/6)**

ORDERING INFORMATION

CTS Part Number: 33510005

MECHANICAL AND PACKAGING SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. CTS part number.
4. XXXMXXXX - Frequency marked with 4 significant digits after the 'M'.

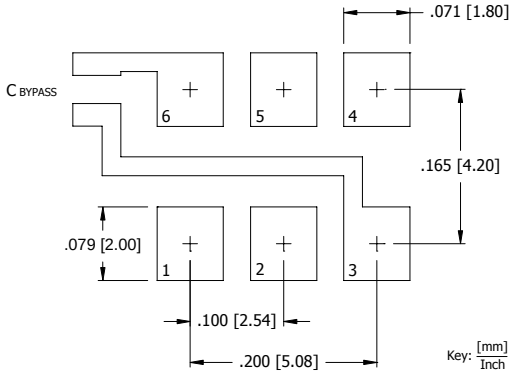
NOTES

1. Termination pads (e4), barrier-plating is nickel (Ni) with gold (Au) flash plate.
2. Reflow conditions per JEDEC J-STD-020, 260°C maximum.
3. MSL = 1.

PIN ASSIGNMENTS

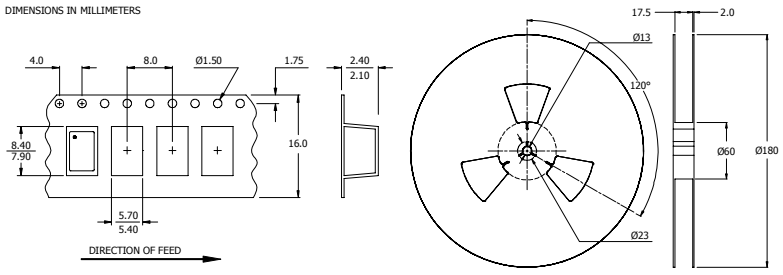
PIN	SYMBOL	DESCRIPTION
1	V_C	Control Voltage
2	OE	Output Enable/Disable
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V_{CC}	Supply Voltage

SUGGESTED SOLDER PAD GEOMETRY



C_{BYPASS} should be ≥ 0.01 uF.

TAPE AND REEL INFORMATION



Device quantity is 1,000 pieces per 180mm reel.

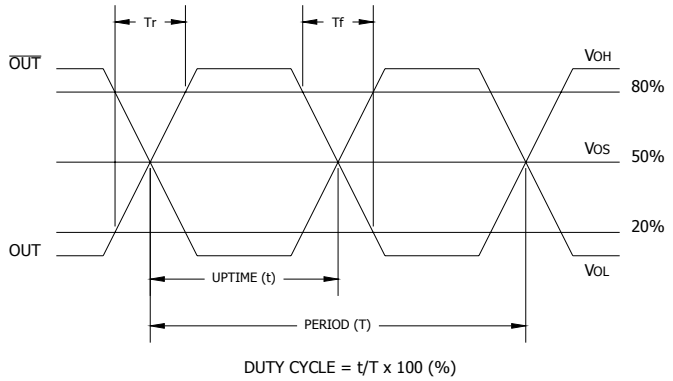
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Electrical and Waveform Parameters	Maximum Supply Voltage	V_{CC}	-	-0.5	-	7.0	V
	Storage Temperature	T_{STG}	-	-55	-	125	°C
	Frequency	f_O	-		155.5200		MHz
	Operating Temperature	T_A	-	-40	25	85	°C
	Frequency Stability						
	vs. Initial Accuracy @ 25°C	$\Delta f/f_O$	At time of shipment, V_C = 1.65V	-	25	-	± ppm
	vs. Temperature		-40°C to 85°C, referenced to 25°C	-	20	-	
	vs. Supply Voltage		±5% change	-	3	-	
	vs. Load		±10% change	-	2	-	
	vs. Aging, 1st year rate		@ 40°C average	-	2	-	
	vs. Aging, 15 year rate		@ 40°C average	-	10	15	
	Supply Voltage	V_{CC}	± 5 %	3.14	3.3	3.47	V
	Supply Current	I_{CC}	Maximum Load	-	40	60	mA
	Control Voltage	V_C	V_{CC} = 3.3V	0.0	1.65	3.3	V
	Input Impedance	Z_{Vc}	-	-	1.5	-	MOhms
	Output Load	R_L	To V_{CC} - 2V, or equivalent	-	50	-	Ohms
	Frequency Deviation [Referenced to f_O at time of shipment]	$\Delta f/f_O$	V_C = 0.0V, V_{CC} = 3.3V	-200	-	-100	ppm
			V_C = 3.0V, V_{CC} = 3.3V	100	-	200	
	Frequency Deviation Slope		V_C = 0.6V to 2.7V, in 0.3V steps	50	-	120	ppm/V
	Absolute Pull Range	APR	V_C = 0.0 to 3.3V	±50	-	-	ppm
	Linearity	L	Best Straight Line Fit	-10	-	10	%
	Modulation Bandwidth	BW	-3dB point	10	-	-	kHz
	Transfer Function	-	-	-	Positive	-	-
	Start Up Time	T_S	Application of V_{CC}	-	-	15	ms
	Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	400	550	ps
	Output Voltage Levels						
	Logic '1' Level	V_{OH}	PECL Load	V_{CC} - 1.025V	-	-	V
	Logic '0' Level	V_{OL}	PECL Load	-	-	V_{CC} - 1.62V	
	Enable Function Low Note 1						
	Enable Input Voltage	V_{IL}	Pin 2 Logic '0', Outputs Enabled	GND	-	0.3*V_{CC}	V
	Disable Input Voltage	V_{IH}	Pin 2 Logic '1', Outputs Disabled	0.7*V_{CC}	-	V_{CC}	
	Open	V_{IO}	Pin 2 Floating, Outputs Enabled	OPEN	-	OPEN	
	Phase Jitter	tjrms	Bandwidth 12 kHz - 20 MHz	-	0.3	0.5	ps RMS
	Phase Noise	-	Single Side Band				dBc/Hz
			@10 Hz	-	-55	-	
			@100 Hz	-	-85	-	
			@1 kHz	-	-115	-	
			@10 kHz	-	-130	-	
			@100 kHz	-	-140	-	
			@1M	-	-150	-	
			@10M	-	-155	-	

Notes:

1. Outputs will be enabled when OE pin is Logic '0' or open. Outputs will be disabled when OE pin is Logic'1'.

PECL OUTPUT WAVEFORM



DUTY CYCLE = t/T x 100 (%)

TEST CIRCUIT, PECL LOAD