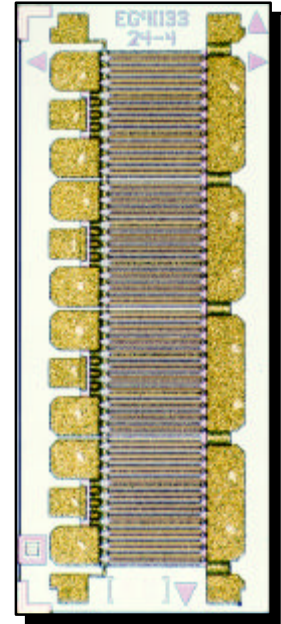
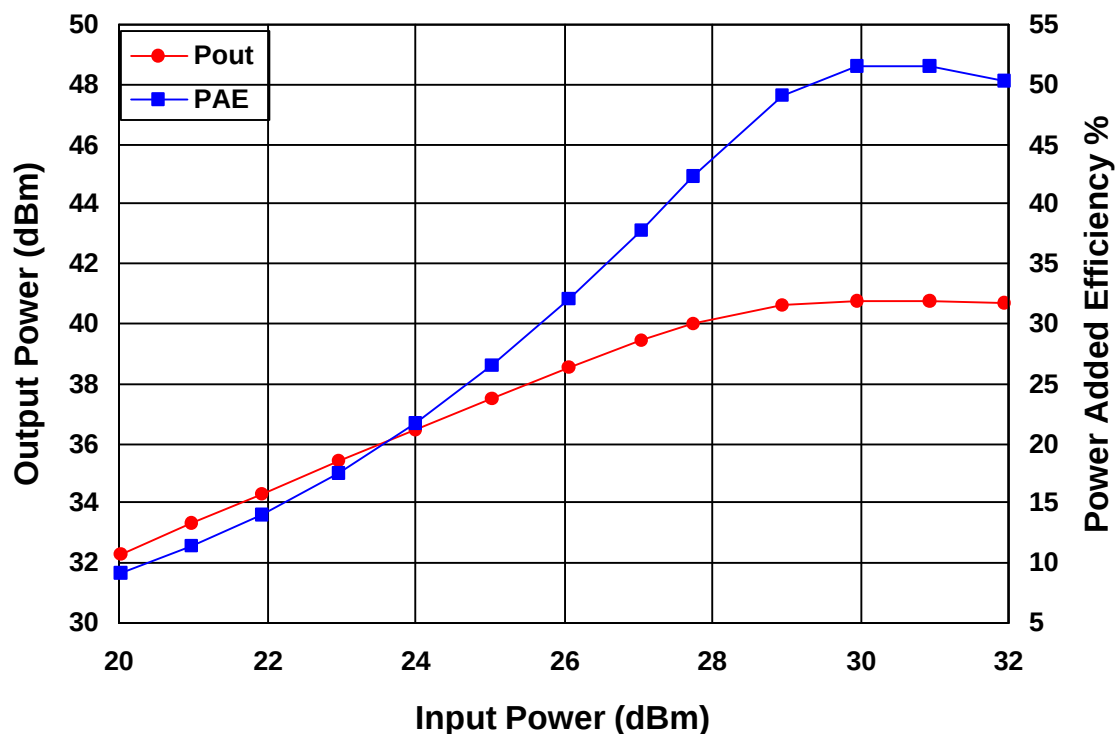


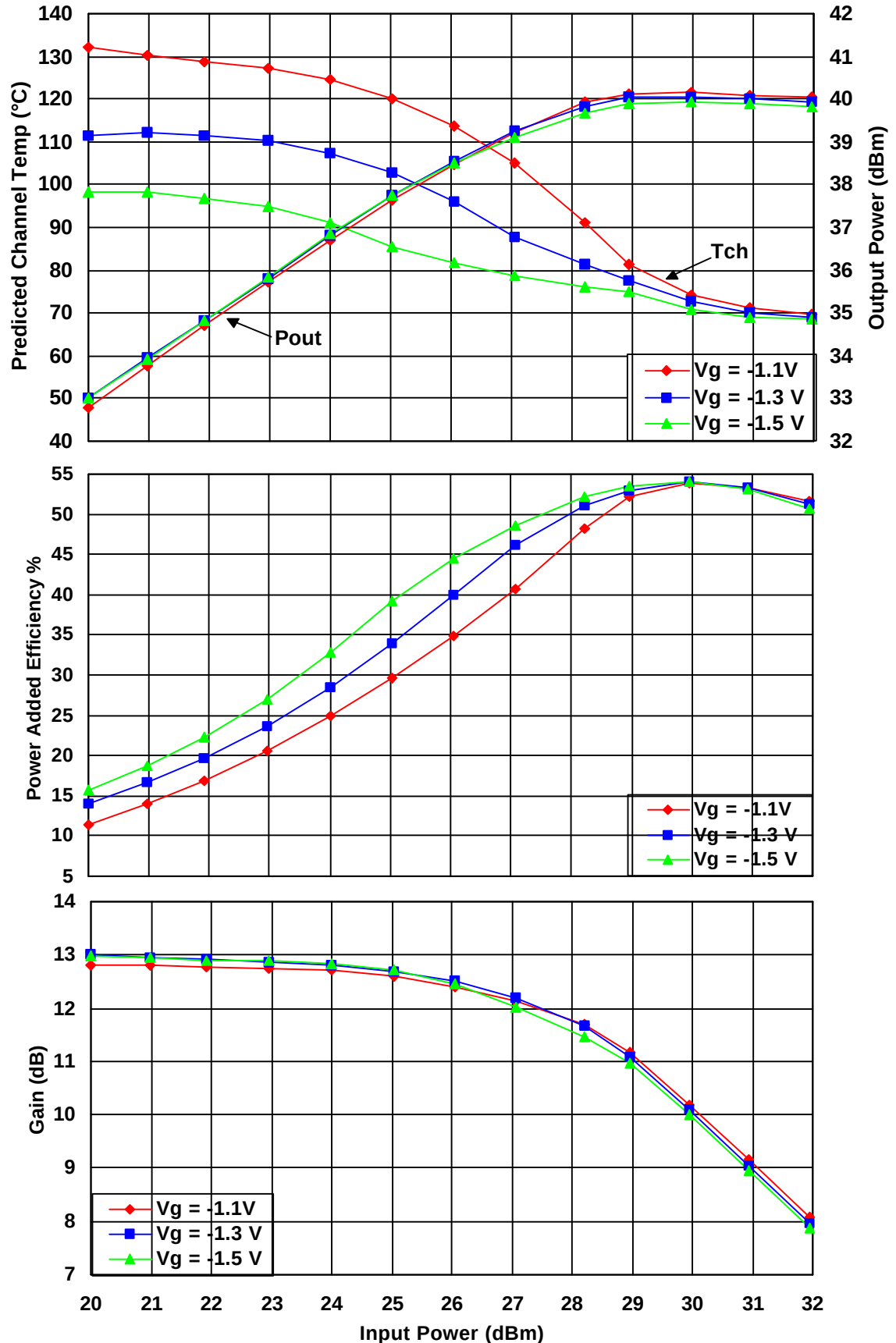
- 0.5 μm gate finger length
- Nominal Pout of 12 Watts at 2.3 GHz
- Nominal PAE of 51.5% at 2.3 GHz
- Nominal Gain of 10.8 dB at 2.3 GHz
- Die size 36.0 x 81.0 x 4.0 mils
(0.914 x 2.057 x 0.102 mm)



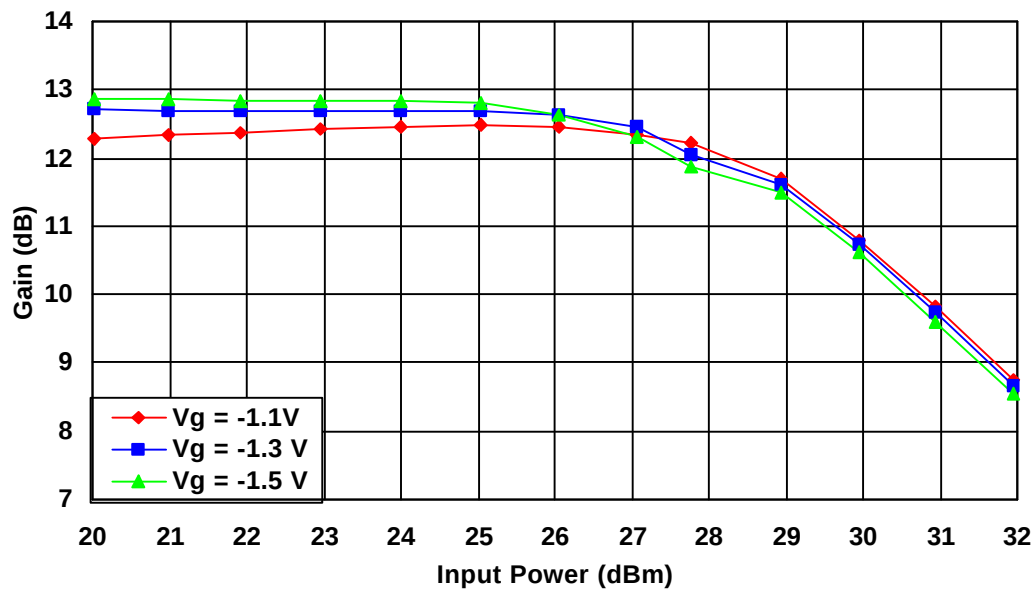
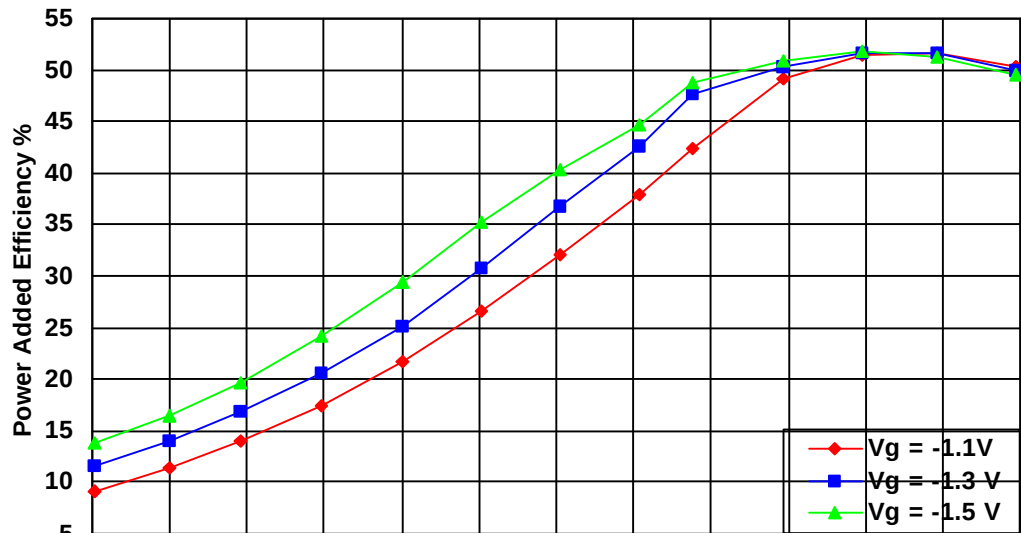
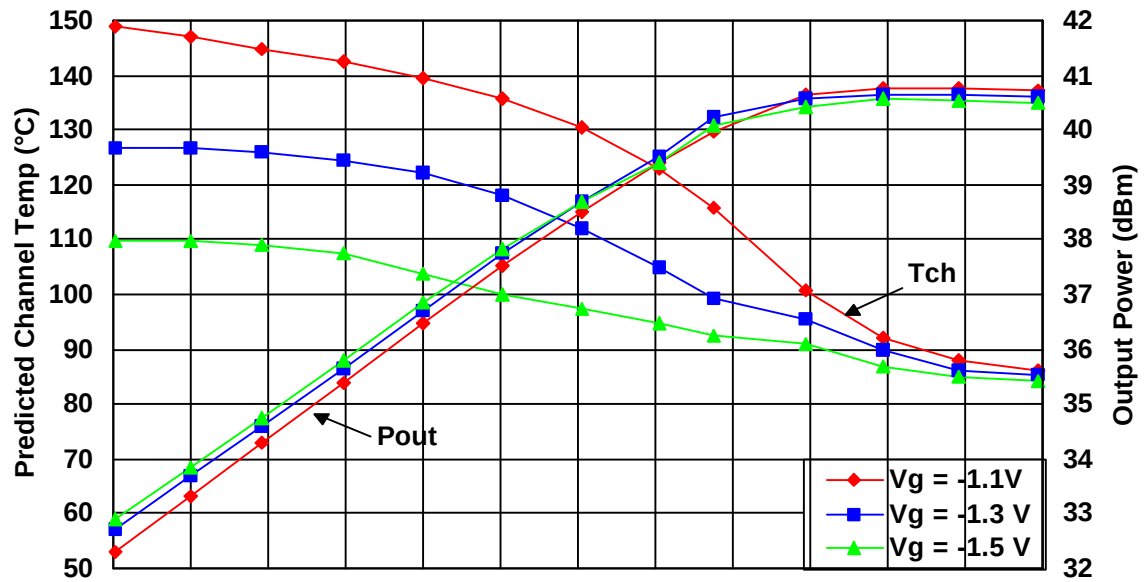
TGF4124 RF Performance at F = 2.3 GHz
V_d = 8.0 V, V_g = -1.1 V, I_q = 2.17 A and T_A = 25°C



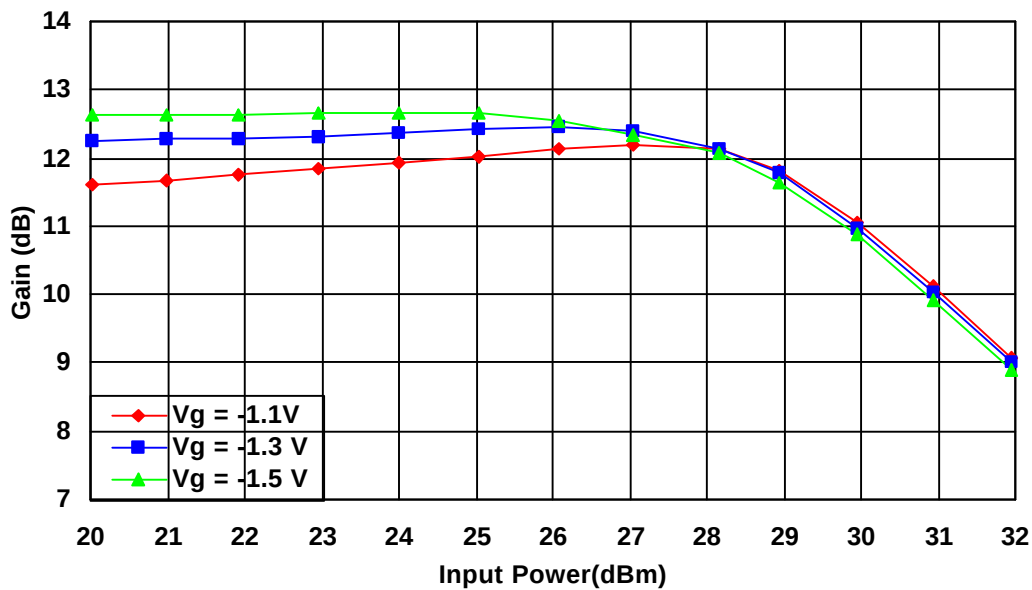
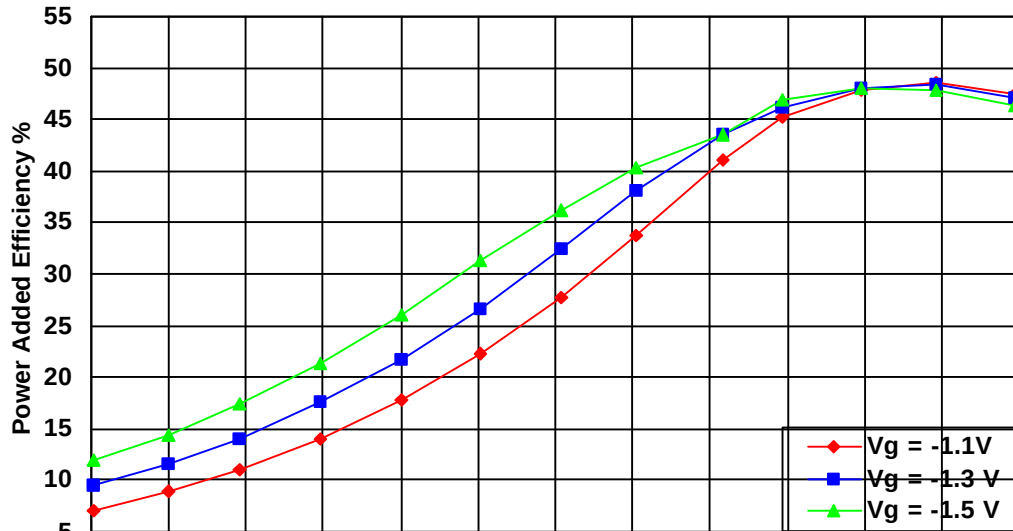
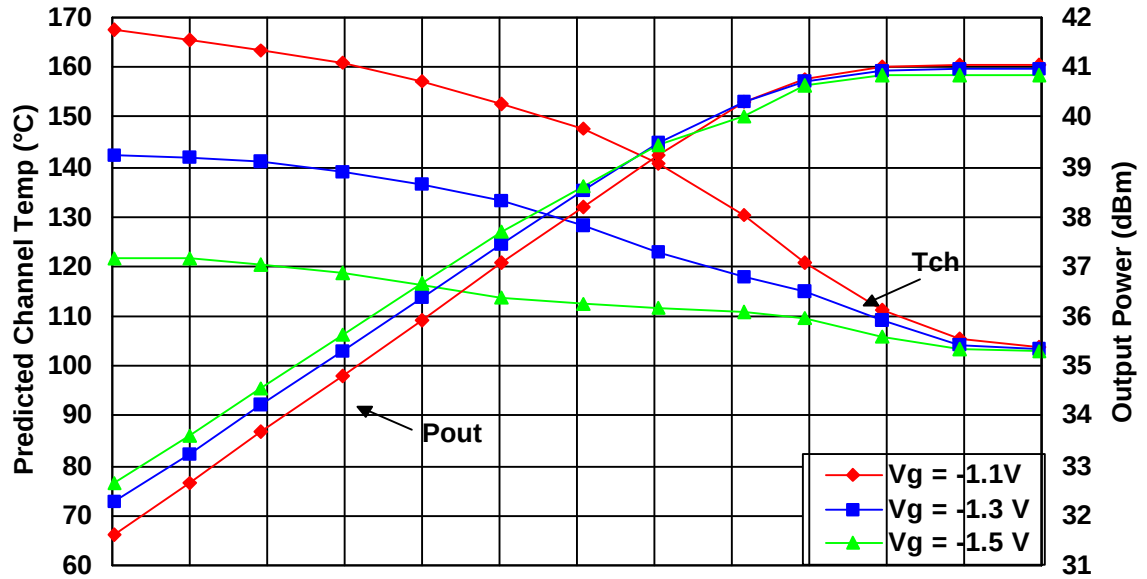
TGF4124 RF Performance for $V_d = 7.0$ V, $F = 2.3$ GHz, and $T_A = 25^\circ\text{C}$
Quiescent I_d is 2.24 A ($V_g = -1.1$ V), 1.81 A ($V_g = -1.3$ V), and 1.37 A ($V_g = -1.5$ V)



TGF4124 RF Performance for $V_d = 8.0\text{ V}$, $F = 2.3\text{ GHz}$, and $T_A = 25^\circ\text{C}$
Quiescent I_d is 2.17 A ($V_g = -1.1\text{ V}$), 1.80 A ($V_g = -1.3\text{ V}$), and 1.40 A ($V_g = -1.5\text{ V}$)



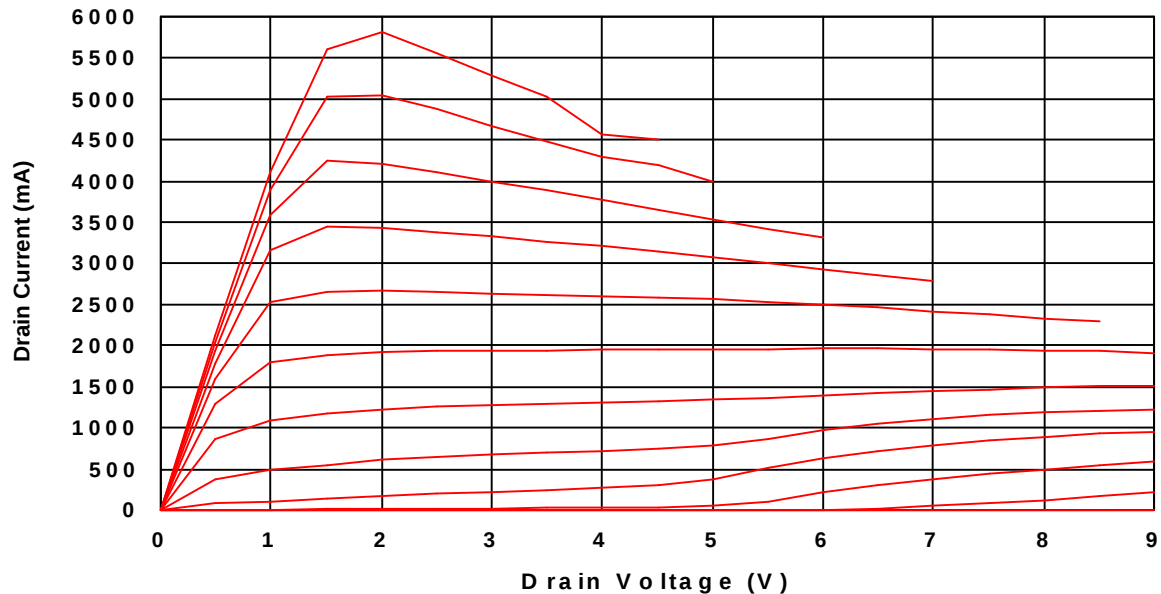
TGF4124 RF Performance for $V_d = 9.0\text{ V}$, $F = 2.3\text{ GHz}$, and $T_A = 25^\circ\text{C}$
Quiescent I_d is 2.11 A ($V_g = -1.79\text{ V}$), 1.79 A ($V_g = -1.3\text{ V}$), and 1.43 A ($V_g = -1.5\text{ V}$)



DC Characteristics for the TGF4124

DC probe Parameters		Nominal	Unit
IDSS	Drain Saturation Current	5880	mA
GM	Transconductance	3960	mS
VP	Pinch Off Voltage	-1.85	V
BVGS	Breakdown Voltage Gate-Source	-22	V
BVGD	Breakdown Voltage Gate-Drain	-22	V

Example of DC I-V Curves
 $V_g = 0.0 \text{ V to } -2.75 \text{ V in } 0.25 \text{ steps}$ $T_A = 25^\circ\text{C}$



Absolute Maximum Ratings

Drain-to-source Voltage, V_{ds}12 V
 Gate-to-source Voltage, V_{gs}-5 V to 0 V
 Mounting Temperature.....320°C
 Storage Temperature..... -65°C to 200°C
 Power Dissipation.....refer to Thermal Model
 Operating Channel Temperature.....refer to Thermal Model

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in this document is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

TGF4124 Linear Model

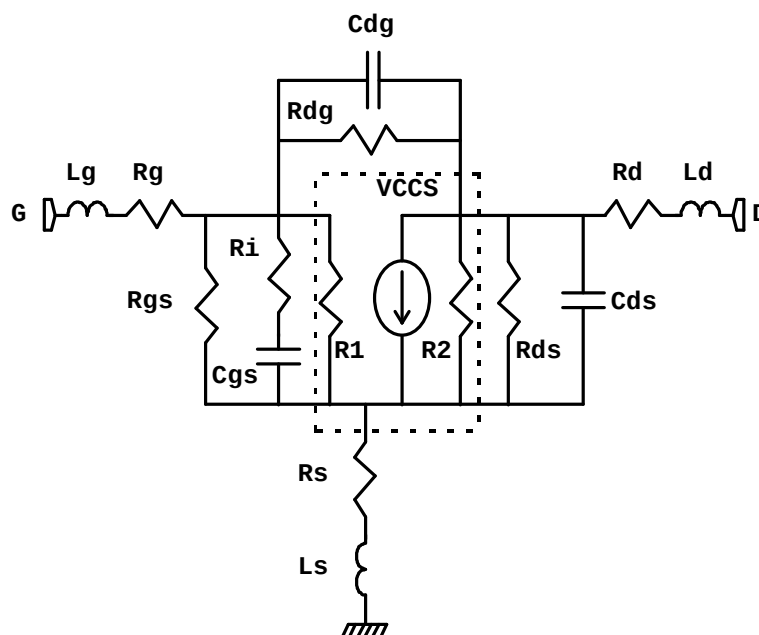
Vds = 8 V and Ids = 1.84 A at T = 25°C

FET Elements

Lg = .00103 nH
 Rg = 0.53233 Ω
 Rgs = 4086 Ω
 Ri = 0.030 Ω
 Cgs = 26.9096 pF
 Cdg = 0.99024 pF
 Rdg = 102026 Ω
 Rs = 0.04943 Ω
 Ls = 0.00808 nH
 Rds = 5.39715 Ω
 Cds = 4.30372 pF
 Rd = 0.19448 Ω
 Ld = 0.00965 nH

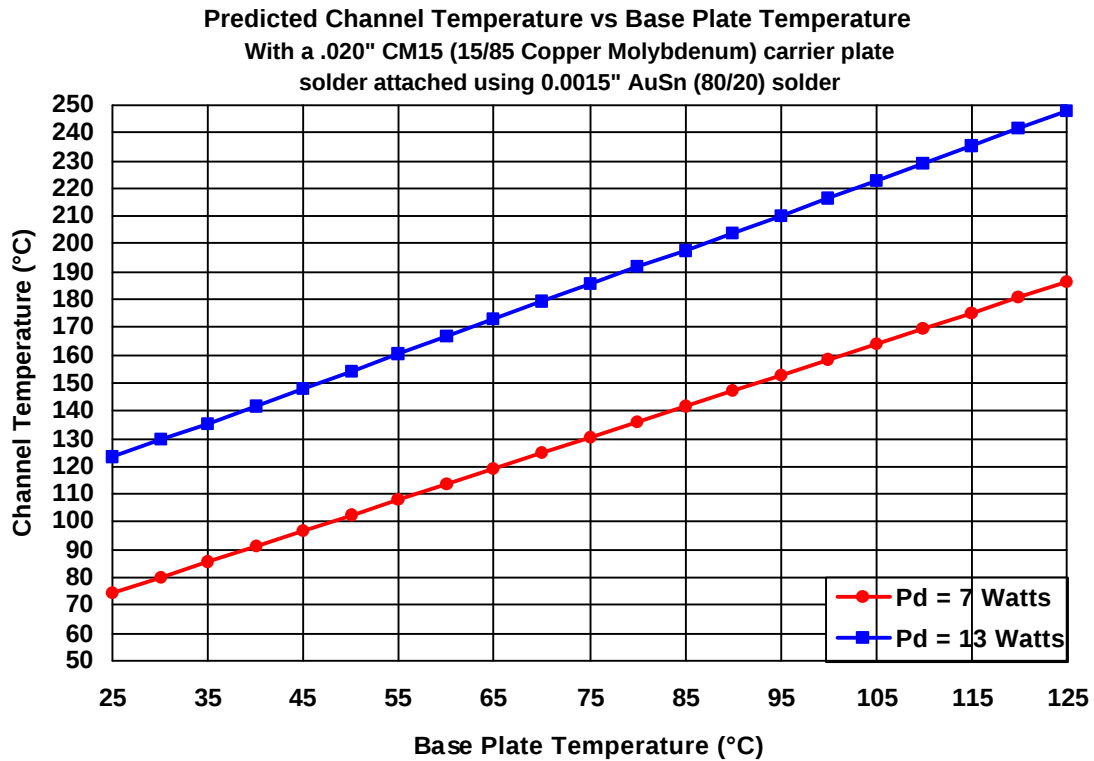
VCCS Parameters

M = 2.668 S
 A = 0
 R1 = 1E19
 R2 = 1E19
 F = 0
 T = 4.50 pS

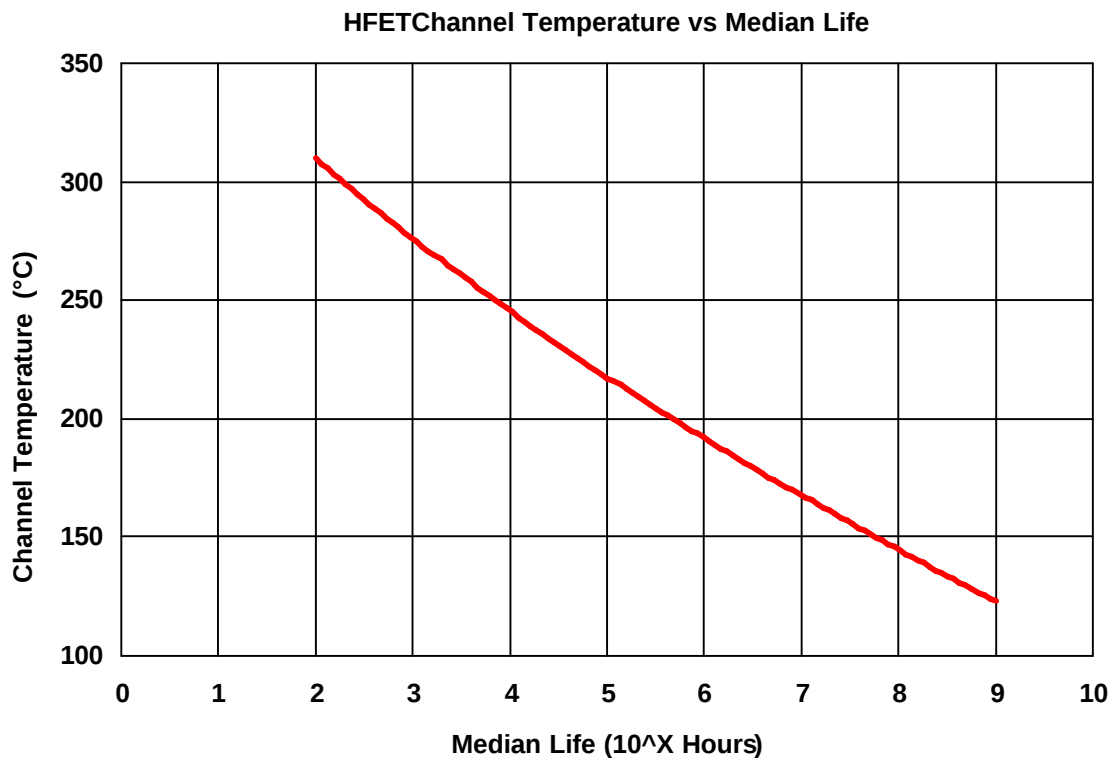


Freq-GHz	MAG-S11	ANG-S11	MAG-S21	ANG-S21	MAG-S12	ANG-S12	MAG-S22	ANG-S22
0.5	0.9655	-162.057	3.91809	95.2201	0.00638	15.0344	0.85618	-178.832
1	0.96563	-171.022	1.9714	86.9895	0.00651	16.8356	0.8587	-178.929
1.5	0.96577	-174.063	1.3101	81.7652	0.00665	21.478	0.86075	-178.77
2	0.96596	-175.605	0.97656	77.3514	0.00684	26.7416	0.86327	-178.562
2.5	0.96619	-176.548	0.77485	73.316	0.00709	32.1233	0.8663	-178.354
3	0.96646	-177.19	0.6393	69.5245	0.0074	37.4067	0.8698	-178.163
3.5	0.96676	-177.663	0.54171	65.9265	0.00778	42.4614	0.87367	-177.998
4	0.96708	-178.031	0.46793	62.5019	0.00822	47.2001	0.87783	-177.864
4.5	0.96742	-178.329	0.41013	59.243	0.00874	51.567	0.88221	-177.762
5	0.96777	-178.579	0.36358	56.1476	0.00931	55.5339	0.88672	-177.694

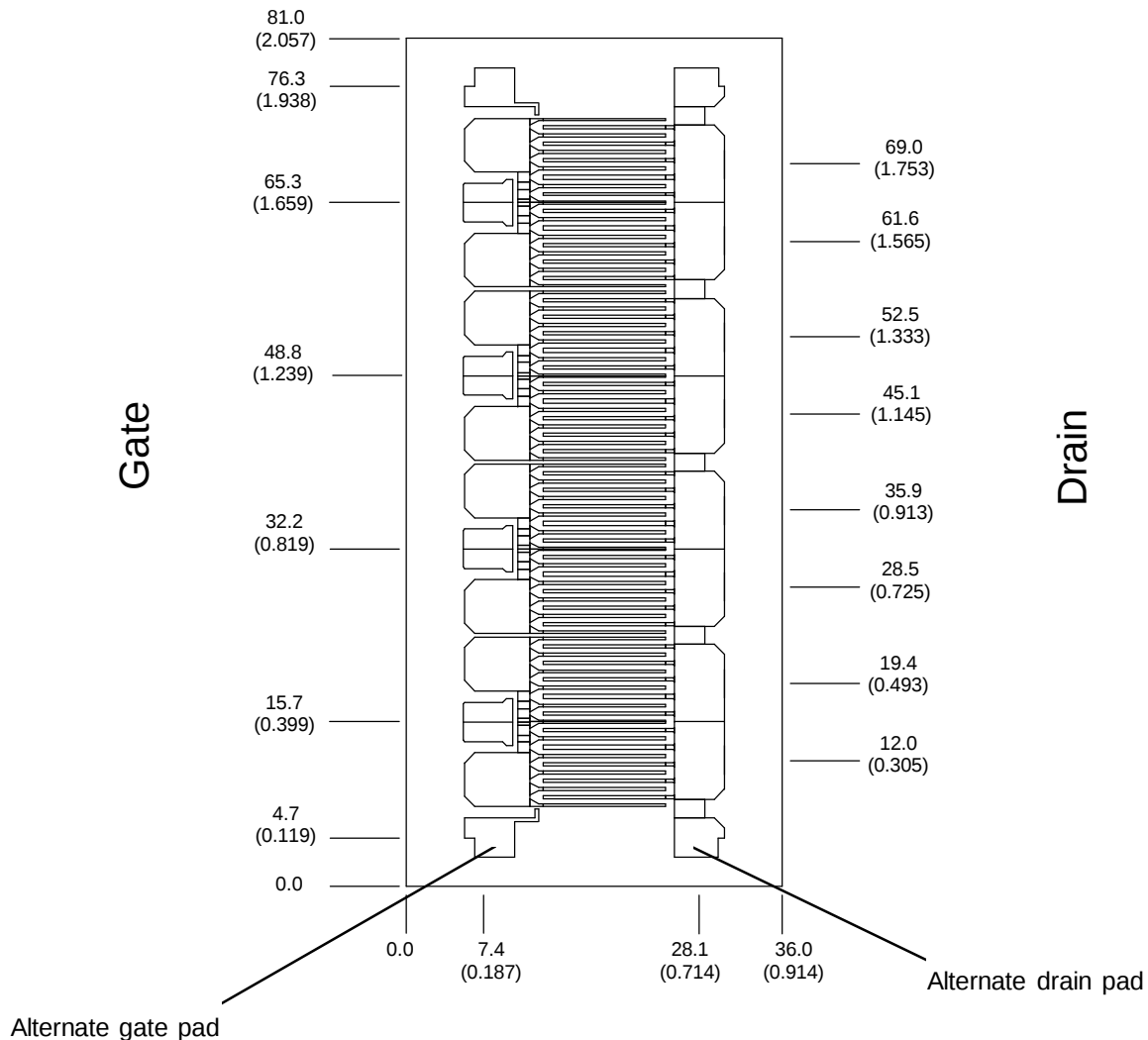
Thermal Model of TGF4124



$T_{ch} = 0.6458 + 5.886 \times Pd + 0.0882 \times Pd^2 + (1.001 + 0.01633 \times Pd + 0.0001833 \times Pd^2) \times T_{base}$
 (Predicted Channel Temperature equation for the given assembly stack up)
 This model assumes a perfect solder connection (no voids) between the FET and the carrier plate.



Mechanical Drawing of TGF4124



Units: mils (mm)

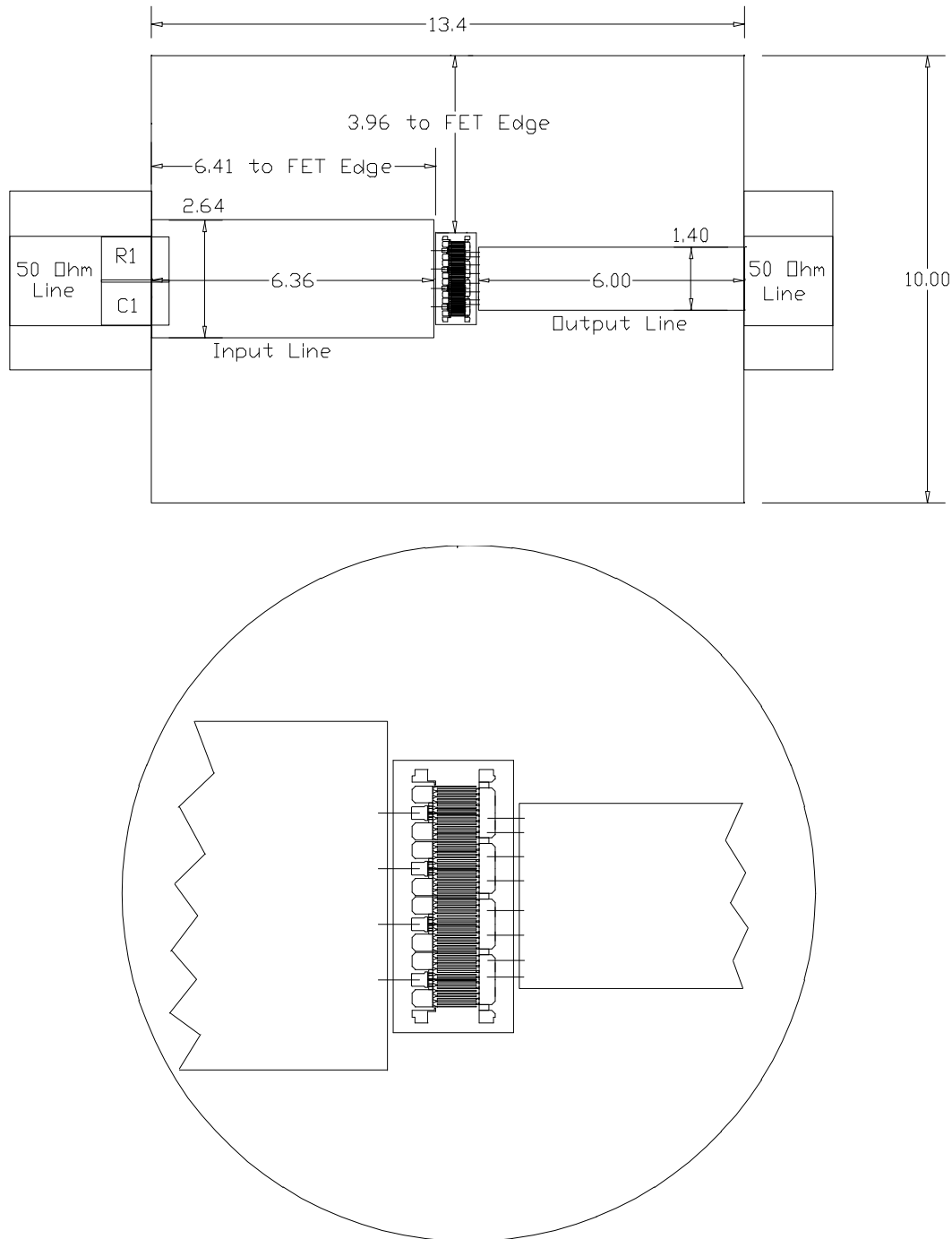
Thickness: 4.0 (0.10)

Gate pad sizes are 4.0 x 4.0 (0.10 x 0.10)

Drain pad sizes are 4.7 x 14.5 (0.12 x 0.37)

A minimum of four gate bonds and eight drain bonds is recommended for operation. Sources are connected to backside metalization. Alternate gate and drain pads are located on either end of the FET for paralleling TGF4124s.

Application circuit for the TGF4124 at 2.3 GHz



The FET is soldered using AuSn solder at 300°C for 30 secs. Input and output matching networks are 0.381 mm ZrSn Tioxide substrates ($\epsilon_r = 38$). The design load impedance is between 3Ω and 4Ω with the 8 pF output capacitance of the FET included in the output network. For further explanation refer to the application note "Designing High Efficiency Amplifiers using HFETs". The carrier plate is 0.51 mm gold plated copper molybdenum. Gold wire 0.018 mm diameter is used for the bonds. Four gate bonds are required with a length of 0.42 mm. Eight drain bonds are required with a length of 0.42 mm. Bondwire end points on the FET are in the middle of the bond pads. Refer to the figures above for bondwire locations. Connection between the 50 ohm line input to the input match is made by a parallel RC network. R1 in this network is 10 ohms, and C1 is 5.6 pF. R1 and C1 are surface mount 0603 piece parts.