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For user manuals and dimensional drawings, visit the product page resources tab on ni.com.

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NI PXIe-5451

400 MS/s, 16-Bit, Dual-Channel Arbitrary Waveform Generator

- Time domain, I/Q, and IF signal generation
- 16-bit resolution, 400 MS/s sampling rate per channel
- 145 MHz analog bandwidth, ±0.34 dB flatness to 120 MHz with digital flatness correction
- 98 dB close-in SFDR at 1 MHz
- -146 dBc/Hz phase noise density at 10 kHz offset
- -160 dBm/Hz average noise density
- 25 ps channel-to-channel skew
- Continuous data streaming >600 MB/s from host

Overview

The NI PXIe-5451 is a 16-bit, 400 MS/s, dual-channel arbitrary waveform generator. It features both single-ended and differential outputs with two analog paths for maximum flexibility and performance. Each of the outputs features up to 98 dB of spurious-free dynamic range (SFDR) at 1 MHz (without harmonics), better than -146 dBc/Hz phase noise density at 10 MHz (10 kHz offset), and less than 25 ps channel-to-channel skew. The NI PXIe-5451 is the ideal instrument to test devices with I/Q inputs, generate multiple wideband signals, or serve as the baseband component of an RF vector signal generator. It also features onboard signal processing (OSP) functions that include digital upconversion, pulse shaping and interpolation filters, gain and offset control, and a numerically controlled oscillator (NCO) for frequency shifting. Common applications include prototyping, validating, and testing of semiconductor components and communications, radar, and electronic warfare systems. With its NI Synchronization and Memory Core (SMC) architecture, the NI PXIe-5451 helps you integrate mixed-signal test systems by enabling synchronization with other instruments such as vector signal analyzers/generators, high-speed digitizers, digital waveform analyzers/generators, and other signal generators. You can also synchronize multiple arbitrary waveform generators to form a phase-coherent multichannel generator for applications such as MIMO (multiple-input, multiple-output) or beamforming antenna schemes.

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Application and Technology

Signal Quality and Flexibility

With 16 bits of resolution, the NI PXIe-5451 achieves a close-in SFDR (without harmonics) of 98 dB at 1 MHz on the performance-optimized direct path. Including harmonics and measured from DC to 200 MHz, it achieves a 10 MHz SFDR of 75 dB and a wideband SFDR of 72 dB at 60 MHz. IMD at 10 MHz is -84 dBc, and the noise floor is also extremely low at -160 dBm/Hz. These specifications provide the dynamic range and out-of-band performance needed to meet the stringent demands of baseband I/Q signal generation (Figure 1).

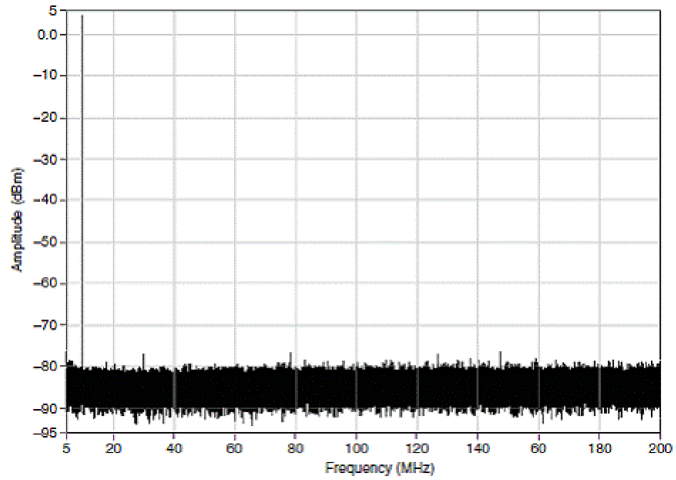

***Figure 1**. With its high sample rate and resolution, the NI PXIe-5451 generates low-distortion, high-SFDR signals over a very high bandwidth (the noise floor is limited by the measurement device).*

The main path, while optimized for flexibility, achieves similar levels of performance. It features a variable analog gain stage with 63 dB of range and four digits of adjust, capable of generating signals using the full 16-bit resolution of the main digital-to-analog converter (DAC) from 5 Vpk-pk (differential, into 100 Ω) down to 1.77 mVpk-pk (single-ended, into 50 Ω). A novel architecture provides DC offset independent of gain, allowing small AC signals on top of high-bias voltages, which are useful for stimulating single-supply components. Other benefits of the main path include a software-enabled reconstruction filter and software-selectable single-ended and differential outputs.

The NI PXIe-5451 also delivers exceptional passband flatness (Figure 2). While the -3 dB analog bandwidth of the direct path is 145 MHz, the digital flatness correction filter provides ±0.34 dB of flatness from DC to 120 MHz. On the main path, the flatness correction filter provides ±0.50 dB of flatness from DC to 120 MHz.

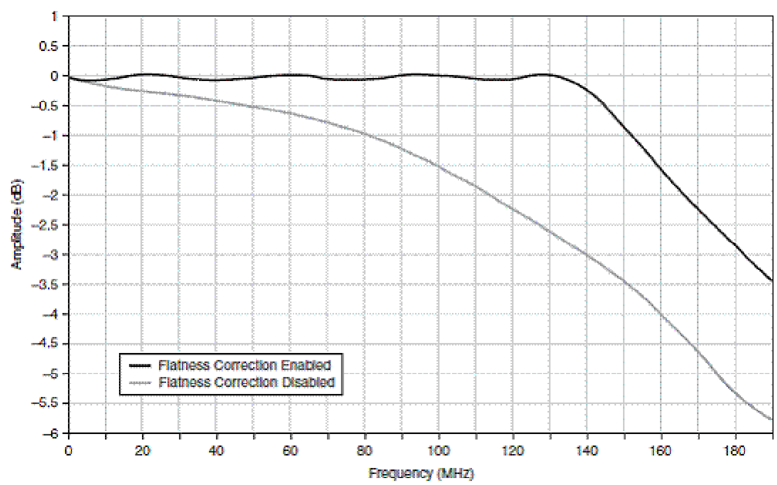

***Figure 2**. Passband flatness (direct path) is significantly improved with the use of digital flatness correction in the NI PXIe-5451 FPGA.*

For maximum signal purity, the phase noise of this module is extremely low. The phase noise density of a tone generated at 10 MHz drops from -121 dBc/Hz at a 100 Hz offset to -152 dBc/Hz at 100 kHz, yielding an integrated system output jitter of less than 350 fs. Its highly stable phase-locked loop (PLL) and high-resolution oscillator provide an output sample rate resolution less than 5.7 μHz, enabling low phase noise signal generation at any frequency with microhertz resolution.

An essential attribute for I/Q generation is tight synchronization between channels. The NI PXIe-5451 features high-performance circuitry that calibrates the channel skew to within 25 ps. You can achieve even more alignment with a 10 ps resolution programmable skew, which is useful in calibrating out cable length mismatches. This tight level of synchronization minimizes the phase error between channels, especially at high frequencies, which is essential for accurately generating high-bandwidth I/Q signals (Figure 3).

Figure 3. *Dedicated channel-alignment circuitry automatically calibrates the two channels on the NI PXIe-5451 to within 25 ps. This particular module exhibits less than 13 ps of skew, demonstrated on a 100 MHz sinusoid.*

High-Speed Data Streaming

In addition to tight synchronization, the SMC architecture on the NI PXIe-5451 takes advantage of the PCI Express bus to continuously stream data from the host controller at more than 600 MB/s in dual-channel mode or at 360 MB/s when generating on a single channel. This enables the module to continuously output I/Q waveforms at 150 MS/s, or, when upconverted, approximately 120 MHz RF bandwidth, either from host memory or a high-speed storage solution such as the NI HDD-8264 3 TB RAID array. With this technology, you can generate terabyte waveforms of unique, high-bandwidth data for several hours. Applications that benefit from this capability include RF and baseband recording and playback for signals intelligence and communications system design, validation, and verification.

Onboard Signal Processing

OSP significantly extends waveform playback time and shortens waveform download times (Figure 4). A field-programmable gate array (FPGA) on the NI PXIe-5451 implements the OSP functionality, which enables several signal processing and I/Q-related functions.

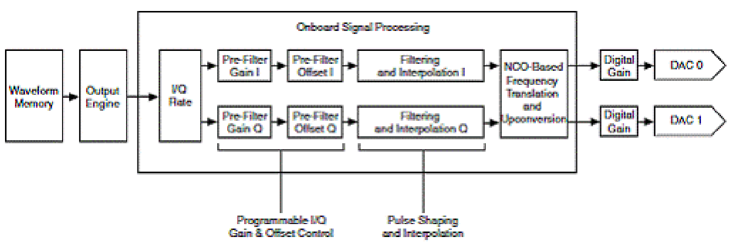

Figure 4. *OSP on the NI PXIe-5451 FPGA performs inline processing of waveform data before it is sent to the digital-to-analog converter (DAC).*

Digital upconversion (DUC) – Converts complex waveform data to a real signal centered at an intermediate frequency and generated out of a single analog channel. The DUC supports I/Q rates up to 200 MS/s and bandwidths limited by the analog bandwidth of the NI PXIe-5451, or 0.8 times the I/Q rate, whichever is lower.

Complex frequency shifting – Shifts complex waveform data higher or lower in frequency and generates separate analog I and Q signals.

Independent I and Q prefilter gain and offset – Adds gain and offset imbalance impairments and I and Q prefilter gain. You can adjust the offset before or during the generation of an output signal (figures 5, 6).

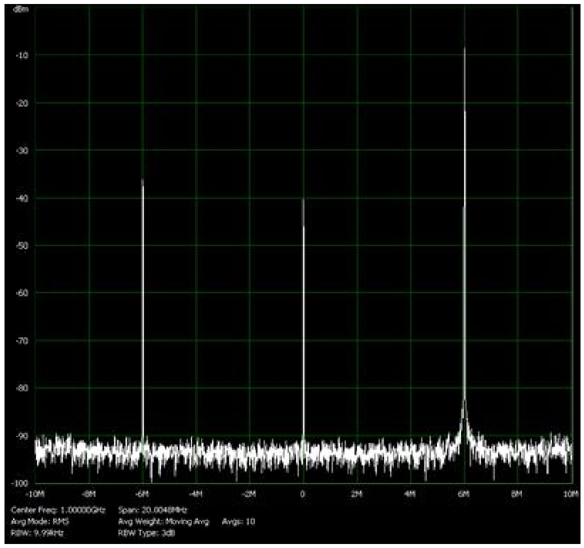

Figure 5. *LO leakage and poor image rejection of a quadrature modulator cause undesired RF emissions.*

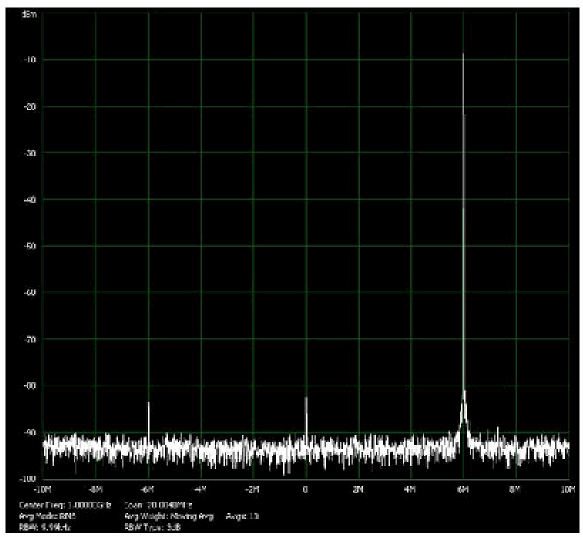

Figure 6. *On-the-fly-adjustable parameters on the NI PXIe-5451 correct for the quadrature modulator impairments seen in Figure 5.*

Pulse-shaping finite impulse response (FIR) filter – Shapes and interpolates the waveform data. FIR filter types include flat, raised cosine, and root raised cosine, with a programmable a parameter. Digital interpolation factors range from 2 to 32,768 times.

Numerically controlled oscillator (NCO) – Produces sinusoidal waveform data for complex (I/Q) frequency shifts before or during generation with up to a ±86 MHz shift and 710 nHz resolution. NCO tuning time is 250 µs.

Baseband interpolation – Generates smooth baseband signals with integer interpolation. You can use the NI PXIe-5451 OSP block to interpolate low-sample-rate waveforms to a much higher sample rate, thereby improving the output frequency spectrum by relocating zero-order sample-and-hold reconstruction images to higher frequencies. With the images at higher frequencies, the device's image-suppression filter greatly suppresses them without disturbing the signal's amplitude response or phase information.

Waveform Sequencing and Triggering

You also can program the NI PXIe-5451 to sequence and loop a set of waveforms. You can choose from several methods to step through the sequence of waveforms. In cases when you know the duration of each waveform in advance, you can program the generator to loop them a specified number of times. When you do not know the duration before the start of generation, you can use a hardware or software trigger to advance the generator to the next waveform in the sequence. The NI PXIe-5451 implements advanced triggering behavior with four trigger modes: single, continuous, burst, and stepped. In addition, scripting provides the ability to link and loop multiple waveforms together, managing triggers and markers. For a detailed discussion of these modes, consult the NI Signal Generators Help guide available at ni.com/manuals.

NI SMC-based generators have the unique capability of storing multiple sequences and their associated waveforms in the generator's onboard memory (see Figure 7). In automated test applications involving multiple tests, each requiring a different waveform sequence, you can download all of the sequences and waveforms once at the beginning of the test cycle and store them in the generator's memory for the entire session. By downloading all required waveforms and sequences once to an SMC-based generator instead of repeatedly reloading them for each test, you save time and improve throughput.

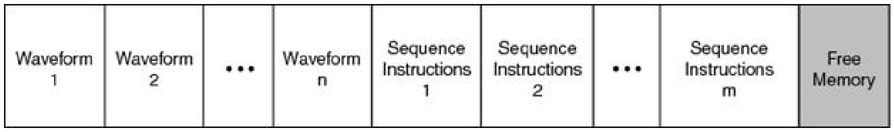

Figure 7. *NI SMC-based arbitrary waveform generators increase test throughput by storing all the waveforms and sequences required for a set of tests in onboard memory.*

Timing and Synchronization

Using NI T-Clock (TClk) synchronization technology, you can synchronize multiple NI PXIe-5451 modules for applications requiring a greater number of channels, such as I/Q signal generation for MIMO systems. Because it is built into the SMC, TClk can synchronize the NI PXIe-5451 with SMC-based vector signal analyzers and generators, high-speed digitizers, and digital waveform generators and analyzers for tight correlation of analog and digital stimulus and response. Using onboard calibration measurements and compensation, TClk can automatically synchronize any combination of SMC-based modules with less than 500 ps module-to-module skew. Greatly improved from traditional synchronization methods, the skew between modules does not increase as the number of modules increases. To achieve even better performance, you can use a high-bandwidth oscilloscope to precisely measure the module-to-module skew. With the oscilloscope measurement for calibration information, TClk can achieve <20 ps module-to-module skew.

NI PXIe-5451 clocking is flexible. Its internal, DDS-based clock is optimized for phase noise performance, and has better than 5.7 μHz frequency resolution. The module can also import its sample clock from the CLK IN front panel connector and multiply and divide this clock's frequency by integers. Finally, the NI PXIe-5451 can phase-lock its internal clock to an external reference or the PXI 10 MHz reference clock.

Driver Software

Accurate, high-throughput hardware improves the performance of a measurement system, but easy-to-use, reliable software reduces development time and ongoing support costs. NI-FGEN, the driver software for the NI PXIe-5451, is the world's most advanced and thoroughly tested arbitrary waveform generator software. It features:

Intuitive application programming interface (API) – In NI LabVIEW and LabWindows/CVI as well as Microsoft Visual Basic and Visual C/C++, the NI-FGEN API is engineered to use the least number of functions possible while maintaining flexibility. Each driver function has thorough online searchable documentation. The NI-FGEN Instrument Driver Quick Reference guide further simplifies programming by providing an overview of each driver function's LabVIEW icon, function name, parameters, and data types.

LabVIEW Express VIs – For generating an arbitrary repetitive signal, the LabVIEW Express VI is a configuration-driven method of programming the NI PXIe-5451 without accessing the underlying NI-FGEN functions.

Soft Front Panel – For quick, nonprogrammatic use of the NI PXIe-5451, the Soft Front Panel supports arbitrary waveform generation.

Example programs – NI-FGEN provides 23 programming examples for LabVIEW, LabWindows/CVI, Visual C++ 6.0 and .NET, and Visual Basic 6.0, giving developers references on which to base custom applications.

LabVIEW Real-Time support – For remotely deployed, autonomous measurement systems or applications requiring the highest possible reliability, NI-FGEN works with the LabVIEW Real-Time Module.

Modulation Toolkit for LabVIEW

The NI Modulation Toolkit for LabVIEW provides functions for signal generation, analysis, and visualization of custom and standard analog and digital modulation. With the Modulation Toolkit, you can develop and analyze custom modulation formats and generate these with the NI PXIe-5451. Some of the standard measurement functions include error vector magnitude (EVM), modulation error ratio (MER), and r (rho). Functions are also available for injecting impairments including I/Q gain imbalance, quadrature skew, and additive white Gaussian noise (AWGN). Visualization functions include trellis, constellation, and 2D and 3D eye diagrams. This hardware and software combination gives you access to customizable functionality not available in traditional instrumentation.

Modulation/Demodulation

- 4-, 8-, 16-, 32-, 64-, 128-, 256-QAM
- 2-, 4-, 8-, 16-FSK
- MSK and GMSK
- 8-, 16-, 64-PSK
- BPSK, QPSK, OQPSK, DQPSK, ^{1}/4DQPSK
- AM, FM, PM

Modulation Analysis Functions

- r (rho)
- DC offset
- Phase error
- Quadrature skew
- I/Q gain imbalance
- Bit error rate (BER)
- Frequency deviation
- Additive white Gaussian noise (AWGN)
- Burst timing measurements
- Modulation error ratio (MER)
- Error vector magnitude

Visualization and Analysis

- Trellis diagrams
- Constellation plot

- 2D and 3D eye diagrams

Modulation Impairments

- Multitone
- DC offset
- Fading profile
- Frequency offset
- Quadrature skew
- I/Q gain imbalance

Analog Waveform Editor

The NI Analog Waveform Editor is an interactive software tool for creating and editing analog waveforms. In the editor, each waveform comprises different components, and each component comprises a collection of primitives. You can create a new waveform segment by selecting from a library of more than 20 waveform primitives (Table 1), by entering a mathematical expression, or by importing data from a file. You can then combine waveform primitives point-by-point using addition, subtraction, multiplication, or division to create more complex segments (Figure 8). You can also concatenate multiple segments to make a larger waveform. To further process the waveform, you can apply standard or custom FIR and IIR filters or smooth any discontinuities between different waveform segments. Once complete, all the waveform settings are stored along with the waveform's raw sample data, making it easy to reload the waveform in the editor and modify the settings of a particular segment or primitive.

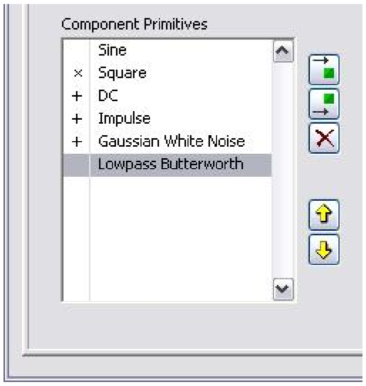

Figure 8. *You can combine more than 20 different waveform primitives to create more complex waveforms.*

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Ordering Information

For a complete list of accessories, visit the product page on ni.com.

Products	Part Number	Recommended Accessories	Part Number
NI PXIe-5451			
NI PXIe-5451, 128 MB	781204-01	No accessories required.	
NI PXIe-5451, 2 GB	781204-03	No accessories required.	
NI PXIe-5451, 512 MB	781204-02	No accessories required.	

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Calibration

NI measurement hardware is calibrated to ensure measurement accuracy and verify that the device meets its published specifications. To ensure the ongoing accuracy of your measurement hardware, NI offers basic or detailed recalibration service that provides ongoing ISO 9001 audit compliance and confidence in your measurements. To learn more about NI calibration services or to locate a qualified service center near you, contact your local sales office or visit ni.com/calibration.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications

400 MS/s 2-Channel Arbitrary Waveform Generator

This document lists specifications for the NI PXIe-5451(NI 5451) arbitrary waveform generator.

Specifications are warranted under the following conditions:

- 15 minutes warm-up time at ambient temperature
- Calibration cycle maintained
- Chassis fan speed set to High
- NI-FGEN instrument driver used
- NI-FGEN instrument driver self-calibration performed after instrument is stable

Unless otherwise noted, the following conditions were used for each specification:

- Signals terminated with 50 Ω to ground
- Main path set to 2.5 V_{pk} differential (gain = 2.5, 5 V_{pk-pk} differential)
- Direct path set to 0.5 V_{pk} differential (gain = 0.5, 1 V_{pk-pk} differential)
- Sample clock set to 400 MS/s
- Onboard Sample clock with no Reference clock
- Analog filter enabled
- 0 °C to 55 °C ambient temperature

Specifications describe the warranted, traceable product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under Specifications or Typical values. Nominal values are not covered by warranty.

Specifications are subject to change without notice. For the most recent NI 5451 specifications, visit ni.com/manuals.

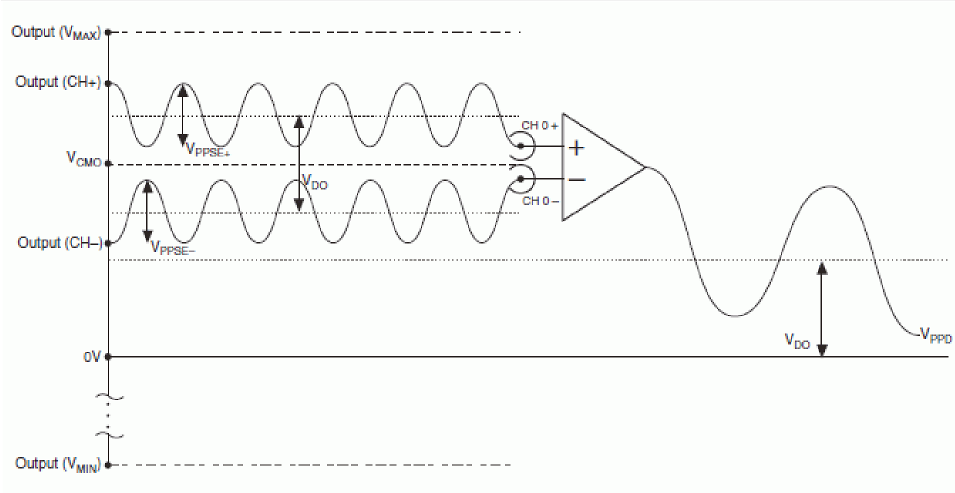
To access all the NI 5451 documentation, navigate to **Start»All Programs»National Instruments»NI-FGEN»Documentation**.

Hot Surface If the NI 5451 has been in use, the device or the shield may exceed safe handling temperatures and may cause burns. Allow the NI 5451 to cool before touching the shield or removing the device from the chassis.

Caution For EMC compliance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

The following figure illustrates the relationship between the differential offset voltage and the common-mode offset voltage, along with a generated peak-to-peak AC signal for single-ended and differential configurations. The peak-to-peak differential receiver voltage rejects the common-mode offset voltage and other common-mode noise present in the signal.

Definition of Common Mode Offset and Differential Offset



$V_{PPD} = V_{PPSE+} + V_{PPSE-}$

where	V_{PPD} represents the differential voltage peak to peak
	V_{PPSE} represents the single-ended voltage peak to peak
	V_{DO} represents the differential offset voltage
	V_{CMO} represents the common mode offset voltage

Note The instantaneous differential voltage is equal to *Output (CH+) – Output (CH–)*. Output offset settings are independent of gain settings.

Analog Outputs

CH 0+/–, CH 1+/– (Analog Outputs, Front Panel Connectors)

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td>Number of Channels</td><td colspan="4">2</td><td>—</td></tr>
<tr><td>Output Type</td><td colspan="4">Single Ended, Differential</td><td>Single-ended output available on main path only.</td></tr>
<tr><td>Output Paths</td><td colspan="4">Main Path, Direct Path</td><td>—</td></tr>
<tr><td>DAC Resolution</td><td colspan="4">16 bits</td><td>—</td></tr>
<tr><td colspan="6">Amplitude and Offset [1]</td></tr>
<tr><td rowspan="10">Full Scale Amplitude Range [2]</td><td colspan="4">Single-Ended Main Path</td><td rowspan="10">Measured on CH +.
V_{pk} on each terminal is equal to analog offset + waveform data × gain.</td></tr>
<tr><td rowspan="2">Flatness Correction State</td><td rowspan="2">Load</td><td colspan="2">Amplitude (V_{PPSE}) [3]</td></tr>
<tr><td>Minimum Value</td><td>Maximum Value</td></tr>
<tr><td rowspan="3">Disabled</td><td>50 Ω</td><td>0.00176</td><td>2.50</td></tr>
<tr><td>1 kΩ</td><td>0.00336</td><td>4.76</td></tr>
<tr><td>Open</td><td>0.00352</td><td>5.00</td></tr>
<tr><td rowspan="3">Enabled</td><td>50 Ω</td><td>0.00124</td><td>1.75</td></tr>
<tr><td>1 kΩ</td><td>0.00235</td><td>3.33</td></tr>
<tr><td>Open</td><td>0.00247</td><td>3.50</td></tr>
<tr></tr>
<tr><td rowspan="3"></td><td colspan="4">Differential Main Path</td><td rowspan="2">Measured as differential $V_{pk\text{-}pk}$. Each terminal $V_{pk\text{-}pk}$ is half of the differential $V_{pk\text{-}pk}$.</td></tr>
<tr><td rowspan="2">Flatness Correction State</td><td rowspan="2">Load</td><td colspan="2">Amplitude (V_{PPD}) [3]</td></tr>
<tr><td>Minimum</td><td>Maximum Value</td><td></td></tr>
</table>

Specification			Value		Comments
			Value		V_{pk} on each terminal is equal to differential offset × 0.5 + common-mode offset + waveform data × gain/2.
	Disabled	50 Ω	0.00352	5.00	
		1 kΩ	0.00671	9.52	
		Open	0.00705	10.00	
	Enabled	50 Ω	0.00247	3.50	
		1 kΩ	0.00470	6.66	
		Open	0.00493	7.00	
Differential Direct Path				Both CH 0+/– or CH 1+/– terminals are terminated to ground through loads of the same value. Single-ended values are half of differential values.	
Flatness Correction State	Load	Amplitude (V_{PPD}) [3]			
		Minimum Value	Maximum Value		
Disabled	50 Ω	0.708	1.00		
	1 kΩ	1.35	1.90		
	Open	1.42	2.00		
Enabled	50 Ω	0.567	0.8		
	1 kΩ	1.08	1.52		
	Open	1.14	1.6		
Amplitude Resolution	4 digits < 0.0025% (0.0002 dB of amplitude range)				—
Analog Offset Range, per terminal	Main Path [4]				Both CH 0+/– or CH 1+/– terminals are terminated to ground through loads of the same value. Offset is any combination of common-mode offset voltage and differential offset voltage.
	Load		Amplitude (V_{pk}) [5] [2]		
	50 Ω		±1.00		
	1 kΩ		±1.905		
	Open		±2.00		
	Direct Path				
	Load		Amplitude (V_{pk}) [5] [2]		
	Any		—		
Offset Resolution	Main Path				Applies to differential, common-mode, and single-ended offsets.
	4 digits < 0.002% of offset range				

Specification	Value	Comments
Accuracy		
DC Accuracy	Single-Ended Main Path	Measured with a DMM. Measured with both output terminals terminated to ground through a high impedance.
	Absolute Gain Error: within ±5 °C of Self-Cal temperature: ±(0.4% of single-ended output range [6] + 0.5 mV) ±(0.3% of single-ended output range [6] + 0.3 mV), typical outside of ± 5 °C of Self-Cal temperature: – 0.05%/°C – 0.035%/°C, typical Offset Error: ±(0.15% of offset + 0.04% of single-ended output range [6] + 1.25 mV) (0 °C to 55 °C) ±(0.08% of offset + 0.025% of single-ended output range [6] + 0.75 mV) (0 °C to 55 °C), typical	
DC Accuracy	Differential Main Path	Measured with a DMM. Measured with both output terminals terminated to ground through a high impedance.
	Absolute Gain Error:	
	within ±5 °C of Self-Cal temperature: ±(0.6% of differential output range [7] + 1 mV)	

Specification	Value	Comments
	±(0.43% × differential output range [7] + 500 μV), typical outside of ±5 °C of Self-Cal temperature: – 0.05%/°C – 0.035%/°C, typical Differential Offset: ± (0.3% of differential offset + 0.01% of differential output range [7] + 2 mV) ± (0.16% of differential offset + 0.01% of differential output range [7] + 1 mV), typical Common Mode Offset: ± (0.3% of common-mode offset + 2 mV) ± (0.16% of common-mode offset + 1 mV), typical **Channel-to-Channel Relative** Gain Error: within ±5 °C of Self-Cal temperature: ±(0.66% of differential output range [7] + 1.75 mV) outside of ±5 °C of Self-Cal temperature: – 0.02%/°C – 0.01%/°C, typical	
DC Accuracy	Differential Direct Path **Absolute** Gain Error: within ±5 °C of Self-Cal temperature: ±0.2% of differential output range [8] outside of ±5 °C of Self-Cal temperature: + 0.030%/°C + 0.015%/°C, typical Differential Offset: ± 1 mV (0 °C to 55 °C) Common Mode Offset [9] : ±350 μV (0 °C to 55 °C) **Channel-to-Channel Relative** Gain Error: within ±5 °C of Self-Cal temperature: ±0.08% of differential output range [8] outside of ±5 °C of Self-Cal temperature: + 0.010%/°C + 0.005%/°C, typical	Measured with a DMM. Differential offset is not adjusted during self-calibration. Measured with both output terminals terminated to ground through a high impedance.

Specification	Value	Comments
Accuracy (Continued)		
AC Amplitude Accuracy	Single-Ended Main Path **Absolute** within ±5 °C of Self-Cal temperature: ±(0.8% of single-ended output range + 1 mV_{RMS}) ±(0.4% of single-ended output range + 750 μV_{RMS}), typical	Measured using a DMM, with full-scale data into high- impedance, 50 kHz sine wave, 400 MS/s. The output range defined in DC Accuracy must be converted to V_{RMS} by dividing by $(2\sqrt{2})$.
	Differential Main Path **Absolute** within ±5 °C of Self-Cal temperature: ±(0.8% of differential output range + 1.5 mV_{RMS}) ±(0.4% of differential output range + 1.5 mV_{RMS}), typical	
	Differential Direct Path **Absolute** within ±5 °C of Self-Cal temperature: ±0.5% of differential output range	

	Channel-to-Channel, Relative within ±5 °C of Self-Cal temperature: ±0.2% of differential output range ±0.07% of differential output range, typical	

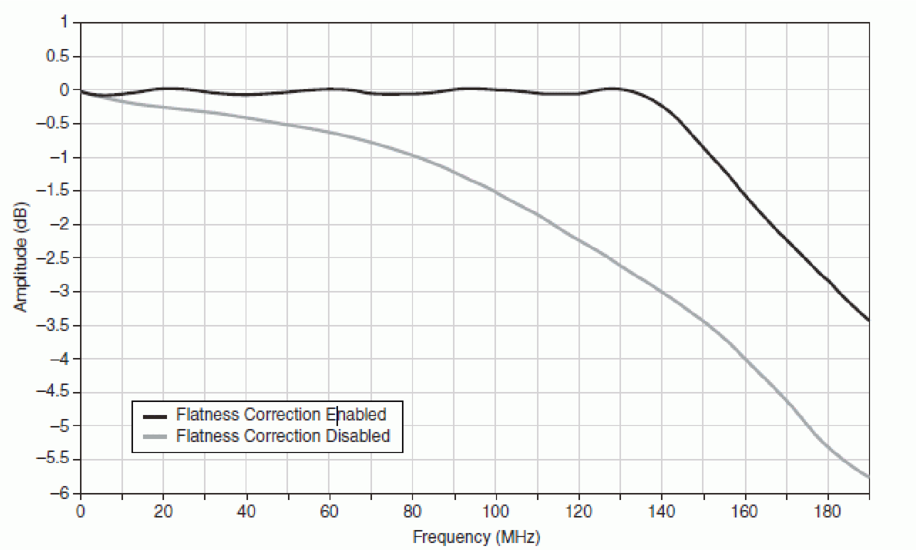
Specification	Value		Comments
Accuracy (Continued)			
Channel-to-Channel Timing Alignment Accuracy	Main Path	Direct Path	±5 °C of self-calibration temperature. Alignment can be improved with manual adjustment by using Sample Clock Delay. Refer to the *Sample Clock Delay* specification in the *Onboard Sample Clock* section for more information.
	50 ps 40 ps, typical	35 ps 25 ps, typical	

Specification	Value			Comments
Output Characteristics				
DC Output Resistance	Main Path	Direct Path		For the direct path only, both output terminals must be terminated with the same impedance to ground.
	50 Ω nominal, per connector	50 Ω nominal, per connector		
Return Loss	Single-Ended and Differential Main Path	Single-Ended Direct Path	Differential Direct Path	Nominal.
	30 dB, up to 20 MHz 27 dB, up to 60 MHz 12 dB, up to 135 MHz	26 dB, 5 MHz to 60 MHz 15 dB, 60 MHz to 145 MHz	35 dB, up to 20 MHz 22 dB, up to 60 MHz 12 dB, up to 145 MHz	
Load Impedance Compensation	Output amplitude is compensated for user-specified load impedance to ground. [10]			Performed in software.
Output Coupling	DC			—
Output Enable	Software-selectable. When disabled, output is terminated with a 50 Ω, 1 W resistor.			—
Maximum Output Overload	Main Path	Direct Path		For the direct path only, both CH 0+/– or CH 1+/– terminals are terminated to ground through loads of the same value.
	±12 V_{pk} from a 50 Ω source	±8 V_{pk} from a 50 Ω source		
Waveform Summing	The output terminals support waveform summing. The outputs of multiple NI 5451 signal generators can be connected together.			Clipping may occur if the summed voltage is outside of the maximum voltage range.

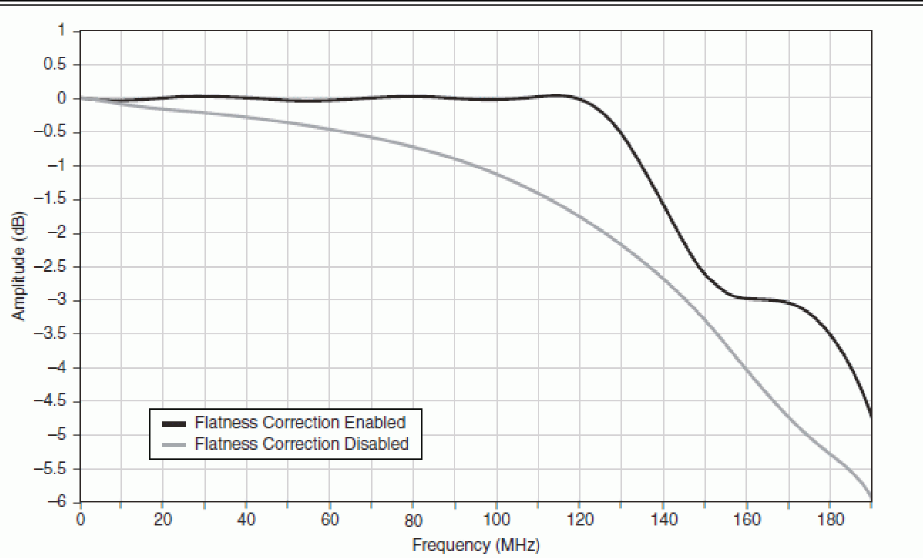
Specification	Value		Comments
Frequency Response			
Analog Bandwidth	Baseband	Complex Baseband	Typical. –3 dB, 400 MS/s. Includes DAC sinc response. Flatness correction disabled.
	Main Path, Filter Disabled		
	180 MHz for each I and Q output	360 MHz when used with external I/Q modulator	
	Main Path, Filter Enabled		
	135 MHz for each I and Q output	270 MHz when used with external I/Q modulator	
	Direct Path		
	145 MHz for each I and Q output	290 MHz when used with external I/Q modulator	
Analog Filter	Main Path	Direct Path	
	7-pole elliptic filter for image suppression	4-pole filter for image suppression	
Passband Flatness	Single-Ended and Differential Main Path, Filter Enabled [11]		With respect to 50 kHz into 100 Ω differential load, 400 MS/s. [12] Flatness correction corrects for analog frequency response and DAC sinc response up to 0.3375 × sample rate. Receiver return loss may degrade flatness.
	Flatness Correction Disabled	Flatness Correction Enabled [13] [12]	
0 MHz to 60 MHz [12] [14]	0.8 dB, typical	±0.30 dB	
		±0.20 dB, typical	
60 MHz [12] [14] to 135 MHz [12] [15]	3 dB, typical	±0.50 dB	

Specification	Value		Comments
		±0.30 dB, typical	
Channel-to-Channel Passband Flatness Matching 0 MHz to 60 MHz [12, 14]	±0.12 dB, typical	±0.12 dB, typical	With respect to 50 kHz on each channel, 400 MS/s. Load variations may degrade performance. Refer to the *AC Amplitude Accuracy* Main Path specification for the correct terminal configuration for the 50 kHz reference accuracy.
Channel-to-Channel Passband Flatness Matching 60 MHz [12, 14] to 135 MHz [12, 15]	±0.20 dB, typical	±0.14 dB, typical	
Passband Flatness	Direct Path		With respect to 50 kHz into 100 Ω differential load, 400 MS/s [12]. Flatness correction corrects for analog frequency response and DAC sinc response up to 0.3 × sample rate. Receiver return loss may degrade flatness.
	Flatness Correction Disabled	Flatness Correction Enabled [13, 12]	
0 MHz to 60 MHz [12, 16]	0.5 dB, typical	±0.24 dB ±0.13 dB, typical	
60 MHz [12, 16] to 120 MHz [12, 17]	1.9 dB, typical	±0.34 dB ±0.19 dB, typical	
Channel-to-Channel Passband Flatness Matching 0 MHz to 60 MHz [12, 16]	0.05 dB, typical	0.03 dB, typical	With respect to 50 kHz on each channel, 400 MS/s. Load variations may degrade performance. Refer to the AC Amplitude Accuracy *Differential Direct Path* specification for more information about the 50 kHz reference accuracy.
Channel-to-Channel Passband Flatness Matching 60 MHz [12, 16] to 120 MHz [12, 17]	0.18 dB, typical	0.04 dB, typical	

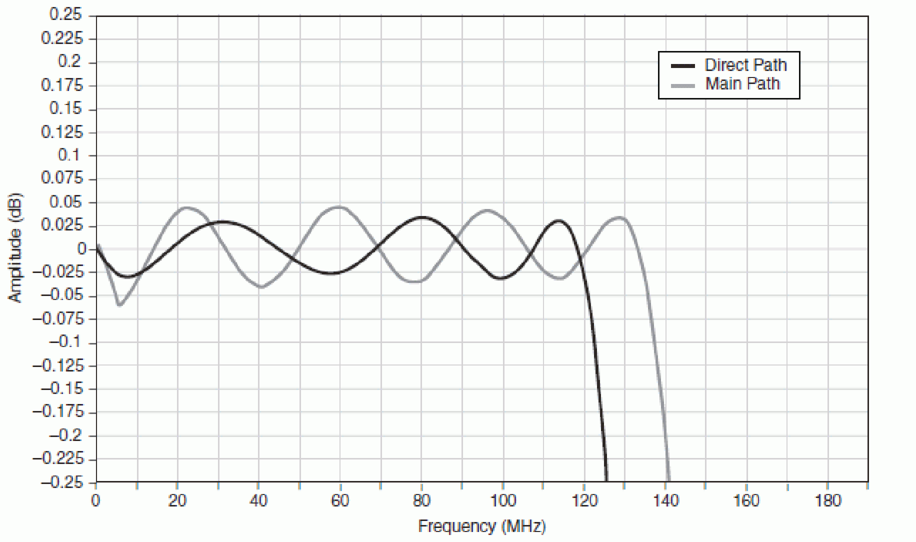
Main Path Filter Enabled Amplitude Response with Flatness Correction Enabled and Disabled, 400 MS/s, Gain=2.5, Differential, Referenced to 50 kHz, Representative Unit



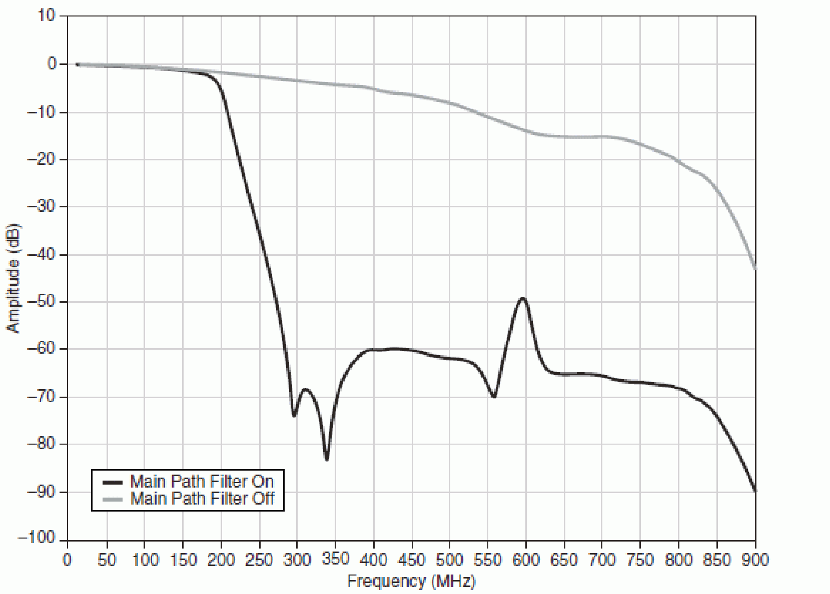
Direct Path Amplitude Response with Flatness Correction Enabled and Disabled,400 MS/s, Differential, Referenced to 50 kHz, Representative Unit



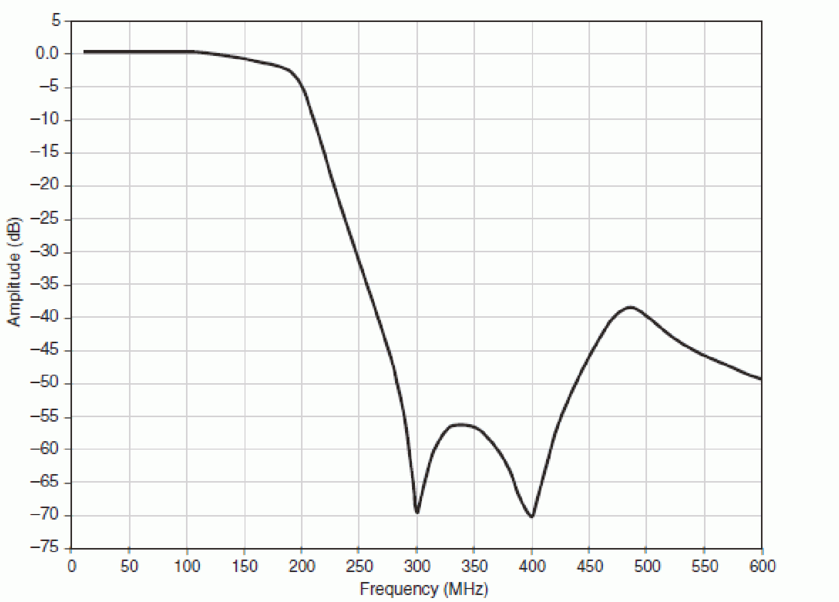
Main and Direct Path Amplitude Response with Flatness Correction Enabled, 400 MS/s, Differential, Referenced to 50 kHz, Representative Unit



Main Path Characteristic Frequency Response of Image Suppression Filter, Representative Unit



Direct Path Characteristic Frequency Response of Image Suppression Filter, Representative Unit



Note Sinc response due to DAC sampling is not included in the previous two figures.

Specification	Value								Comments
Spectral Characteristics									
Spurious Free Dynamic Range (SFDR) at 1 MHz	SFDR (dB)								Nominal. 400 MS/s, amplitude –1 dBFS. Includes aliased harmonics. Differential output measured single-ended with a balun, or differential amp. Terminated into 50 Ω to ground on each terminal.
	Frequency Range	Single-Ended Main Path			Differential Main Path			Differential Direct Path	
		Gain = 0.25 0.5 V_{PPSE}	Gain = 0.75 1.25 V_{PPSE}	Gain = 1.25 2.5 V_{PPSE}	Gain = 0.5, 1 V_{PPD}	Gain = 1.25, 2.5 V_{PPD}	Gain = 2.5, 5 V_{PPD}	Gain = 0.5, 1 V_{PPD}	
SFDR with Harmonics	DC to 7 MHz	82			85			88	
	DC to 200 MHz	75			75			75	
SFDR without Harmonics	DC to 7 MHz	82	88	95	98			98	
	DC to 200 MHz	82	83	84	84			84	

Specification	Value								Comments
Spectral Characteristics (Continued)									
SFDR with Harmonics	SFDR (dB)								400 MS/s, amplitude –1 dBFS. Measured from DC to 200 MHz. All values are typical and include aliased harmonics. Differential output measured single-ended with balun. Terminated into 50 Ω to ground on each terminal.
	Frequency	Single-Ended Main Path			Differential Main Path			Differential Direct Path	
		Gain = 0.5, 0.5 V_{PPSE}	Gain = 1.25, 1.25 V_{PPSE}	Gain = 2.5, 2.5 V_{PPSE}	Gain = 0.5, 1 V_{PPD}	Gain = 1.25, 2.5 V_{PPD}	Gain = 2.5, 5 V_{PPD}	Gain = 0.5, 1 V_{PPD}	
	10 MHz	73 (75)[*]	73 (75)[*]	73 (75)[*]	73 (75)[*]	73 (75)[*]	73 (73)[*]	73 (75)[*]	
	60 MHz	65	61	56	61	67	64	70 (72)[*]	
	100 MHz	53	52	49	52	54	53	60	
	120 MHz	62	62	62	62	62	62	62	
	160 MHz	—						62	

[*] Long, non-repetitive waveforms like modulated signals offer better spurious performance. For periodic waveforms represented by a small number of unique samples, DAC nonlinearities limit dynamic specifications.

Note The first specification listed is for a 10.0 MHz sinusoid at a 400 MS/s sample rate (waveform contains 40 unique samples), while the specification in parentheses is for a 10.0 MHz sinusoid at a 399.9 MS/s sample rate (waveform contains over 3000 unique samples with unique DAC codes).

Specification	Value			Comments
Spectral Characteristics (Continued)				
SFDR without Harmonics	Frequency	SFDR (dB)		400 MS/s sample rate. Amplitude –1 dBFS. Measured from DC to 200 MHz. All values are typical and include aliased harmonics. Differential output measured single-ended with balun. Characterized at the same gain ranges as SFDR with Harmonics.
		Single-Ended and Differential Main Path	Differential Direct Path	
	10 MHz	74 (76)[*]	74 (76)[*]	
	60 MHz	72 (74)[*]	72 (74)[*]	
	100 MHz	66	64	
	120 MHz	62	62	
	160 MHz	—	62	

[*] Long, non-repetitive waveforms like modulated signals offer better spurious performance. For periodic waveforms represented by a small number of unique samples, DAC nonlinearities limit dynamic specifications.

Note The first specification listed is for a 10.0 MHz sinusoid at a 400 MS/s sample rate (waveform contains 40 unique samples), while the specification in parentheses is for a 10.0 MHz sinusoid at a 399.9 MS/s sample rate (waveform contains over 3000 unique samples with unique DAC codes).

Specification	Value		Comments
Spectral Characteristics (Continued)			
Out of Band Performance	In-Band Tone Frequency (MHz)	Out of Band Spur Level (dBm)	Nominal. Generating full-scale sine wave at frequency listed, 400 MS/s. Measured 200 MHz to 2 GHz. Anti-imaging filter is fixed and optimized for 400 MS/s.

Specification	Value		Comments
	Main Path, Filter Enabled		
	0 to 20	<–65 dBm	
	20 to 50	<–45 dBm	
	Direct Path		
	0 to 20	<–80 dBm	
	20 to 50	<–65 dBm	
Channel-to-Channel Crosstalk	Aggressor Output Amplitude	Main Path*	Measured single ended at the victim channel, 0 V DC output, 400 MS/s sample rate. Aggressor channel is terminated into 50 Ω, sine wave output, 400 MS/s sample rate. All values nominal.
	2.5	–90 dBc, 0 MHz to 200 MHz	
	1.25	–85 dBc, 0 MHz to 200 MHz	
	0.5	–80 dBc, 0 MHz to 200 MHz	
	0.15	–70 dBc, 0 MHz to 200 MHz	
	Direct Path		
	<80 dBc, 0 MHz to 200 MHz <90 dBc, 0 MHz to 150 MHz		

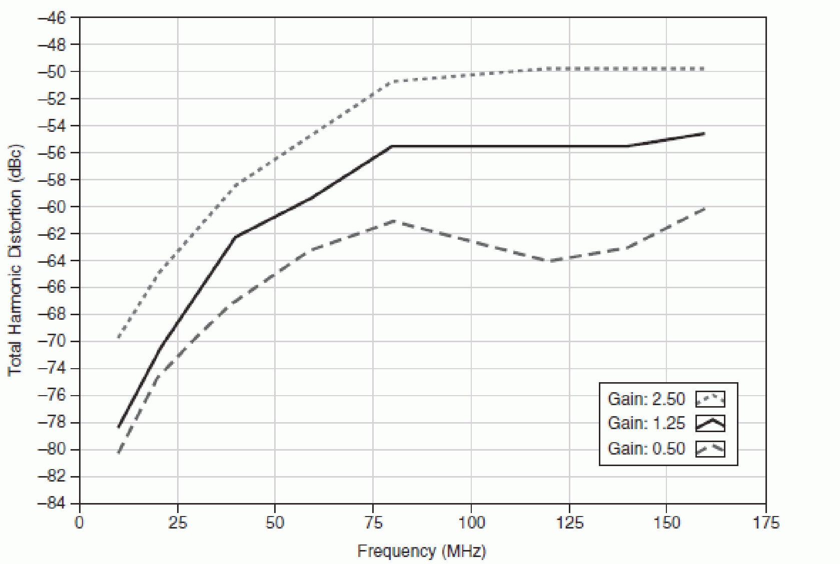
* The dBc values are referenced to the differential tone power on the aggressor channel. Results are independent of victim and aggressor filter configurations, terminal configurations, and victim channel output amplitude.

Specification	Value				Comments
Spectral Characteristics (Continued)					
Total Harmonic Distortion (THD)	Main Path				Amplitude –1 dBFS. Includes the 2nd through the 6th harmonic. All values are typical. Measured at 0.1 MHz offset. 400 MS/s sample rate. Differential main path output measured single ended with a balun.
	Output Amplitude	Frequency (MHz)	THD (dBc)		
			Single-Ended	Differential	
	2.5 V_{PPSE}, 5 V_{PPD}	10	–71	–71	
		20	–66	–69	
		40	–59	–64	
		60	–55	–61	
		80	–51	–55	
		120	–50	–51	
		140	–50	–52	
		160	–50	–53	
	1.25 V_{PPSE}, 2.5 V_{PPD}	10	–78	–75	
		20	–72	–73	
		40	–63	–69	
		60	–60	–65	
		80	–56	–59	
		120	–56	–59	
		140	–56	–59	
		160	–55	–59	
	0.5 V_{PPSE}, 1 V_{PPD}	10	–80	–79	
		20	–74	–75	
		40	–68	–69	
		60	–64	–69	
		80	–62	–65	
		120	–65	–70	
		140	–64	–69	
		160	–61	–66	
Total Harmonic Distortion (THD)	Direct Path				Amplitude –1 dBFS. Includes the 2nd through the 6th harmonic.
	Output Amplitude	Frequency (MHz)	THD (dBc)		

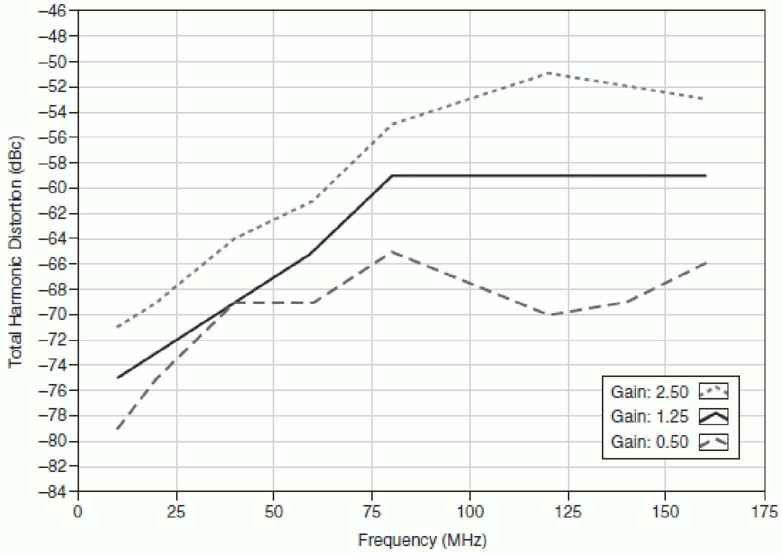
Specification	Value			Comments
	0.5 V_{PPSE}, 1 V_{PPD}	10	–75	All values are typical. Measured at 0.1 MHz offset. 400 MS/s sample rate. Differential direct path output measured single ended with a balun.
		20	–70	
		40	–68	
		80	–68	
		100	–68	
		120	–78	
		160	–83	
Spectral Characteristics (Continued)				
Intermodulation Distortion (IMD_3)	Single-Ended and Differential Main Path			The waveform amplitude for each tone is –7 dBFS. Typical. 400 MS/s sample rate. Two-tone frequencies are frequency ±100 kHz.
	Output Amplitude	Frequency (MHz)	IMD (dBc)	
	2.5 V_{PPSE}, 5 V_{PPD}	10	–87	
		20	–82	
		40	–71	
		60	–63	
		80	–57	
		120	–51	
		160	–48	
	1.25 V_{PPSE}, 2.5 V_{PPD}	10	–92	
		20	–87	
		40	–79	
		60	–72	
		80	–66	
		120	–61	
		160	–57	
	0.5 V_{PPSE}, 1 V_{PPD}	10	–87	
		20	–85	
		40	–82	
		60	–79	
		80	–75	
		120	–79	
		160	–75	
Spectral Characteristics (Continued)				
Intermodulation Distortion (IMD_3)	Single-Ended and Differential Main Path			The digital amplitude for each tone is –7 dBFS. All values are typical. 400 MS/s sample rate. Two-tone frequencies are frequency ±100 kHz. Differential direct path output measured single-ended with balun.
	Output Amplitude	Frequency (MHz)	IMD (dBc)	
	0.1 V_{PPSE}, 0.2 V_{PPD}	10	–89	
		20	–83	
		40	–78	
		60	–73	
		80	–69	
		120	–66	
		160	–65	
	Direct Path			
	Output Amplitude	Frequency (MHz)	IMD (dBc)	
	0.5 V_{PPSE}, 1 V_{PPD}	10	–84	
		20	–81	
		40	–75	
		80	–71	
		100	–68	
		120	–68	
		160	–66	

Specification	Value					Comments
Spectral Characteristics (Continued)						
Average Noise Density	Output Amplitude	Average Noise Density				Average noise density from DC to 200 MHz generating –40 dBFS, 1 MHz sine wave at 400 MS/s. Differential output measured with a balun. Differential dBm numbers referred back to a 50 Ω system.
	Single-Ended Main Path					
	VPPSE	dBm	$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	dBm/Hz	dBFS/Hz	
	2.5	12	12.57	–145	–157	
	0.5	–2	9.99	–147	–145	
	0.06	–20.4	9.99	–147	–126.6	
	Differential Main Path					
	VPPD	dBm	$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	dBm/Hz	dBFS/Hz	
	5	18	17.76	–142	–160	
	1	4	14.11	–144	–148	
	0.12	–14.4	14.11	–144	–129.6	
	Differential Direct Path					
	VPPD	dBm	$\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$	dBm/Hz	dBFS/Hz	
	1	4.0	2.24	–160	–164	

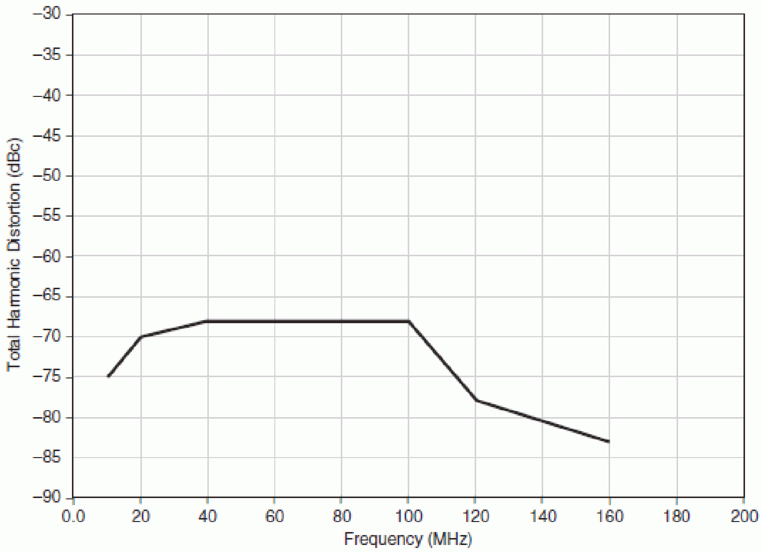
Single-Ended Main Path, Total Harmonic Distortion, Typical



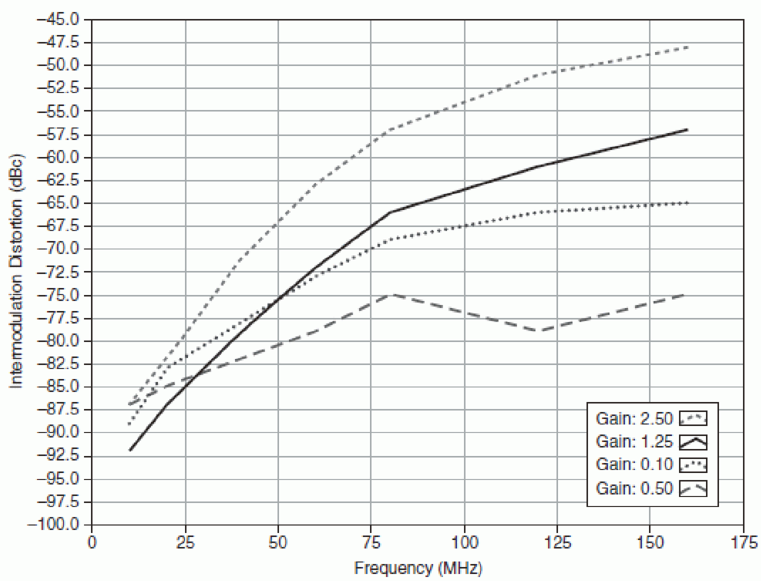
Differential Main Path, Total Harmonic Distortion, Typical



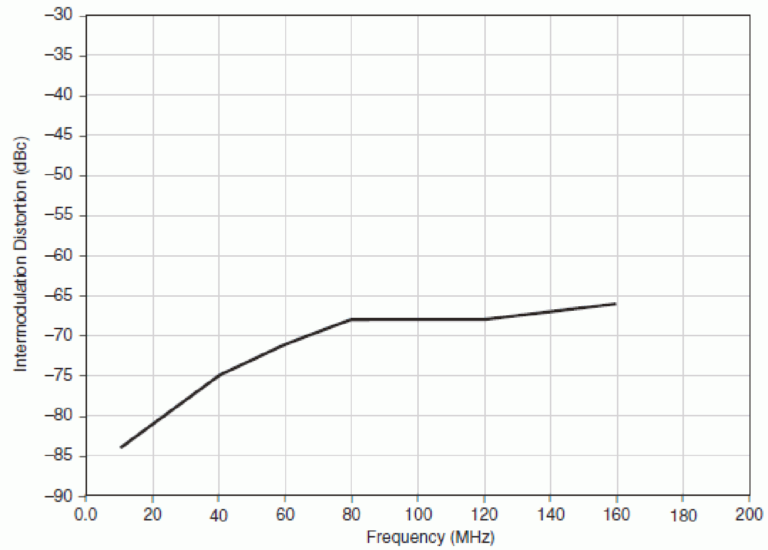
Direct Path, Total Harmonic Distortion, Typical



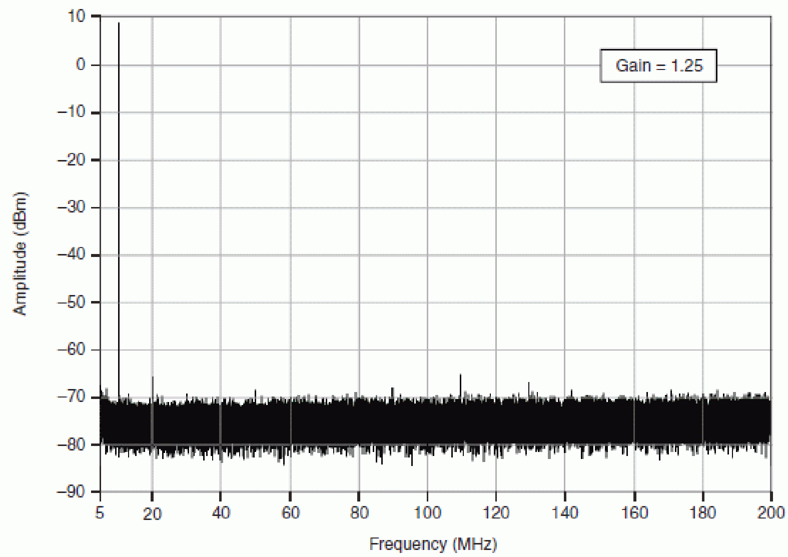
Single-Ended and Differential Main Path, Intermodulation Distortion, 200 kHz Separation, Typical



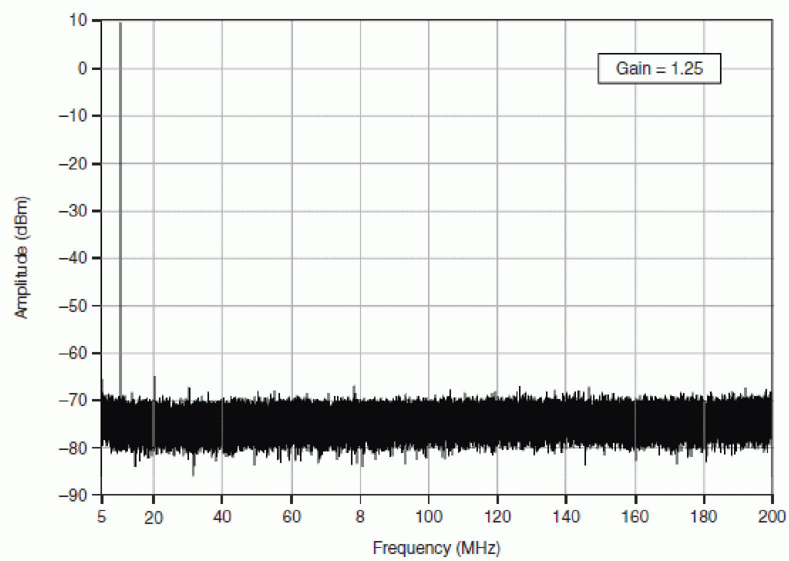
Direct Path, Intermodulation Distortion, 200 kHz Separation, Typical



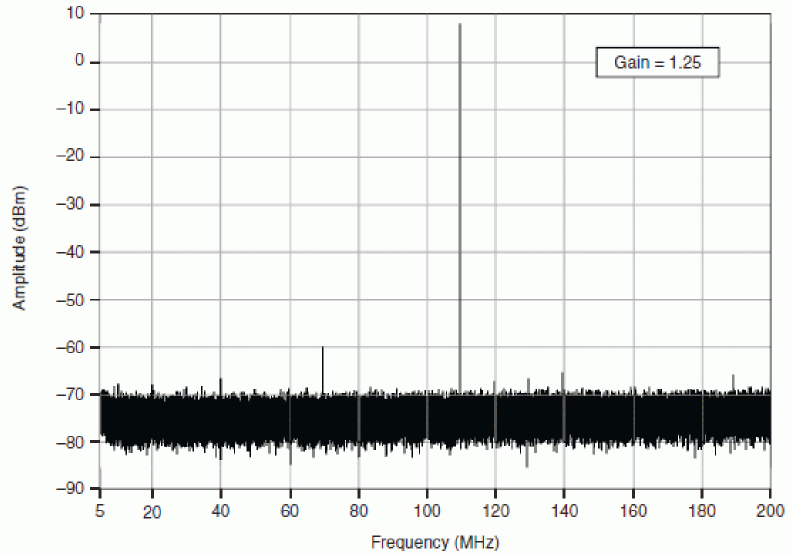
Single-Ended Main Path 10.000 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit



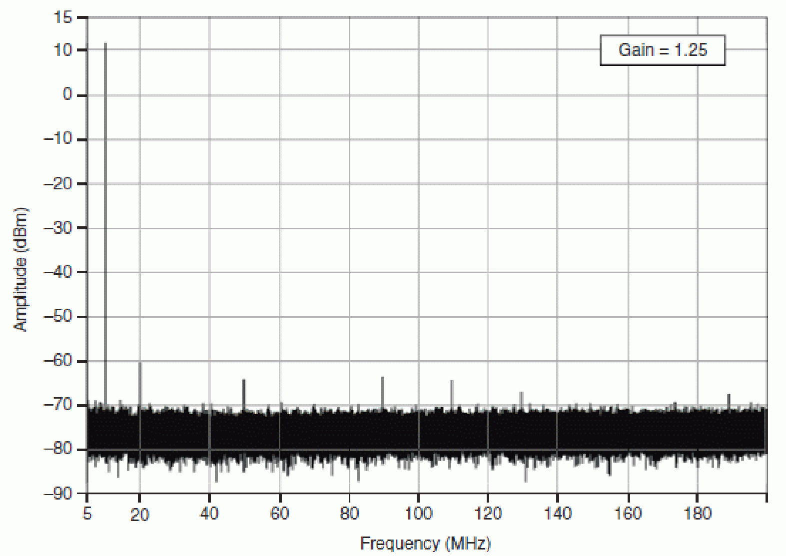
Single-Ended Main Path 10.100 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit



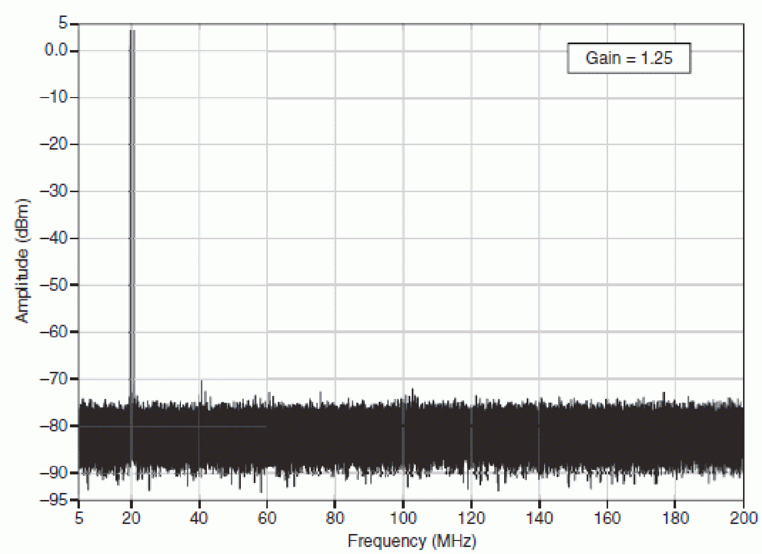
Single-Ended Main Path 110.100 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit



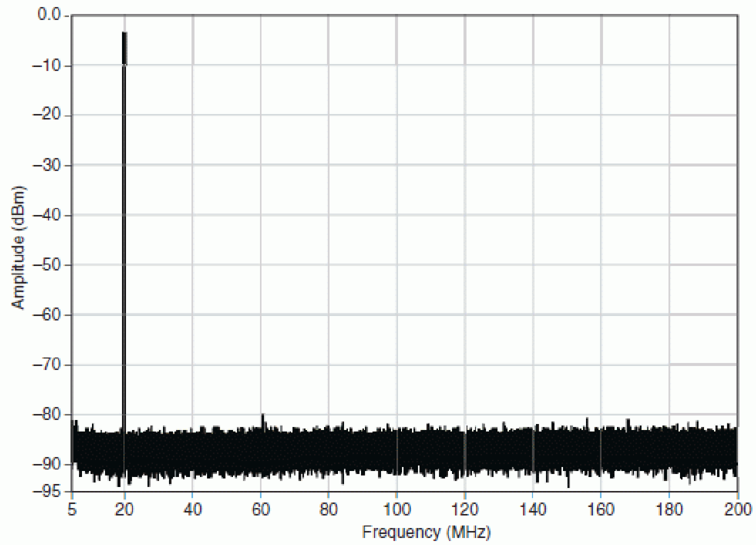
Differential Main Path 10.000 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, measured through a balun, Representative Unit



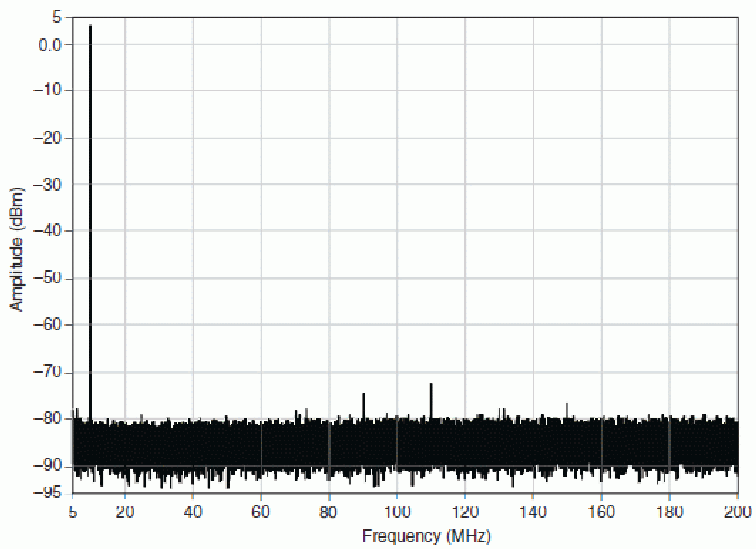
Single-Ended Main Path Intermodulation Distortion, 1 MHz Separation, 20 MHz Tone, 400 MS/s, –7 dBFS, Representative Unit



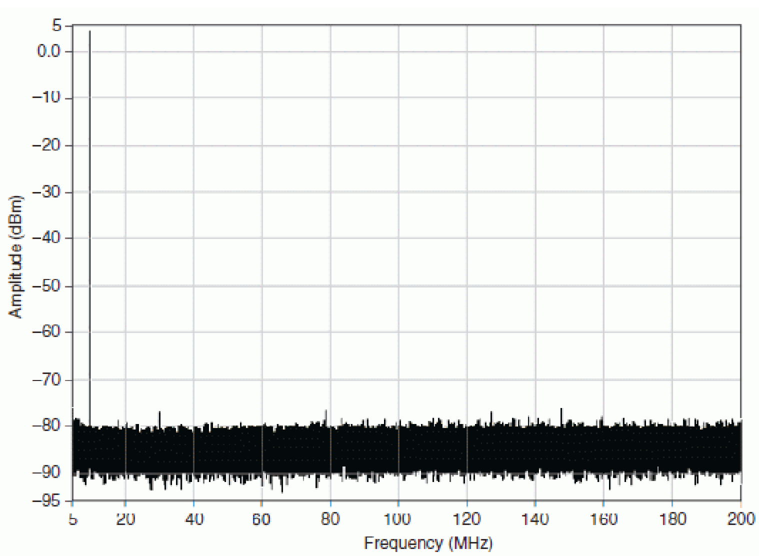
Direct Path Intermodulation Distortion, 1 MHz Separation, 20 MHz Tone, 400 MS/s, –7 dBFS, Representative Unit



Direct Path 10.000 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit



Direct Path 10.100 MHz Single-Tone Spectrum, 400 MS/s, –1 dBFS, Representative Unit



Note The noise floor on all spectral graphs is limited by the measurement device.

Specification	Value	Comments
Output Phase Noise and Jitter *		

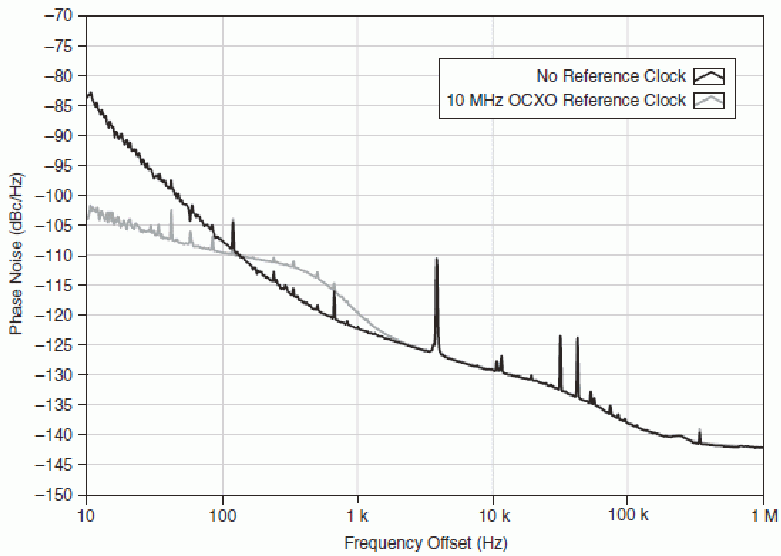
Specification	Value							Comments
Sample Clock Source	Output Freq. (MHz)	System Phase Noise Density† (dBc/Hz)					System Output Integrated Jitter†	—
		100 Hz	1 kHz	10 kHz	100 kHz	1 MHz		
Internal, High Resolution Clock, 400 MS/s	10	<–121	<–137	<–146	<–152	<–153	<350 fs	Typical.
	100	<–101	<–119	<–126	<–136	<–141	<350 fs	
CLK IN External 10 MHz Reference Clock,400 MS/s	10	<–122	<–135	<–146	<–152	<–153	<350 fs	Typical.
	100	<–105	<–115	<–126	<–136	<–141	<350 fs	

*Generating sine wave at an output frequency of 400 MS/s.

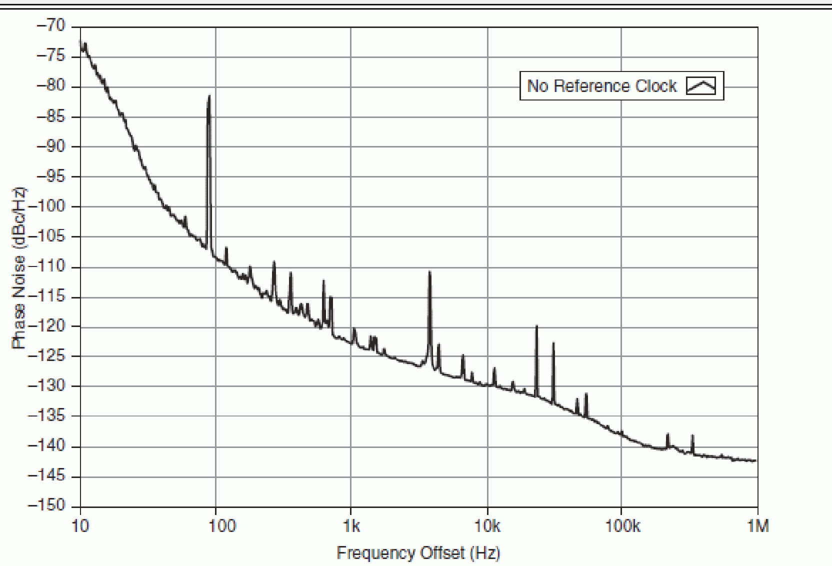
† System output jitter integrated from 100 Hz to 100 kHz.

Note Specifications valid for both main path and direct path, limited by the output noise floor.

Phase Noise on a Representative Module, 100 MHz Sine Wave, 400 MS/s Internal Clock Sample Rate, Chassis Fans Low, Shown With and Without a Reference Clock



Phase Noise on a Representative Module, 100 MHz Sine Wave, 400 MS/s Internal Clock Sample Rate, Chassis Fans High, No Reference Clock



Specification	Value		Comments
Suggested Maximum Frequencies for Common Functions			
	Main Path	Direct Path	The Direct path is optimized for frequency-domain performance.
Sine	135 MHz	145 MHz	
Square	150 MHz*	33 MHz (<133 V/µs slew rate)†	
Ramp	20 MHz*	1 MHz (<50 V/µs slew rate)†	

Specification	Value		Comments
Triangle	20 MHz* (5 MHz)	8 MHz	
Pulse Response			
Rise/Fall Time (10% to 90%)	Flatness Correction Disabled	Flatness Correction Enabled	Typical. Values into 50 Ω at each output.
	Main Path, Filter Disabled		
	1.5 ns	—	
	Main Path, Filter Enabled		
	3 ns	3 ns	
	Direct Path		
	3 ns	2.5 ns	
Aberration	Flatness Correction Disabled	Flatness Correction Enabled	Typical. Values into 50 Ω at each output.
	Main Path, Filter Disabled		
	3%	—	
	Main Path, Filter Enabled†		
	18%	25%	
	Direct Path*		
	18% (7%)‡	22%	

* Filter Disabled.

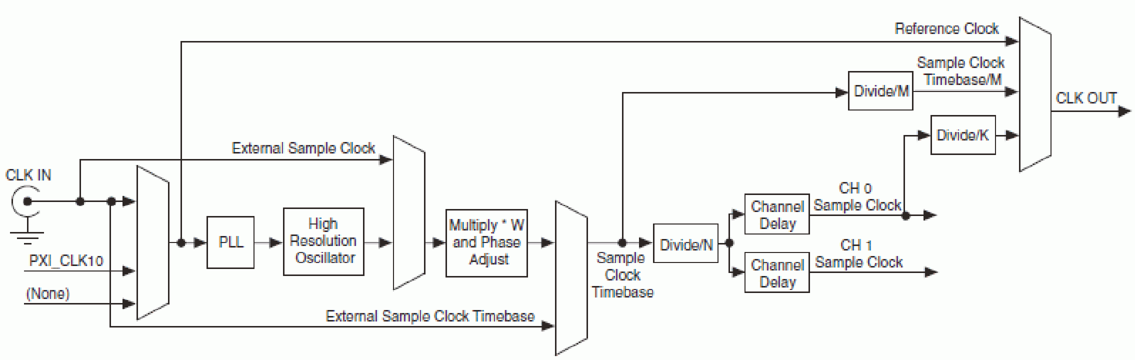
† Aberrations on pulsed waveforms are due to the analog reconstruction filter and can be significantly reduced if waveform data has limited slew rate. Waveforms with higher slew rates are not recommended.

‡ 7% aberrations achievable with 133 V/μs slew rate limiting on waveform data. Pulsed waveforms should contain multiple data points per rising or falling edge, regardless of DAC rate or signal frequency.

Clocking

The clocking of the NI 5451 is very flexible. Waveform generation is driven by the Sample clock. You have multiple choices for configuring the device clocking, as shown in the following figure.

NI PXIe-5451 Clocking

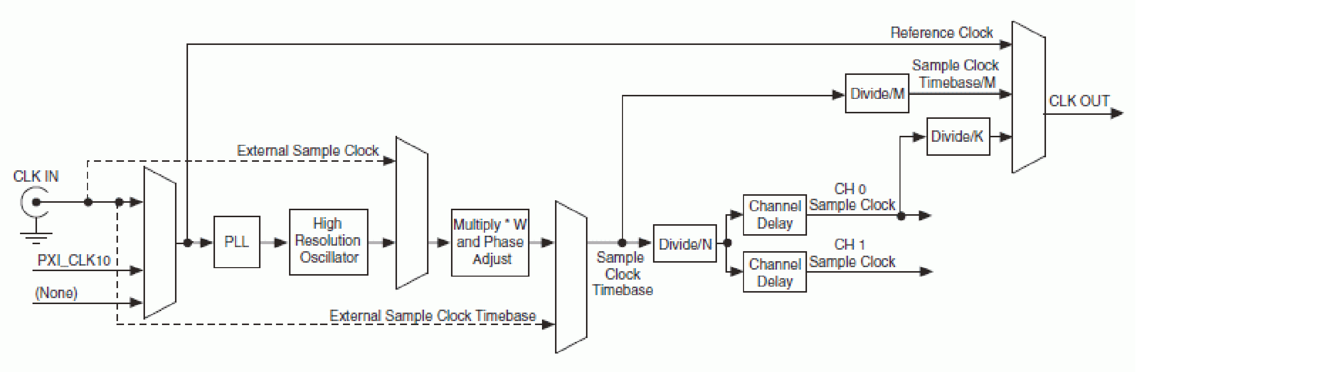


Tip Refer to the clocking documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Devices»NI 5451»Theory of Operation»Clocking** for more information about clocking options on the NI 5451.

Onboard Sample Clock

The following figure shows the NI 5451 onboard Sample clock path.

NI PXIe-5451 Onboard Sample Clock and External Reference Clock Path

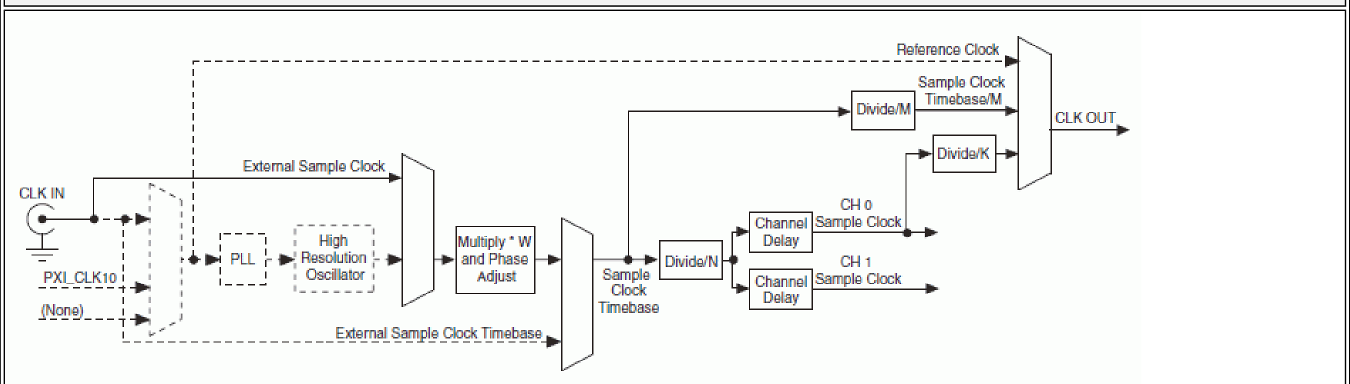


Specification	Value	Comments
Sample Clock Rate Range	12.2 kS/s to 400 MS/s	—
Sample Clock Rate Frequency Resolution	<5.7 µHz	Varies with Sample clock frequency. Specification is worst-case.
Sample Clock Delay	0 ns to 2 ns, independent per channel	Set in software with the Channel Delay property or the *NIFGEN_ATTR_CHANNEL_DELAY* attribute.
Sample Clock Delay Resolution	10 ps	Nominal.
Sample Clock Timebase Phase Adjust	±1 Sample clock timebase period	—
Reference Clock Sources	1. None (internal reference) 2. PXI_CLK10 (backplane) 3. CLK IN (front panel connector)	—
Reference Clock Frequency	1 MHz to 100 MHz in increments of 1 MHz 100 MHz to 200 MHz in increments of 2 MHz 200 MHz to 400 MHz in increments of 4 MHz, Default of 10 MHz.	±0.01% accuracy required
Internal Reference Clock Frequency Accuracy	±0.01%	Measured without an external Reference clock. When locking to a Reference clock, frequency accuracy is solely dependent on the frequency accuracy of the Reference clock source.

External Sample Clock

The following figure shows the NI 5451 external Sample clock path.

NI PXIe-5451 External Sample Clock Path



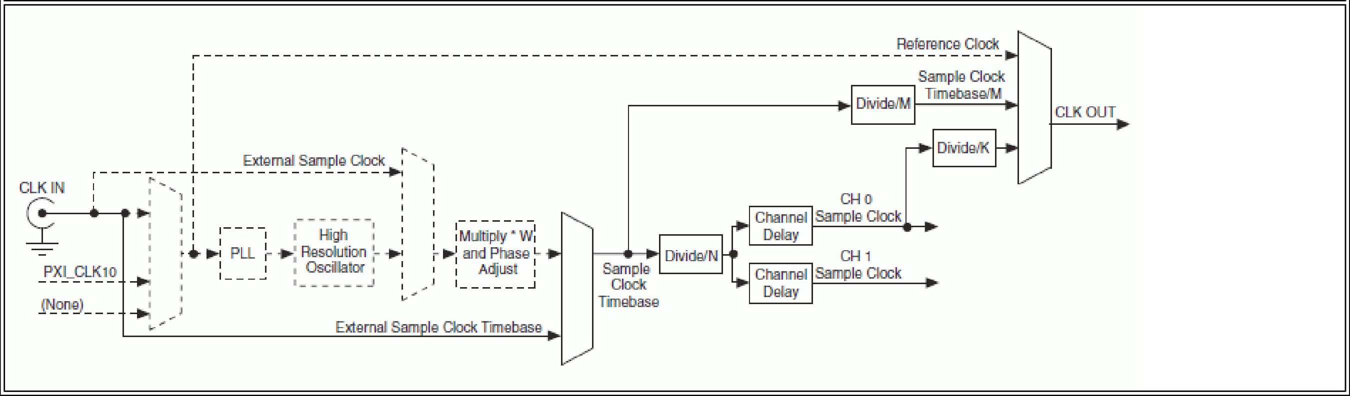
Specification	Value	Comments
External Sample Clock Source	CLK IN, front panel connector, with multiplication and division	—
External Sample Clock Rate	10 MS/s, 20 MS/s to 400 MS/s	—
Sample Clock Rate Range	12.2 kS/s to 400 MS/s	—
Multiplication/Division Factor Range	Varies depending on the external Sample clock rate	Shown as *Multiply*W* and *Divide/N* in the previous figure.
Sample Clock Delay	0 ns to 2 ns, independent per channel	Set in software with the Channel Delay property or the *NIFGEN_ATTR_CHANNEL_DELAY* attribute.

Specification	Value	Comments
Sample Clock Delay Resolution	10 ps	Nominal.
Sample Clock Timebase Phase Adjust	±1 Sample clock timebase period	—

External Sample Clock Timebase

The following figure shows the NI 5451 external Sample clock timebase path.

NI PXIe-5451 External Sample Clock Timebase Path



Specification	Value	Comments
External Sample Clock Timebase Sources	CLK IN, front panel connector, with division	—
External Sample Clock Timebase Rate Range	200 MS/s to 400 MS/s	—
Divide Factor Range	1, 2 to 32768 in steps of 2	Shown as *Divide/N* in the previous figure.
Sample Clock Delay	0 ns to 2 ns, independent per channel	—
Sample Clock Delay Resolution	10 ps	Nominal.

Exporting Clocks

Specification	Value		Comments
	Destination	Rates	
Reference Clock	CLK OUT	1 MHz to 400 MHz	—
	PFI<0..1>	1 MHz to 200 MHz	
Sample Clock	CLK OUT	100 kHz to 400 MHz	With optional divider.
	PFI<0..1>	0 MHz to 200 MHz	
Sample Clock Timebase	CLK OUT	100 kHz to 400 MHz	With optional divider.
	PFI<0..1>	0 MHz to 200 MHz	

Terminals

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Specification	Value	Comments
Direction	Input	—
Destinations	1. Reference clock 2. Sample clock 3. Sample clock timebase	—
Frequency Range	1 MHz to 400 MHz	Not applicable for all destinations. Refer to the specifications for your clocking configuration for applicable ranges.
Input Voltage Range	500 mV_{pk-pk} to 5 V_{pk-pk} into 50 Ω (–2 dBm to +18 dBm)	50% duty cycle input.
	550 mV_{pk-pk} to 4.5 V_{pk-pk} into 50 Ω (–1.2 dBm to +17 dBm)	45% to 55% duty cycle input.
Input Protection Range	6 V_{pk-pk} into 50 Ω 19.5 dBm	50% duty cycle input.
	5.4 V_{pk-pk} into 50 Ω 18.5 dBm	45% to 55% duty cycle input.

Specification	Value	Comments
Duty Cycle Requirements	45% to 55%	—
Input Impedance	50 Ω, nominal	—
Input Coupling	AC	—
Voltage Standing Wave Ratio (VSWR)	1.3:1 up to 2 GHz	Nominal.

CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)

Specification	Value	Comments
Direction	Output	—
Sources	1. Sample clock, divided by integer *K* (1≤ *K* ≤ 3, minimum) 2. Reference clock 3. Sample clock timebase, divided by integer *M* (1 ≤ *M* ≤ 1048576)	The maximum value of the divisor, *K*, is sample rate dependent.
Frequency Range	100 kHz to 400 MHz	—
Output Voltage	≥0.7 $V_{pk\text{-}pk}$ into 50 Ω	Typical.
Maximum Output Overload	3.3 $V_{pk\text{-}pk}$ from a 50 Ω source	—
Output Coupling	AC	—
VSWR	1.3:1 up to 2 GHz	Nominal.

PFI 0 and PFI 1 (Programmable Function Interface, Front Panel Connectors)

Specification	Value		Comments
Direction	Bidirectional		—
Frequency Range	DC to 200 MHz		—
As an Input (Trigger)			
Destinations	Start trigger, Script trigger		—
Input Range	0 V to 5 V		—
Input Protection Range	–2 V to +6.5 V		—
V_{IH}	1.8 V		—
V_{IL}	1.5 V		—
Input Impedance	10 kΩ, nominal		—
As an Output (Event)			
Sources	1. Sample clock divided by integer *K* (2 ≤ *K* ≤ 3, minimum) 2. Sample clock timebase divided by integer *M* (2 ≤ *M* ≤ 1048576) 3. Reference clock 4. Marker event 5. Data marker event 6. Exported Start trigger 7. Exported Script trigger 8. Ready for Start event 9. Started event 10. Done event		The maximum value of the Sample clock divisor, *K*, is sample rate dependent.
Output Impedance	Main Path	Direct Path	
	50 Ω, nominal	50 Ω (+4%, –0%)	
Maximum Output Overload	–2 V to +6.5 V		—
V_{OH}	Minimum: 2.4 V (open load), 1.3 V (50 Ω load)		Output drivers are +3.3 V TTL/CMOS compatible up to 200 MHz.
V_{OL}	Maximum: 0.4 V (open load), 0.2 V (50 Ω load)		
Rise/Fall Time	3 ns		Typical. Load of 10 pF.

Triggers and Events

Triggers

Specification	Value	Comments
Sources	1. PFI<0..1> (SMB front panel connectors) 2. PXI_Trig<0..7> (backplane connector) 3. Immediate (does not wait for a trigger). Default.	—
Types	1. Start trigger edge 2. Script trigger edge and level 3. Software trigger	—
Edge Detection	Rising, falling	—
Minimum Pulse Width	25 ns	Refer to the ts1 documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Devices»NI 5451»Triggering»Trigger Timing**.
Delay from Trigger to Analog Output with OSP Disabled	154 Sample clock timebase periods + 65 ns, nominal	Refer to the ts2 documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Devices»NI 5451»Triggering»Trigger Timing**.
Additional Delay with OSP Enabled	Varies with OSP configuration.	—
Trigger Exporting		
Exported Trigger Destinations	1. PFI<0..1> (SMB front panel connectors) 2. PXI_Trig<0..6> (backplane connector)	—
Exported Trigger Delay	50 ns, nominal	Refer to the t_{s3} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Devices»NI 5451»Triggering»Trigger Timing**.
Exported Trigger Pulse Width	>150 ns	Refer to the t_{s4} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Devices»NI 5451»Triggering»Trigger Timing**.

Events

Specification	Value		Comments
Destinations	1. PFI<0..1> (SMB front panel connectors) 2. PXI_Trig<0..6> (backplane connector)		—
Types	Marker<0..3>, Data Marker<0..1>, Ready for Start, Started, Done		There are two data markers per channel.
Quantum	Marker position must be placed at an integer multiple of two samples.		—
Width	Adjustable, minimum of 2 samples. Default is 150 ns.		Refer to the t_{m2} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Fundamentals»Waveform Fundamentals»Events»Marker Events**.
Skew	Destination	With Respect to Analog Output	Refer to the t_{m1} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Fundamentals»Waveform Fundamentals»Events»Marker Events**.
	PFI<0..1>	±3 Sample clock periods	
	PXI_Trig<0..6>	±6 Sample clock periods	

Waveform Generation Capabilities

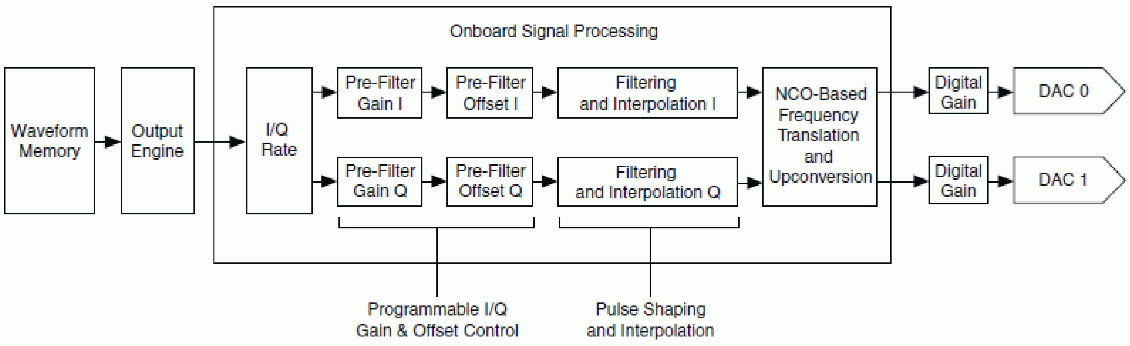
Specification	Value			Comments
Memory Usage	The NI 5451 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.			For more information, refer to the *NI Signal Generators Help* by navigating to **NI Signal Generators Help» Programming» Reference» NI-TClk Synchronization Help** .
Onboard	128 MB option: 134,217,728 bytes	512 MB option: 536,870,912 bytes	2 GB option: 2,147,483,648	Memory is shared between both channels.

Specification	Value				Comments
Memory Size			bytes		
Loop Count	1 to 16,777,215 Burst trigger: Unlimited				—
Quantum	Waveform size must be an integer multiple of two samples.				—
Output Modes					
Arbitrary Waveform mode	A single waveform is selected from the set of waveforms stored in onboard memory and generated.				—
Script mode	A script allows you to link and loop multiple waveforms in complex combinations. A script is a series of instructions that indicates how waveforms saved in the onboard memory should be sent to the device. The script can specify the order in which the waveforms are generated, the number of times they are generated, and the triggers and markers associated with the generation.				—
Output Modes (Continued)					
Arbitrary Sequence mode	A sequence directs the NI 5451 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.				—
Minimum Waveform Size (Samples)					
Trigger Mode	Number of Channels	Arbitrary Waveform Mode	Arbitrary Sequence Mode >180 MS/s	Arbitrary Sequence Mode ≤180MS/s	The minimum waveform size is sample rate dependent. Measured using a 200 MHz trigger.
Single	1	4	2	2	
	2	4	4	4	
Continuous	1	142	140	58	
	2	284	280	116	
Stepped	1	210	154	54	
	2	420	308	108	
Burst	1	142	1,134	476	
	2	284	2,312	952	
Memory Limits (bytes)					
	Number of Channels	128 MB	512 MB	2 GB	
Arbitrary Waveform Mode, Maximum Waveform Memory	1	67,108,352	268,434,944	1,073,741,312	All trigger modes except where noted.
	2	33,553,920	134,217,216	536,870,400	
Arbitrary Sequence Mode, Maximum Waveform Memory	1	67,108,352	268,434,944	1,073,741,312	Condition: One or two segments in a sequence.
	2	33,553,920	134,217,216	536,870,400	
Arbitrary Sequence Mode, Maximum Waveforms	1	1,048,575	4,194,303	16,777,217	Condition: One or two segments in a sequence.
	2	524,287	2,097,151	8,388,607	
Arbitrary Sequence Mode, Maximum Segments in a Sequence	1	8,388,597	33,554,421	134,217,717	Condition: Waveform size is <4,000 samples.
	2	4,194,293	16,777,205	67,108,853	
Waveform Play Times					
Maximum Play Time, Sample Rate	Number of Channels	128 MB	512 MB	2 GB	Single Trigger mode. Play times can be significantly extended by using Continuous, Stepped, or Burst Trigger modes.
400 MS/s	1	0.17 seconds	0.67 seconds	2.68 seconds	
	2	0.084 seconds	0.34 seconds	1.34 seconds	
25 MS/s	1	2.68 seconds	10.74 seconds	42.95 seconds	
	2	1.34 seconds	5.37 seconds	21.47 seconds	
100 kS/s	1	11 minutes 11 seconds	44 minutes 44 seconds	2 hours 58 minutes 57 seconds	

Specification	Value				Comments
	2	5 minutes 35 seconds	22 minutes 22 seconds	1 hour 29 minutes 29 seconds	

Onboard Signal Processing

Onboard Signal Processing Block Diagram



Specification	Value			Comments
I/Q Rate				
OSP Interpolation Range	2, 4, 8, 12, 16, 20 24 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16) 16,384 to 32,768 (multiples of 32)			—
I/Q Rate	(Sample clock rate) ÷ (OSP interpolation)			Example: For a Sample clock rate of 400 MS/s, I/Q rate range = 12.2 kS/s to 200 MS/s.
Data Processing Modes*	1. Real (I path only) 2. Complex (I/Q)			—
OSP Modes†	1. IF 2. Baseband			—
Maximum Bandwidth‡	0.8 × I/Q rate			—

* Data Processing Mode describes the OSP engine data source. The data can be a single stream of real data (**Real**), or separate streams of real and imaginary data (**Complex**).

† OSP Mode describes the signal processing function performed on the data after interpolation. In IF Mode, I and Q data streams are quadrature upconverted to an intermediate frequency in a single output stream (to DAC 0/I). In Baseband Mode, frequency shifting can be applied to the I and Q data streams before they go into separate output streams (DAC 0/I and DAC 1/Q).

‡ When using an external I/Q modulator, RF Bandwidth = 0.8 × I/Q rate.

Note: For more information about frequency translation and upconversion, refer to the *NI Signal Generators Help* and navigate to **NI Signal Generators Help»Devices»NI 5451»Onboard Signal Processing (OSP)»Numerically Controlled Oscillator (NCO)**.

Specification	Value			Comments
Prefilter Gain and Offset				
Prefilter Gain and Offset Resolution	21 bits			—
Prefilter Gain Range	–16.0 to +16.0 (|Values| < 1 attenuate user data)			Unitless.
Prefilter Offset Range	–1.0 to +1.0			Applied after Prefilter gain.
Prefilter Output	(User data × Prefilter gain) + Prefilter offset			Overflows occur when |Output| > 1.
Finite Impulse Response (FIR) Filtering				
Filter Types	Parameter	Minimum	Maximum	
Flat	Passband	0.4	0.4	Lowpass filter that minimizes ripple to: I/Q rate × Passband.
Raised Cosine	Alpha	0.1	0.4	When using pulse shaping, these filters require an OSP interpolation factor of 24 or greater.
Root Raised Cosine	Alpha	0.1	0.4	
Numerically Controlled Oscillator (NCO)				
Maximum Frequency	0.4 × sample rate			—
Frequency Resolution	Sample rate/2^{48}			Example: 1.42 μHz with a sample rate of 400 MS/s.
Tuning Speed	250 μs			Software- and system-dependent.

Specification	Value	Comments
Digital Performance		
Maximum NCO Spur	<–90 dBc	Full-scale output.
Interpolating Flat Filter Passband Ripple	<0.1 dB	Passband from 0 to (0.4 × I/Q Rate). Ripple is dependent upon the interpolation rate.
Interpolating Flat Filter Out-of-Band Suppression	>80 dB	Stopband suppression from (0.6 × I/Q rate).

Specification				Value						Comments
IF Modulation Performance (Nominal)										
QAM Order	Symbol Rate (MS/s)	Alpha	Bandwidth	EVM (%)			MER (dB)			—
				40 MHz IF	70 MHz IF	110 MHz IF	40 MHz IF	70 MHz IF	110 MHz IF	
M = 4	0.16	0.25	200 kHz	0.2	0.2	0.2	57	57	56	
	0.80	0.25	1.00 MHz	0.2	0.2	0.2	57	56	55	
	4.09	0.22	4.98 MHz	0.2	0.3	0.2	57	52	55	
M = 16	17.6*	0.25	22.0 MHz	0.3	0.5	0.4	51	45	49	
	32.0*	0.25	40.0 MHz	0.6	—	0.6	42	—	43	
M = 64	5.36	0.15	6.16 MHz	0.2	0.3	0.2	54	51	53	
	6.95	0.15	7.99 MHz	0.3	0.3	0.3	52	51	50	
	25.0	0.15	28.75 MHz	0.4	0.6	0.4	46	43	46	
M = 256	6.95	0.15	7.99 MHz	0.3	0.3	0.4	52	51	49	

Notes: Single-Ended Main Path, –1 dBFS, Flatness Correction Enabled, Onboard Sample Clock without Reference.

Number of Symbols = 1024

All measurements were made using the NI PXIe-5622, not phase-locked to the NI 5451, equalization enabled, 40 MHz IF and 110 MHz IF using internal clocking, 70 MHz IF using external clocking at 100 MHz.

* Fractional interpolation performed on data before generation. For more information, refer to the *NI Signal Generators Help* and navigate to **NI Signal Generators Help»Devices»NI 5451»Theory of Operation»Onboard Signal Processing (OSP)»Baseband Interpolation Considerations**.

Calibration

Specification	Value	Comments
External Calibration	The external calibration calibrates the ADC voltage reference and passband flatness. Appropriate constants are stored in nonvolatile memory.	—
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. Onboard channel alignment circuitry is used to calibrate the skew between channels. The self-calibration is initiated by the user through the software and takes approximately 60 seconds to complete. Appropriate constants are stored in nonvolatile memory.	—
Calibration Interval	Specifications valid within 1 year of external calibration	—
Warm-up Time	15 minutes	—

Power

Specification	Typical	Maximum	Comments
+3.3 VDC	1.9 A	2.0 A	—
+12 VDC	2.6 A	2.9 A	—
Total Power	37.5 W	41.4 W	—

Software

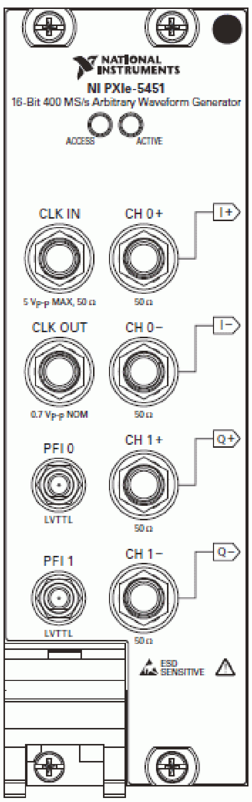
Specification	Value	Comments
Driver Software	NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5451. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments:	—

Specification	Value	Comments
	LabVIEW ▪ LabWindows™/CVI™ ▪ Measurement Studio ▪ Microsoft Visual C++ .NET ▪ Microsoft Visual C/C++ ▪ Microsoft Visual Basic	
Interactive Control and Configuration Software	The FGEN Soft Front Panel supports interactive control of the NI 5451. The FGEN Soft Front Panel is included on the NI-FGEN driver CDs. Measurement & Automation Explorer (MAX) provides interactive configuration and test tools for the NI 5451. MAX is also included on the NI-FGEN CDs. You can use the NI 5451 with NI SignalExpress.	—

Physical

Hardware Front Panel

NI 5451 Front Panel



Specification	Value	Comments
Dimensions	3U, Two Slot, PXI Express module 21.6 cm × 4.0 cm × 13.0 cm (8.5 in. × 1.6 in. × 5.1 in.)	—
Weight	550 g (19.4 oz)	—

Front Panel Connectors

Label	Function(s)	Connector Type	—
CH 0+/I+	Differential and Single-Ended Analog Output	SMA	
CH 0–/I–	Differential Analog Output	SMA	
CH 1+/Q+	Differential and Single-Ended Analog Output	SMA	
CH 1–/Q–	Differential Analog Output	SMA	
CLK IN	Sample clock, Sample clock timebase, and Reference clock input.	SMA	
CLK OUT	Sample clock, Sample clock timebase, and Reference clock output.	SMA	
PFI 0	Marker output, trigger input, Sample clock output, exported trigger output.	SMB	

Specification	Value		Comments
PFI 1	Marker output, trigger input, Sample clock output, exported trigger output.	SMB	
Front Panel LED Indicators			
Label	Function		For more information about the front panel LEDs, refer to the *NI Signal Generators Help*.
ACCESS	The ACCESS LED indicates the status of the PXI Express bus and the interface from the NI 5451 to the controller.		
ACTIVE	The ACTIVE LED indicates the status of the onboard generation hardware of the NI 5451.		

NI PXIe-5451 Environment

Note To ensure that the NI PXIe-5451 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5451 kit. The NI PXIe-5451 is intended for indoor use only.

Specifications	Value	Comments
Operating Temperature	0 ºC to +55 ºC in all NI PXI Express chassis: Meets IEC 60068-2-1 and IEC 60068-2-2. **Note**: Refer to *KnowledgeBase 4AEB2ML1* at ni.com for more information about maximizing PXI Express data transfer rates when operating at ambient temperatures below 10 ºC.	—
Storage Temperature	–25 ºC to +85 ºC. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC 60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC 60068-2-56.	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	Spectral and jitter specifications could degrade.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 Hz to 500 Hz, 0.31 g_{rms}. Meets IEC 60068-2-64.	Spectral and jitter specifications could degrade.
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 meter maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—

Safety Standards

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations and certifications, refer to the *Online Product Certification* section.

Note For EMC compliance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification
To obtain product certifications and the DoC for this product, visit ni.com/certification, search by module number or product line, and click the appropriate link in the Certification column.

Environmental Management
NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers. For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.
Waste Electrical and Electronic Equipment (WEEE)
EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit ni.com/environment/weee.htm. **电子信息产品污染控制管理办法 （中国 RoHS）** **中国客户** National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

[1] **Note** For all configurations, both CH± terminals are terminated to ground through loads of the same value.

The voltage output levels are set in the software and are based on a 50 Ω per line load termination to ground (the default), or based on the user-specified load resistance. Common-mode offset assumes outputs are terminated into equal loads to ground. Refer to the *NI Signal Generators Help* and navigate to **NI Signal Generators Help»Devices»NI 5451»Front Panel Connectors»Differential and Single-Ended Channel Connectors** for more information.
Gain values in NI-FGEN correspond to V_{pk} which is half the amplitude in $V_{pk\text{-}pk}$.

[2] Combinations of waveform data, offset, and gain that exceed a single-ended output of 3.2 V_{pk} may result in waveform clipping.

[3] Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, you can use waveforms less than the full scale of the DAC or you can use digital gain. Additional offset can be added using waveform data.

[4] **Note** For the Main path, V_{CM} +V_{DIFF}/2 and V_{CM} – V_{DIFF}/2 shall be between ±2 V, into an open load.

[5] Additional offset can be added using waveform data.

[6] For DC accuracy, *single-ended output range* is defined as 2x the gain setting into high impedance. For example, the accuracy of a DC signal with a gain of 2.5, a load impedance of 1 GΩ, and a single-ended output range of 5 V is calculated by the following equation:

Gain Error within ±5 °C of Self-Cal temperature: ±(0.4% × 5 V + 0.5 mV) = ±20.5 mV

Gain Error at +10 °C of Self-Cal temperature: ±20.5 mV – 0.05% × 5 °C × (5 V) = +8/–33 mV

Offset Error: [2 V offset at gain=2.5] ±(0.15% × (2 V) + 0.04% × (5 V) + 1.25 mV) = ±6.25 mV

[7] For DC accuracy, *differential output range* is defined as 2x the gain setting into high impedance. For example, the accuracy of a DC signal with a gain of 5, a load impedance of 1 GΩ, and a differential output range of 10 V is calculated by the following equation:

Gain Error within ±5 °C of Self-Cal temperature: ±(0.6% × 10 V + 1 mV) = ±61 mV

Gain Error at + 10 °C of Self-Cal temperature: ±61 mV – 0.05% × 5 °C × (10 V) = +36/–86 mV

Differential Offset Error: [Requested differential offset = 1 V at gain = 5] ±(0.3% × (1 V) + 0.01% × (10 V) + 2 mV) = ±6 mV

[8] For DC accuracy, *differential output range* is defined as 2x the gain setting into high impedance. For example, the accuracy of a DC signal with a gain of 1, a load impedance of 1 GΩ, and a differential output range of 2 V is calculated by the following equation:

Gain Error within ±5 °C of Self-Cal temperature: ±0.2% × (2 V) = ±4 mV

Gain Error at + 10 °C of Self-Cal temperature: 4 mV + 0.03% × 5 × (2 V) = +7/–1 mV

[9] Direct path common mode offset is minimized through active circuitry. Applying an external nonzero common-mode offset to the output terminal is not recommended; however the common-mode circuitry can sink or source up to 5 mA of common-mode bias current. Terminate both output terminals to ground through the same impedance. If the output terminals are not terminated to ground, the maximum termination voltage is 250 mV through 50 Ω.

[10] The voltage output levels are set in the software and are based on a 50 Ω per line load termination to ground (the default), or based on the user-specified load resistance. Common-mode offset assumes outputs are terminated into equal loads to ground. Refer to the *NI Signal Generators Help* and navigate to **NI Signal Generators Help»Devices»NI 5451»Front Panel Connectors»Differential and Single-Ended Channel Connectors** for more information.

[11] Flatness correction is not supported if the filter is disabled.

[12] Frequency ranges with flatness correction enabled are sample rate dependent.

[13] Valid for use without OSP enabled or when interpolating by 2x with OSP enabled. For all larger interpolation rates using OSP, the OSP filters may introduce extra ripple. Refer to the *Interpolating Flat Filter Passband Ripple* specification in the *Onboard Signal Processing* section for more information about OSP filter ripple.

[14] Value = Min (0.3375 × Sample Rate, 60 MHz)

[15] Value = 0.3375 × Sample Rate

[16] Value = Min (0.3 × Sample Rate, 60 MHz)

[17] Value = 0.3 × Sample Rate

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