300-MHz Quadrature Modulator

Description

The IC U2793B-AFS is a 300-MHz quadrature modulator that uses TEMIC Semiconductors' advanced UHF process. It features low current consumption, single-ended RF ports and adjustment-free application, which makes the device suitable for all digital radio systems, e.g., GSM, PCN, JDC and WLAN. As an option, output level and spurious products are adjustable at Pins 19 and 20. In conjunction with TEMIC Semiconductors' U2795B mixer, an up converter up to 2 GHz can be realized.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Supply voltage: 5 V (typical)
- Low power consumption: 15 mA / 5 V (typical at 0 dBm output level
- Output level and spurious products adjustable (optional)
- Excellent sideband suppression by means of duty cycle regeneration of the LO input signal
- Phase-control loop for precise 90° phase shifting
- Power-down mode
- Low LO input level: –15 dBm (typical)
- 50-Ω single-ended LO and RF port
- LO frequency range of 30 MHz to 300 MHz

Benefits

- Extended talk time due to increased battery life
- Few external components results in cost and board space saving
- Adjustment free hence saves time
- Modular system for different applications by adding U2795B reduces the costs

Block Diagram

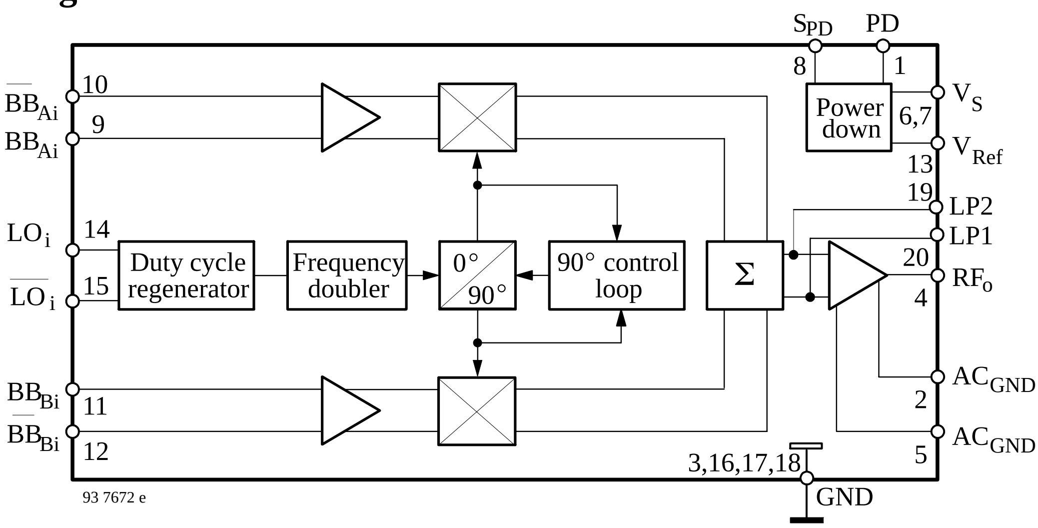


Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U2793B-AFS	SSO20	Tube
U2793B-AFSG3	SSO20	Taped and reeled

Pin Description

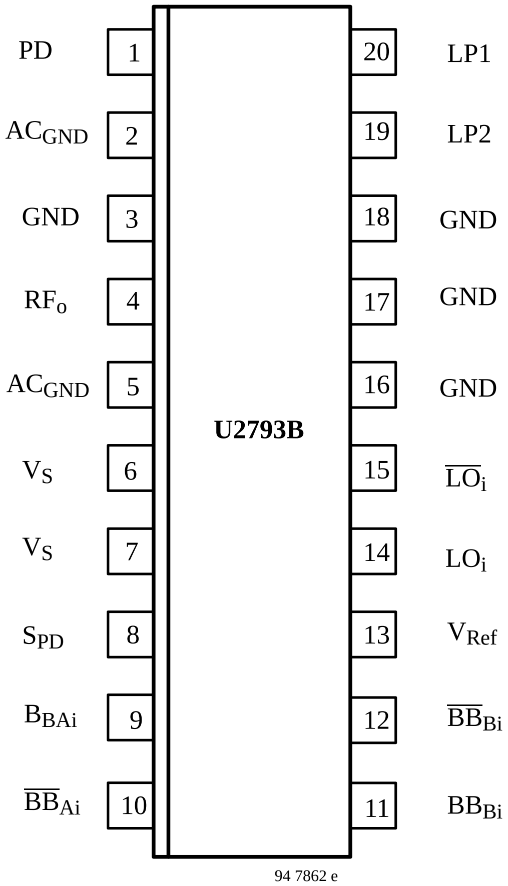


Figure 2. Pinning SSO20

Pin	Symbol	Function
1	PD	Power down port
2	AC_{GND}	AC ground
3	GND	Ground
4	RF_o	RF output
5	AC_{GND}	AC ground
6	V_S	Supply voltage
7	V_S	Supply voltage
8	S_{PD}	Settling time power down
9	BB_{Ai}	Baseband input A
10	$\overline{BB}_{Ai}$	Baseband input A inverse
11	BB_{Bi}	Baseband input B
12	$\overline{BB}_{Bi}$	Baseband input B inverse
13	V_{Ref}	Reference voltage (2.5 V)
14	LO_i	Input LO
15	$\overline{LO}_i$	Input LO inverse, typically grounded
16	GND	Ground
17	GND	Ground
18	GND	Ground
19	LP2	Output low pass and power control
20	LP1	Output low pass and power control

Absolute Maximum Ratings

Parameters		Symbol	Value	Unit
Supply voltage	Pins 6 and 7	V_S	6	V
Input voltage	Pins 9, 10, 11, 12, 14 and 15	V_i	0 to V_S	V
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	–40 to +125	°C

Operating Range

Parameters		Symbol	Value	Unit
Supply voltage	Pins 6 and 7	V_S	4.5 to 5.5	V
Ambient temperature range		T_{amb}	–40 to +85	°C

Thermal Resistance

Parameters		Symbol	Value	Unit
Junction ambient	SSO20	R_{thja}	140	K/W

Electrical Characteristics

Test conditions (unless otherwise specified); V_S = 5 V, T_{amb} = 25°C, referred to test circuit.
System impedance Zo = 50 Ω, f_{LO} = 150 MHz, P_{LO} = –15 dBm, V_{BBi} = 1.0 V_{pp}, differential

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit
Supply-voltage range	Pins 6 and 7	V_S	4.5	5	5.5	V
Supply current	Pins 6 and 7	I_S		15		mA
Baseband inputs	**Pin 9–10, 11–12**					
Input-voltage range (differential)		V_{BBi}		1000	1500	mVpp
Input impedance		Z_{BBi}		30		kΩ
Input-frequency range		f_{BBi}	0		50	MHz
LO input	**Pins 14 and 15**					
Frequency range		f_{LOi}	30		300	MHz
Input level [1]		P_{LOi}		–15	–5	dBm
Input impedance		Z_{iLO}		[2)]		Ω
Voltage standing wave ratio		$VSWR_{LO}$		3.5		
Duty-cycle range		DCR_{LO}	0.4		0.6	
RF output	**Pin 4**					
Output level	f_{LO} = 150 MHz, V_{BBi} = 1 V_{pp}, differential f_{LO} = 50 MHz, V_{BBi} = 0.3 V_{pp}, differential	P_{RFo}	–3	–1 0		dBm
LO suppression	P_{LO} = –20 dBm	LO_{RFo}	32	45		dB
Voltage standing wave ratio		$VSWR_{RF}$		1.4	2	
Sideband suppression [3]		SBS_{RFo}	35	45		dB
Phase error [4]		Pe		<1		deg
Amplitude error		Ae		< ± 0.25		dB
Noise floor	V_{BBi} = 2 V, $V_{\overline{BBi}}$ = 3 V V_{BBi} = $V_{\overline{BBi}}$ = 2.5 V	N_{FL}		–137 –143		dBm/Hz
Power-down mode						
Supply current	V_{PD} ≤ 0.5 V, Pins 6, 7, V_{PD} = 1 V	I_{PD}		 10	1	µA
Settling time	Pins 1 to 4 C_{SPD} = 100 pF C_{LO} = 100 pF, C_{RFo} = 1 nF	t_{SPD}		10		µs
Switching voltage	**Pin 1**					
Power on		V_{PDon}	4			V
Power down		V_{PDdown}			1	V
Reference voltage	**Pin 13**					
Voltage range		V_{Ref}		2.5 ± 5 %		V
Output impedance		Zo_{Ref}		30		Ω

Note:
1 Required LO level is a function of the LO frequency.
2 The LO input impedance is consisting of a 50 Ω resistor in series with a 15 pF capacitor
3 With the Pins 19 and 20 spurious performance especially for low frequency application can be improved by adding a chip capacitor between LP1 and LP2. In conjunction with a parallel resistor the output level can be adjusted to the following mixer stage without degration of LO suppression and noise performance which would decrease if the I/Q input level is reduced.
4 For T_{amb} = –40 to +85°C and V_S = 4.5 to 5.5 V

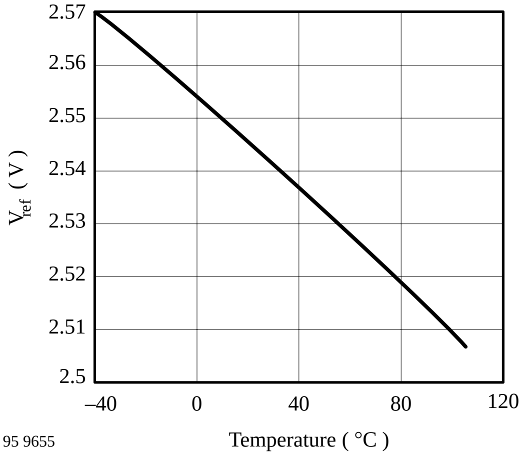


Figure 3. Reference voltage versus T_{amb}

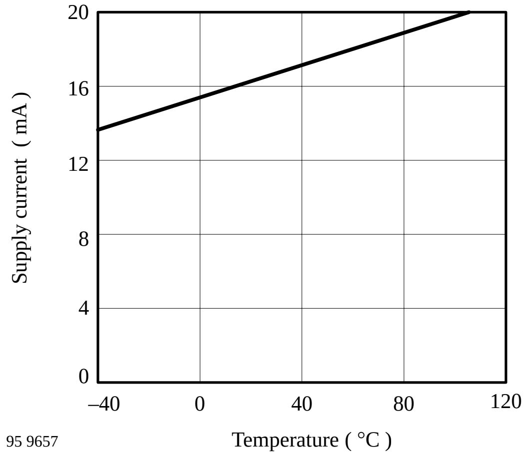


Figure 5. Supply current versus T_{amb}

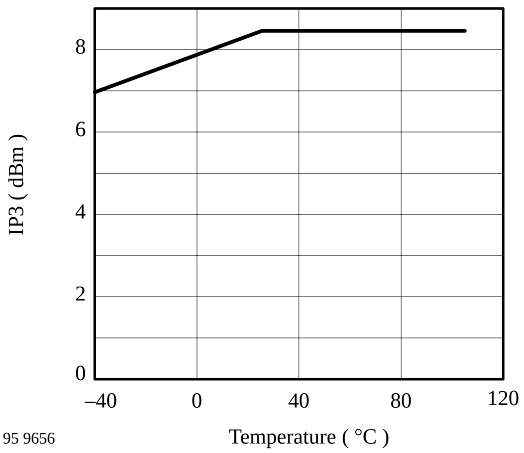


Figure 4. OIP3 versus T_{amb}, LO = 150 MHz, level –10 dBm

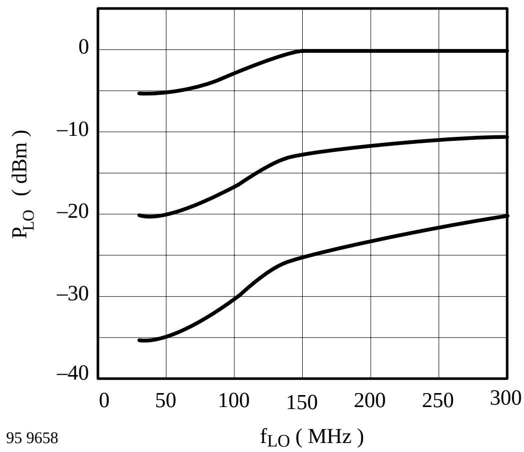


Figure 6. Recommended LO power range versus LO frequency at T_{amb} = 25°C

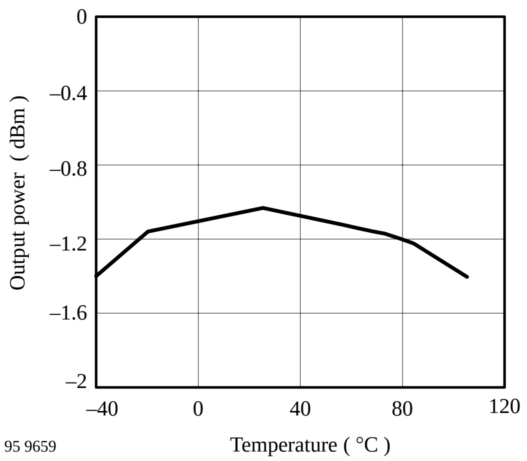


Figure 7. Output power versus T_{amb}

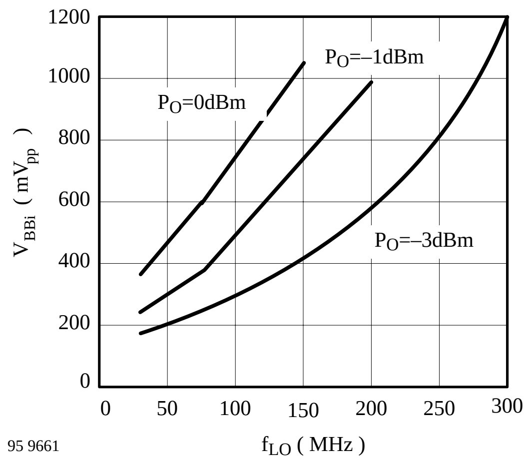


Figure 9. Typical required V_{BBi} input signal (differential) versus LO frequency for P_O = 1 dBm and P_O = –3 dBm

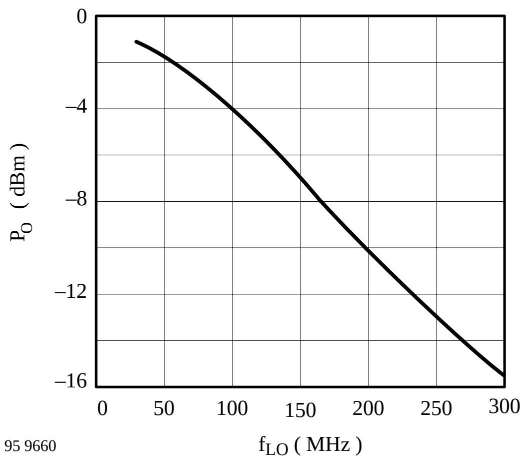


Figure 8. Typical output power vs. LO frequency at T_{amb} = 25°C, V_{BBi} = 250 mV (differential)

Evaluation Board Circuitry

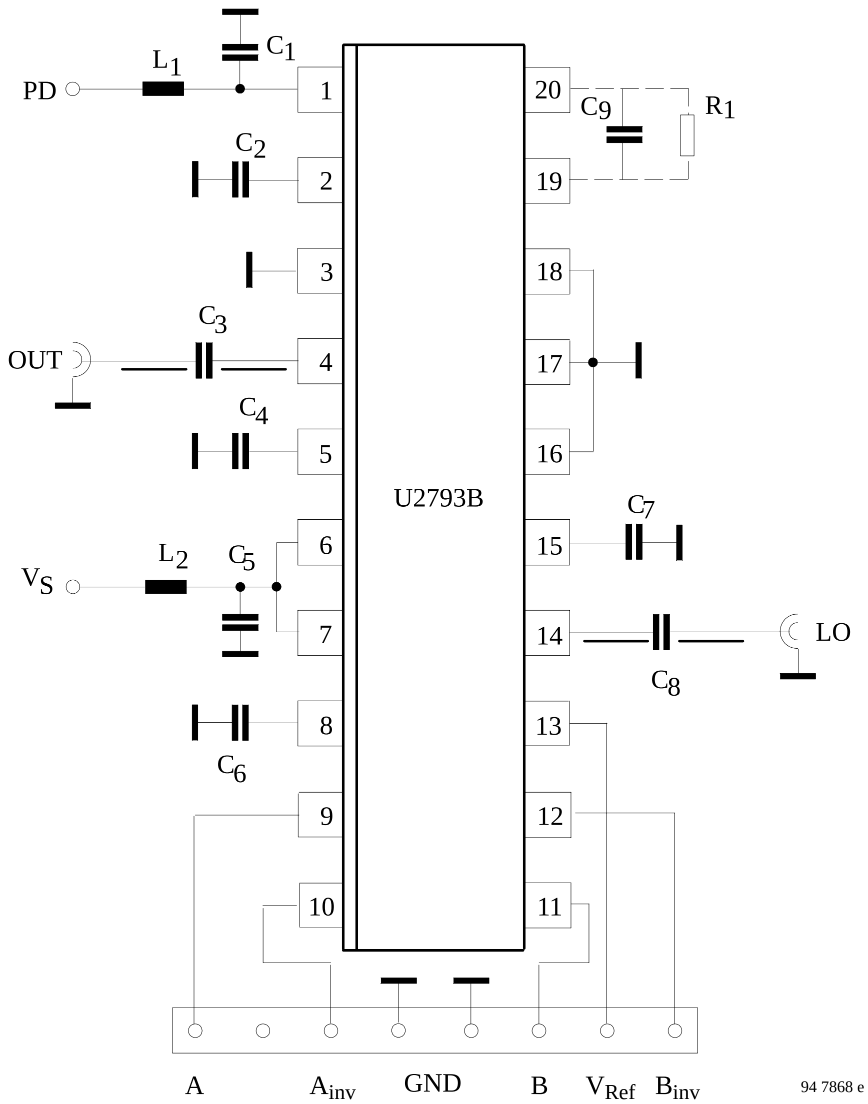


Figure 10. Evaluation board circuitry

Part list	
C1, C2, C3, C4, C6	1 nF
C7, C8	100 pF
C5	100 nF
C9, R1	1 to 10 pF
L1, L2	PCB Inductor
═══	50-Ω Microstrip
– – – –	optional

The above listed components result in a PD settling time of < 20 µs. Use of other component values will require consideration for time requirements in burst-mode applications.

PCB Layout Evaluation Board

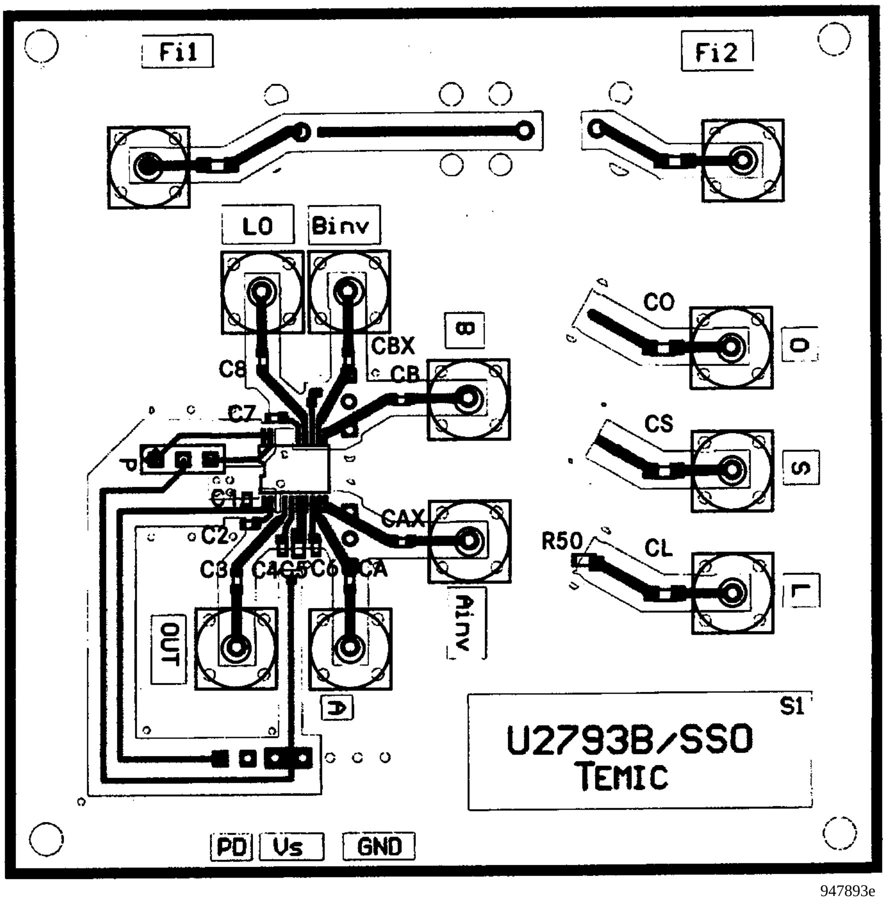


Figure 11. PCB layout

Application Circuit

Bias network for AC-coupled baseband inputs (V_{BA}, V_{BB}).
R1 = 2.5 kΩ, R2 ≦ 10 kΩ for ≥ 35 dB LO suppression which is in reference to < 2 mV input offset.

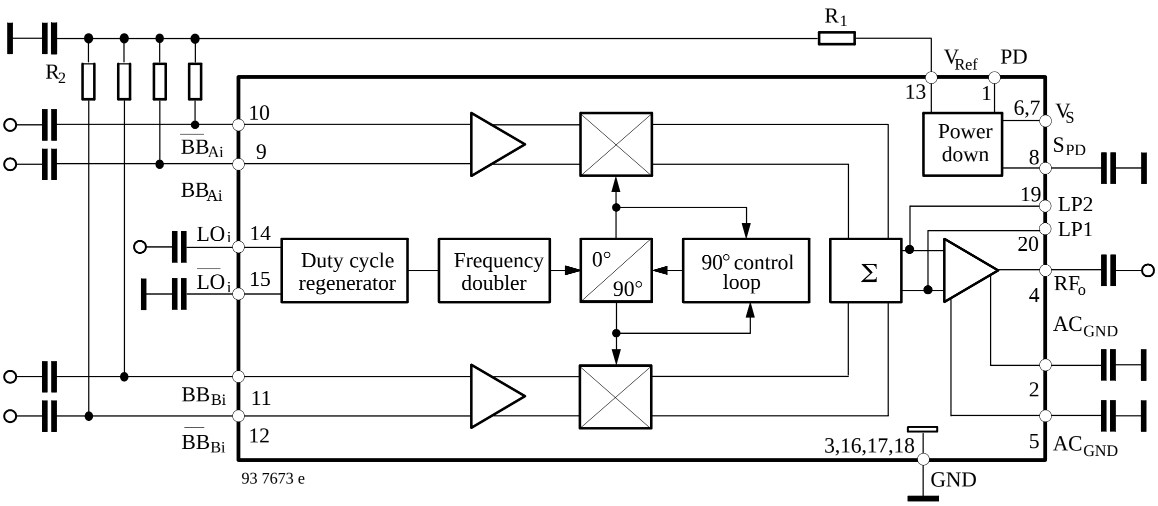


Figure 12. Application circuit with AC-coupled baseband inputs

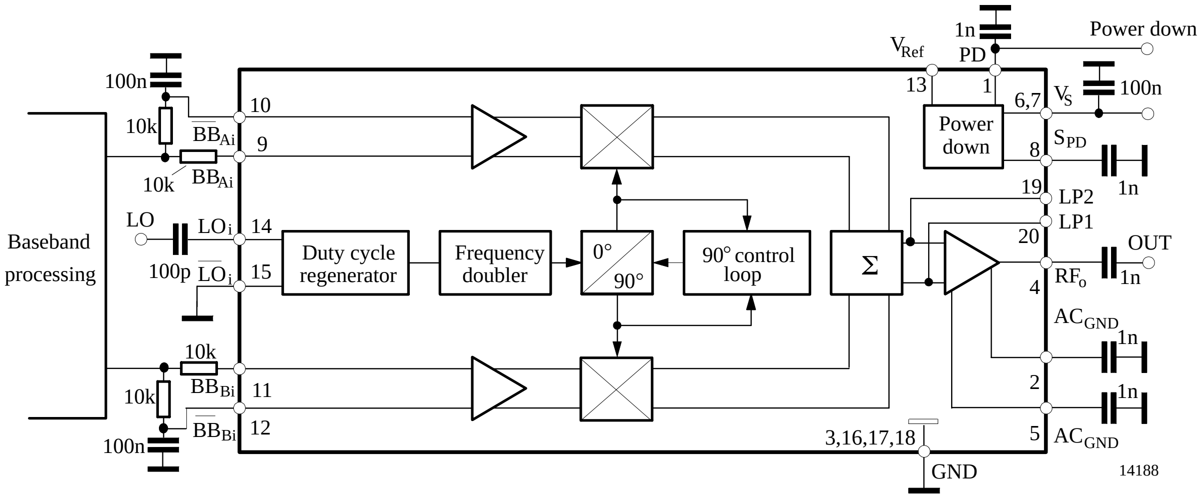
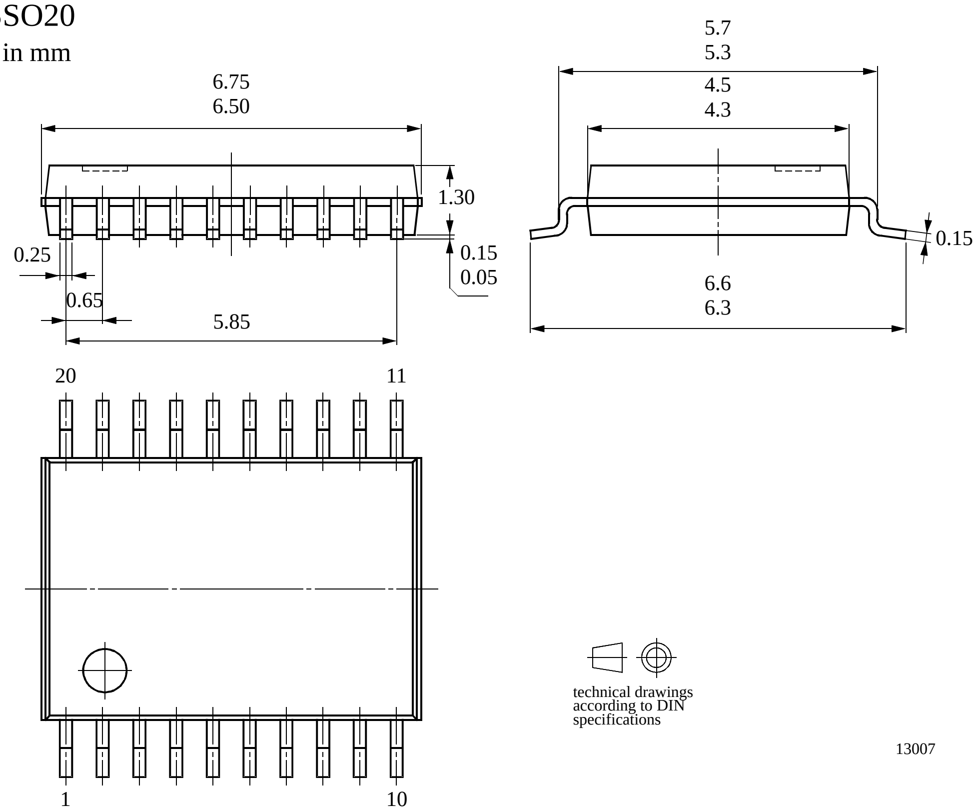


Figure 13. Application circuit with DC-coupled baseband inputs

Package Information

Package SSO20

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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