

S-Band Radar Transistor

The high power pulsed radar transistor device part number IB3134M25 is designed for S-Band radar systems operating over the instantaneous bandwidth of 3.1-3.4 GHz. While operating in class C mode this common base device supplies a minimum of 25 watts of peak pulse power under the conditions of 300µs pulse width and 10% duty cycle. All devices are 100% screened for large signal RF parameters, including power gain compression. Excellent spectral stability into output mismatch over a broad input power range make it ideal for use in reliable high power solid state transmitters.



Silicon Bipolar
– Ultra-high f_T

Class C Operation
– High Efficiency

Common Base Configuration
– Single Power Supply

Gold Metal
– Maximum Reliability

Emitter Ballasting
– Optimum Thermal Distribution

Internal Impedance Matching
– Ease of Use
– Ultra-low Loss Design

BeO Package
– Unmatched Thermal Reliability

RF Test Fixture
– Broadband
– Matched to 50Ω
– Long-term Correlation
– 100% Device RF Screening
– No External Tuning Allowed

Insertion Phase Marking
– 5° Increment Marking

TYPICAL DATA TYPICAL DATA TYPICAL DATA TYPICAL DATA

Device	Test Seq Name	Freq (GHz)	PW (us)	Duty (%)	Vcc (V)	P _{IN} (W)	IRL (dB)	P _{OUT} (W)	G _P (dB)	OPC (dB)	OPF (dB)	I _c (A)	N _c (%)	Droop (dB)	VSWR 1.5:1	VSWR LMT 2:1
50032502-6	OPC	3.100	300	10	32.0	2.9	--	33.4	--	0.13	--	--	--	--	--	--
	Nominal	3.100	300	10	32.0	2.6	-19	32.4	10.95	--	0.35	2.19	46	-0.26	S	P
	OPC	3.250	300	10	32.0	2.9	--	31.4	--	0.05	--	--	--	--	--	--
	Nominal	3.250	300	10	32.0	2.6	-24	31.0	10.77	--	--	2.18	45	-0.66	S	P
	OPC	3.400	300	10	32.0	2.9	--	31.9	--	0.29	--	--	--	--	--	--
	Nominal	3.400	300	10	32.0	2.6	-23	29.9	10.60	--	--	1.90	49	-0.18	S	P

MAXIMUM RATINGS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Collector-Emitter Voltage	V_{CES}	--	70	V	$V_{BE}=0V$.
BD	Emitter-Base Voltage	V_{EBO}	--	2.5	V	--
BD	Storage Temperature Range	T_{STG}	-55	+150	°C	--
BD	Operating Junction Temperature Range	T_J	-55	+200	°C	--
Note	Screen 'BD' = parameter qualified By Design.					

THERMAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
BD	Thermal Resistance	$R_{TH(JC)}$	--	1.45	°C/W	$V_{CC}=V1$, $PW=PW1$, $DF=DF1$, $T_F=25\pm5^\circ C$, $P_{OUT}=25W$, $N_C=40\%$, $F=F3$.
Note	Screen 'BD' = parameter qualified By Design.					

PROCESSING SPECIFICATIONS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	DC Wafer Probe	--	--	--	--	Per Integra specification.
Q1	Wafer DC and RF Qualification	--	--	--	--	Per Integra specification.
LM	Wire Bond Strength	--	--	--	--	Line monitor per Integra specification.
100%	Pre-cap visual inspection	--	--	--	--	Per Integra specification.
100%	Gross leak test	--	--	--	--	MIL-STD-750D, Method 1071.6, Test Condition C.
Note	Screen 'Q1' = parameter is qualified by assembly and test of 3 pieces minimum per wafer.					
Note	Screen 'LM' = parameter is qualified by assembly line monitor.					

DC ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Collector-Emitter Breakdown Voltage	BV_{CES}	70	--	V	$I_C=20mA$, $V_{BE}=0V$, $T_F=25\pm5^\circ C$.
100%	Zero Base Voltage Collector Leakage Current	I_{CES}	--	1.5	mA	$V_{CE}=30V$, $V_{BE}=0V$, $T_F=25\pm5^\circ C$.
100%	DC Current Gain	H_{FE}	10	150	--	$V_{CE}=5V$, $I_C=0.1A$, $T_F=25\pm5^\circ C$.

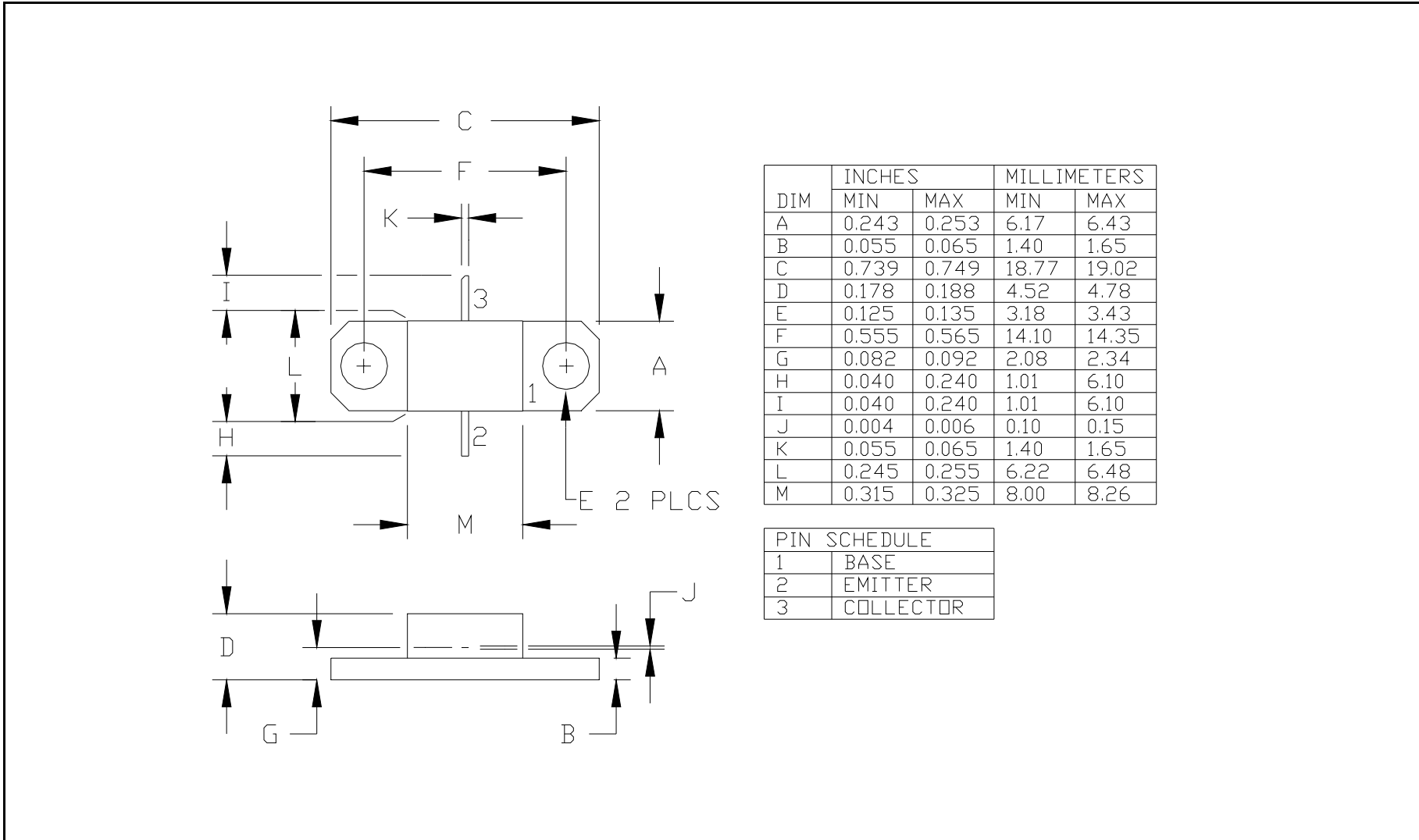
RF ELECTRICAL CHARACTERISTICS

Screen	Parameter	Symbol	Min	Max	Units	Test Conditions
100%	Input Return Loss	IRL	10	--	dB	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Output Power 1	P_{O1}	25	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Output Power 2	P_{O2}	25	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Output Power 3	P_{O3}	25	--	W	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Collector Efficiency ($P_O/I_C/V_{CC}$) 1	N_{C1}	40	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, F=F1.$
100%	Collector Efficiency ($P_O/I_C/V_{CC}$) 2	N_{C2}	40	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2.$
100%	Collector Efficiency ($P_O/I_C/V_{CC}$) 3	N_{C3}	40	--	%	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN3}, F=F3.$
100%	Pulse Amplitude Droop	D	--	0.5	Db	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$
100%	Output Power Flatness = $10 \cdot \text{LOG}(P_{OMAX}/P_{OMIN})$	OPF	--	1.00	dB	Calculate from P_O at each frequency F.
100%	Output Power Compression = $10 \cdot \text{LOG}(P_{OC}/P_O)$	OPC	-0.02	+0.52	dB	P_{OC} measured with P_{IN} increased by 0.5dB at $F=F1, F2, F3.$
100%	Delta Insertion Phase Variation	d-IP	-30	+30	Deg	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN2}, F=F2, F3.$ Mark in 5° increments.
100%	Stability into 1.5:1 VSWR	VSWR-S	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$ Rotate 1.5:1 output VSWR through 360° phase. No oscillatory or pulse break-up characteristics allowed on detected output pulse. All non-harmonically related signals must be at least -65 dBc.
100%	2:1 Load Mismatch Tolerance	LMT	--	--	--	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$ Rotate 2:1 output VSWR through 360° phase. Post test $P_O = \text{Pre test } P_O \pm 0.20\text{dB}.$
BD	Pulse Risetime	RT	--	150	ns	$V_{CC}=V1, PW=PW1, DF=DF1, T_F=25\pm5^\circ C, P_{IN}=P_{IN1}, P_{IN2}, P_{IN3}, F=F1, F2, F3.$ Measure between 10% and 90% detected power points.
Note	$V1 = 32V; PW1 = 300\mu s; DF1 = 10\%; P_{IN1} = P_{IN2} = P_{IN3} = 2.6W; F1 = 3.10 \text{ GHz}, F2 = 3.25 \text{ GHz}, F3 = 3.40 \text{ GHz}.$					
Note	$T_F = \text{Device flange temperature}.$					
Note	Parts are binned and marked in 5 degree increments for Insertion Phase IP : ITI-1, -2, -3, -4, -5, -6, -7, -8, -9, -10, -11, -12.					
Note	Screen 'BD' = parameter qualified By Design.					

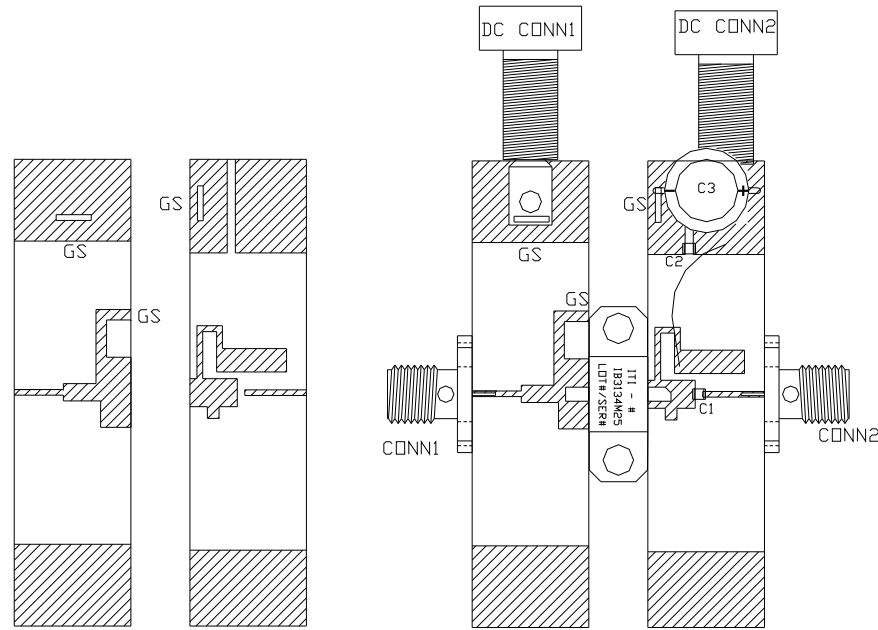
BROADBAND RF TEST FIXTURE IMPEDANCE CHARACTERISTICS

Frequency (GHz)	$Z_{IF} (\Omega)$	$Z_{OF} (\Omega)$
3.10	5.1 – j8.0	7.9 – j9.3
3.25	4.7 – j6.9	6.9 – j7.7
3.40	4.9 – j6.9	6.8 – j7.5
Impedance Definition		

PACKAGE DIMENSIONAL OUTLINE DRAWING



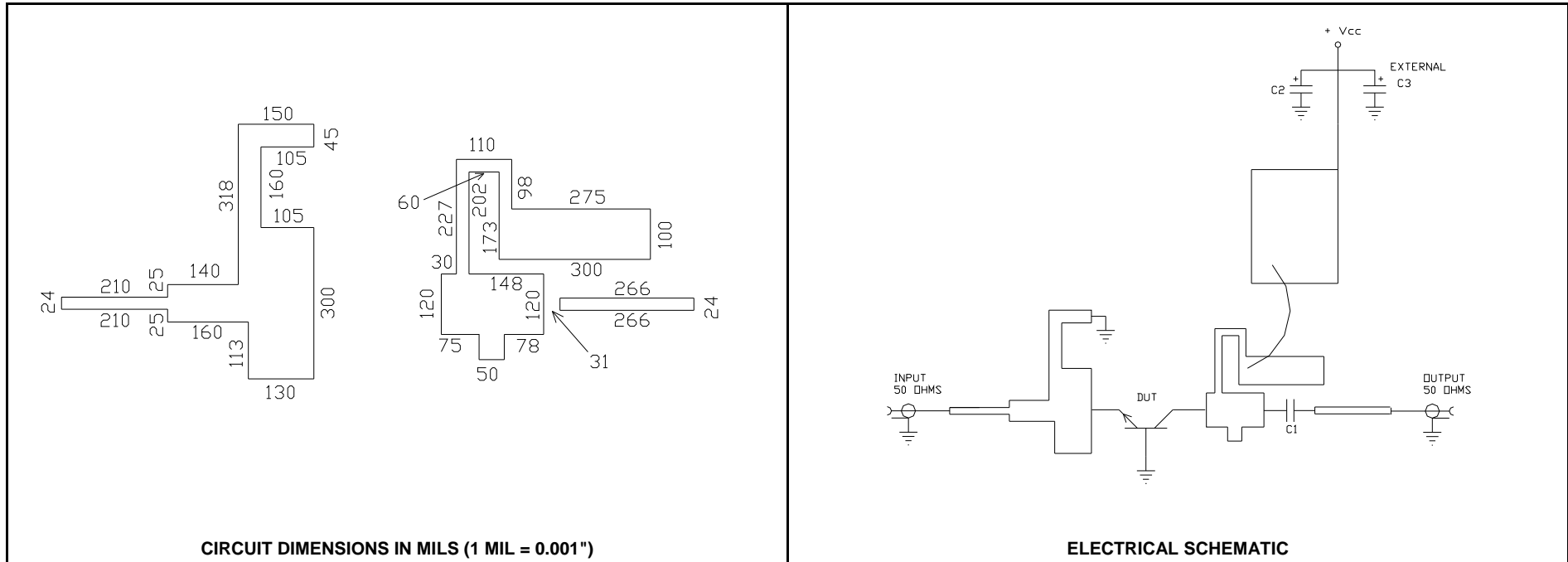
BROADBAND RF TEST FIXTURE



COMPONENT	DESCRIPTION
DUT	TRANSISTOR #IB3134M25
PC BOARD	ROGERS #RT6010.2LM, TH=0.025" 2E/2E
C1, C2	CHIP CAPACITOR, TYPE ATC100A, 39 pF
C3	ELECTROLYTIC CAPACITOR, 68uF / 63V
C4 - NOT SHOWN	ELECTROLYTIC CAPACITOR, 2200uF / 63V
GS	GROUND SHIM, COPPER, TH=0.001"
CONN1, CONN2	SMA CONNECTOR, TYPE DS #2052-5636-02
INPUT PC BOARD CARRIER	0.5 INCH BRASS - 01
OUTPUT PC BOARD CARRIER	0.5 INCH BRASS - 01
TRANSISTOR CARRIER	2 INCH COPPER - 01
TRANSISTOR CLAMP	NORYL CLAMP -01
HEAT SINK	2 INCH HEAT SINK - 09
DC CONN1	BANANA JACK, BLACK
DC CONN2	BANANA JACK, RED
JP	JUMPER WIRE
NOTE	FIXTURE HARDWARE DRAWINGS AVAILABLE ON REQUEST

ASSEMBLY AND PARTS LIST

BROADBAND RF TEST FIXTURE



DEFINITIONS

Data Sheet Status	
Proposed Specification	This data sheet contains proposed specifications.
Preliminary Specification	This data sheet contains specifications based on preliminary measurements and data.
Product Specification	This data sheet contains final product specifications.
Maximum Ratings	
Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only and operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.	

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO base is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with general or domestic waste.

DISCLAIMER

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