# ZL70550 Preliminary Datasheet
# Ultra-Low-Power Sub-GHz RF Transceiver

Power Matters.™

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# 1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

## 1.1 Revision 2

The following is a summary of the substantive changes in revision 2 of this document, dated February 2016.

- Item 1. Updated document format to be more in line with current Microsemi corporate branding standards, including restructuring the outline.
- Item 2. Updated RX state current and TX state current; see Features and Specifications, page 2, and Current Consumption, page 11.
- Item 3. Updated reference frequency to 24 MHz, which affects calculations for data rates, for channel separation, and for IF center frequency. See Features and Specifications, page 2, and General RF Parameters, page 11, and Receiver, page 13, and Crystal Oscillator, page 14.
- Item 4. Updated sensitivity specifications in Features and Specifications, page 2, and in Receiver, page 13.
- Item 5. Added Japanese bands in Features and Specifications, page 2.
- Item 6. Removed erroneous references to PHY in Features and Specifications, page 2, and in Z-Star Packet Mode, page 8.
- Item 7. Updated figures to show ten bytes of preamble and three bytes of frame sync; see MAC Packet Modes, page 5.
- Item 8. Updated output voltage, output current, and output rise time specifications in Digital Interface, page 10.
- Item 9. Added and modified table notes in General RF Parameters, page 11, in Current Consumption, page 11, in Receiver, page 13, and in Crystal Oscillator, page 14.
- Item 10. Updated limits for reference spurs in Synthesizer, page 12.
- Item 11. Updated limits for maximum input power, RSSI range, LBT minimum level, and 1-dB compression in Receiver, page 13.
- Item 12. Removed specifications for external clock output, average wake-up current, PLL clock time, PA ramp up/down, and channel change settling time in Electrical Specifications, page 9.
- Item 13. Updated graphs in Transmit Power Characteristics, page 15.
- Item 14. Changed markings for QFN in Drawing and Markings for 32-Pin QFN Package, page 21.
- Item 15. Changed package drawing for CSP and markings for CSP in Drawing and Markings for 29-Pin CSP Package, page 22.
- Item 16. Updated part numbers and table notes under Ordering Information, page 24.

This Preliminary Datasheet version contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

## 1.2 Initial Release

Revision 1, dated September 2015, was the first publication of this document.

This Advanced Datasheet version contained initial estimated information based on simulation, other products, devices, or speed grades. Such information can be used as estimates, but not for production, as the data is not fully characterized.

# 2 Overview

## 2.1 Introduction

The ZL70550 ultra-low-power RF transceiver provides efficient wireless communications for applications where power consumption is of primary importance. With combined ultralow transmit, receive, and sleep currents, the ZL70550 device is best-in-class for a wide range of high- and low-duty-cycle applications. The transceiver's small size and ultralow power requirements make it feasible to operate the device with a single coin-cell battery or with energy-harvesting sources in extremely small form factors. The built-in support for Microsemi's highly efficient and powerful Z-Star protocol allows users to rapidly develop ultra-low-power wireless applications.

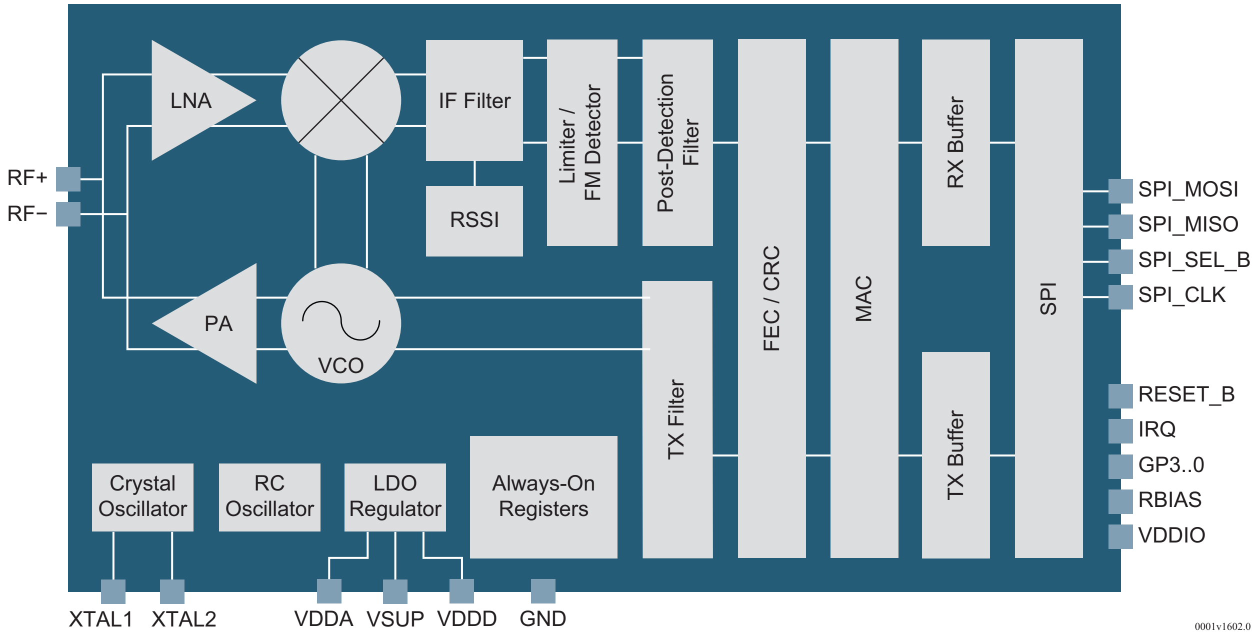
## 2.2 Features and Specifications

The ZL70550 RF transceiver features include:

- Ultralow power
  - Typical TX current (with 50-Ω match):
    < 2.75 mA at −10 dBm;
    < 5.3 mA at 0 dBm
  - Typical RX current: <2.4 mA (low $I_{RX}$ mode)
  - Sleep current: <10 nA typical
  - Supply: 1.71 V to 3.6 V
- Operating frequency range: 779 MHz to 965 MHz
  - North American ISM band: 902 MHz to 928 MHz
  - European SRD band: 863 MHz to 870 MHz
  - Chinese band: 779 MHz to 787 MHz
  - Japanese bands: 916 MHz to 930 MHz and 950 MHz to 956 MHz
- Sensitivity and data rate:
  - Raw data rate: 200 kbit/s, 100 kbit/s, or 50 kbit/s
  - Typical sensitivity:
    −106 dBm typical at 50 kbit/s at 3.2 mA and with FEC
    −103 dBm typical at 50 kbit/s at 2.4 mA and with FEC
    −99 dBm typical at 200 kbit/s at 3.2 mA and without FEC
    −95 dBm typical at 200 kbit/s at 2.4 mA and without FEC
- Very few external components
  - Matching network, crystal, decoupling capacitors, and bias resistor
  - Standard interface: SPI bus
- Optional built-in MAC
  - Microsemi Z-Star or user protocol support
  - Transmit and receive buffer
  - Automatic CSMA packet transfers
  - Efficient header optimized for small or large payloads
  - Optional preamble, frame sync, length, FEC, and CRC
- RoHS compliant

### 2.2.1 Block Diagram

***Figure 1 •*** **ZL70550 RF Transceiver Block Diagram**




## 2.3 Target Applications

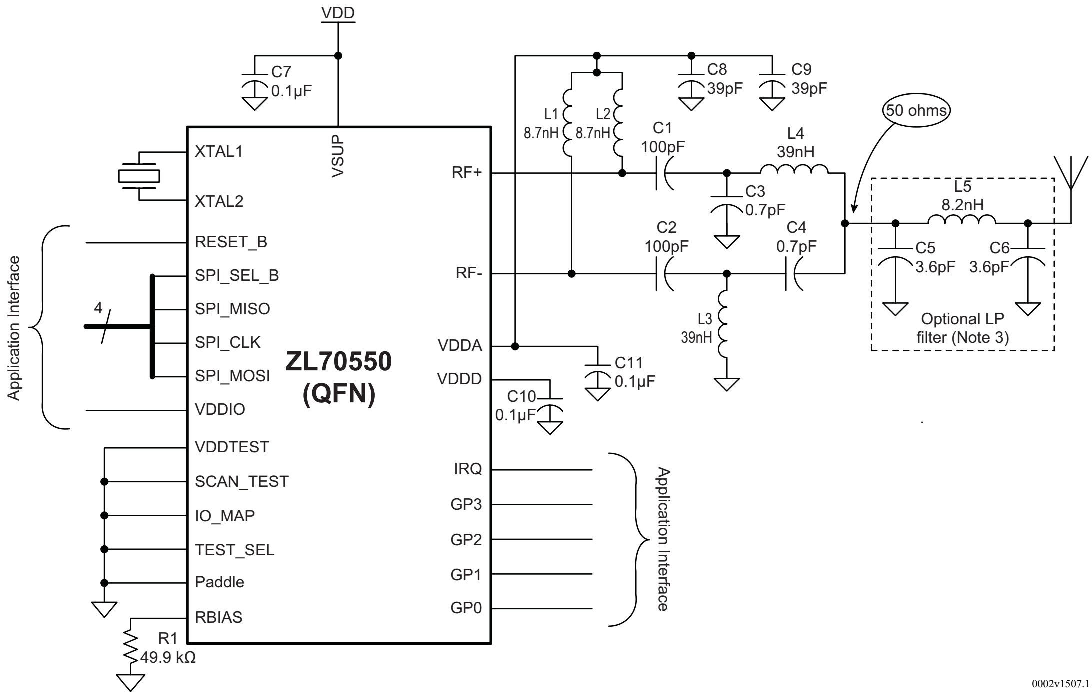
End applications may include:

- Medical monitoring
- Industrial/building/home automation
- Security
- Smart cities
- Advanced metering infrastructure
- Asset management
- Energy harvesting
- Voice/compressed-audio communications

## 2.3.1 Typical Application Diagram

The following figure is representative of a 50-Ω single-ended implementation (refer to Figure 2, page 4). An optional low-pass filter on the output is recommended to attenuate second and third harmonic spurious emissions to meet regulatory standards.

***Figure 2 •*** **50-Ω Single-Ended Application Example with Optional Low-Pass Filter**




**Notes:**

1. This schematic is based on the REMOTE550 board from the ZLE70550 Application Development Kit.
2. C3, C4, L3, and L4 values may change if the layout differs from the REMOTE550 board layout. To ensure optimal performance, please do not deviate from the REMOTE550 board layout.
3. L1 and L2 are optimized for tuning over the middle to upper frequency range (863 MHz to 965 MHz). Changing L1 and L2 to approximately 12 nH allows tuning over the lower to middle frequency range (779 MHz to 868 MHz).
4. The optional low-pass filter reduces the transmitter spurious emissions by approximately 16 dB for the second harmonic and 23 dB for the third harmonic. Another option would be to replace this circuit with a SAW filter to attenuate spurious emissions and to provide protection against blockers.
5. Use Murata part number GCM155R71C104KA55D or equivalent for C10 and C11.

# 3 Functional Descriptions

The ultra-low-power ZL70550 RF transceiver enables RF telemetry in applications powered by coin-cell batteries or energy harvesting, where wireless telemetry was previously unfeasible. End applications may include wireless sensors, medical monitoring, industrial/home automation, or smart cities.

With a typical peak/average current consumption below 2.4 mA in receive and 2.75 mA in transmit, and with an upper data rate of 200 kbit/s, the ZL70550 device enables bidirectional RF links over a distance of more than 100 meters (based on antenna gain and matching loss).

The output power is programmable and can be reduced to −25 dBm to save power in cases where the link budget allows it, or can be increased up to 0 dBm for more range or to allow for system losses such as a very small antenna or body tissue absorption.

To achieve the minimum possible power consumption, the ZL70550 device offers many automatic calibrations, all available to the user via the SPI bus.

In addition to its ultralow power consumption, the ZL70550 device also includes a highly flexible Media Access Controller (MAC) that offers four different packet modes of operation ranging from automatic packet transactions to low-level direct modulation via a serial clock and data.

## 3.1 MAC Packet Modes

The three different packet modes in which the ZL70550 MAC state machine operates, as well as a direct modulation mode where users have full control over their own packet or streaming protocols, are described in Table 1, page 5. These packet modes give users tremendous flexibility in defining their own packet parameters and transaction capabilities, ranging from a user-defined bit stream to fully automated multipacket transactions based on Microsemi's Z-Star protocol.

***Table 1 •*** **Packet Modes of Operation**

| Packet Mode | Description | Pre/Frm Sync | FEC | PHY Header | Auto-Length | MAC Header | CRC |
|---|---|---|---|---|---|---|---|
| Raw bit | Optional serial clock and data (TX/RX buffer or GP3..0 pins) | No | No | No | No | No | No |
| Raw byte | Compatible with ZL70251 MAC with optional FEC and CRC | Yes | Opt | No | No | No | Opt |
| User | User-defined packet (no MAC header) | Yes | Opt | Yes | Yes | No | Opt |
| Z-Star | Fully functional MAC based on Microsemi's Z-Star protocol | Yes | Opt | Yes | Yes | Yes | Yes |

### 3.1.1 Raw Bit Packet Mode

In raw bit mode, raw bits are transmitted without preamble, frame sync pattern, header, or CRC. If these properties are needed, then they must be encoded in the bit stream. The bit stream may be sourced from the TX buffer, from the GP3..0 pins, or generated from an internal pattern generator.

On the receiver side, the bit stream is received without frame synchronization or byte alignment. The received data either can be placed in the receive buffer or can be output with a clock on the GP3..0 pins.

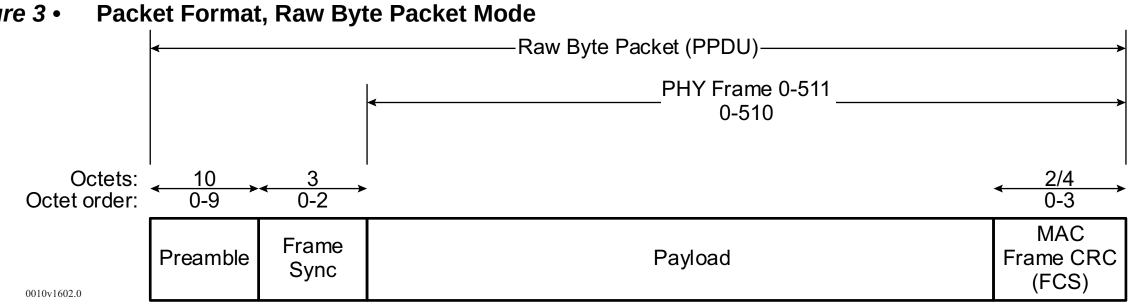
Raw bit mode has two basic applications. First, it can be used for raw bit error testing using the GP3..0 pins. Second, it can be used for applications where the packet framing is not desired, or for data rates not supported by the ZL70550 device. There are limitations to this second case.

### 3.1.2 Raw Byte Packet Mode

In raw byte packet mode, packets are transmitted without a MAC header, similar to the ZL70251 device. The CRC is optional but requires either a fixed-length packet or length information in the packet such that the application processor can dynamically extract the length from the beginning of the packet and change the RX packet length before the end of the packet is received.

The packet format is shown in Figure 3, page 6. If raw byte packet mode is used, then the TX and RX packet lengths are controlled by *tx_buf_len* and *rx_frm_len*, respectively. During reception, users may update *rx_frm_len*, providing this occurs before the end of the packet. Usually this requires users to embed the packet length as the first byte of the payload. The packet may optionally be terminated if the RSSI drops below the RSSI threshold setting or if a SPI Abort command is executed. In all cases, *rx_frm_len* indicates the length of the received packet.

***Figure 3 •*** **Packet Format, Raw Byte Packet Mode**

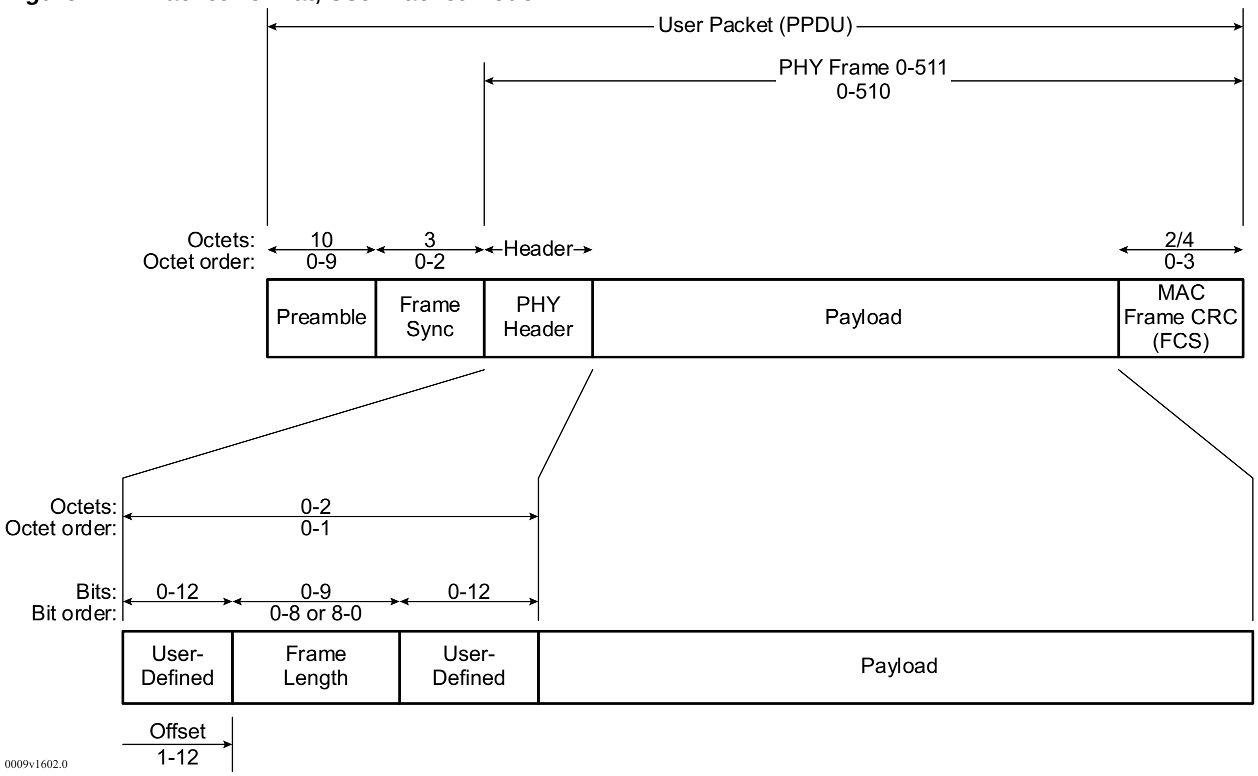


### 3.1.3 User Packet Mode

In user packet mode, packets are transmitted with a PHY header and optional FEC and CRC. The basic packet format is shown in Figure 4, page 7. The PHY header contains the length of the packet, which is used by the receiver to terminate the packet and calculate the CRC. The format of the PHY header in the received packet is flexible in that the length may be located at a programmable offset from the beginning of the PHY frame. It may be of various lengths and either MSB or LSB first.

For automatic PHY header generation on the transmit side, single-byte PHY headers are supported with LSB first by setting *tx_auto_hdr* equal to 1. For other formats, the PHY header must come from the transmit buffer.

***Figure 4 •*** **Packet Format, User Packet Mode**



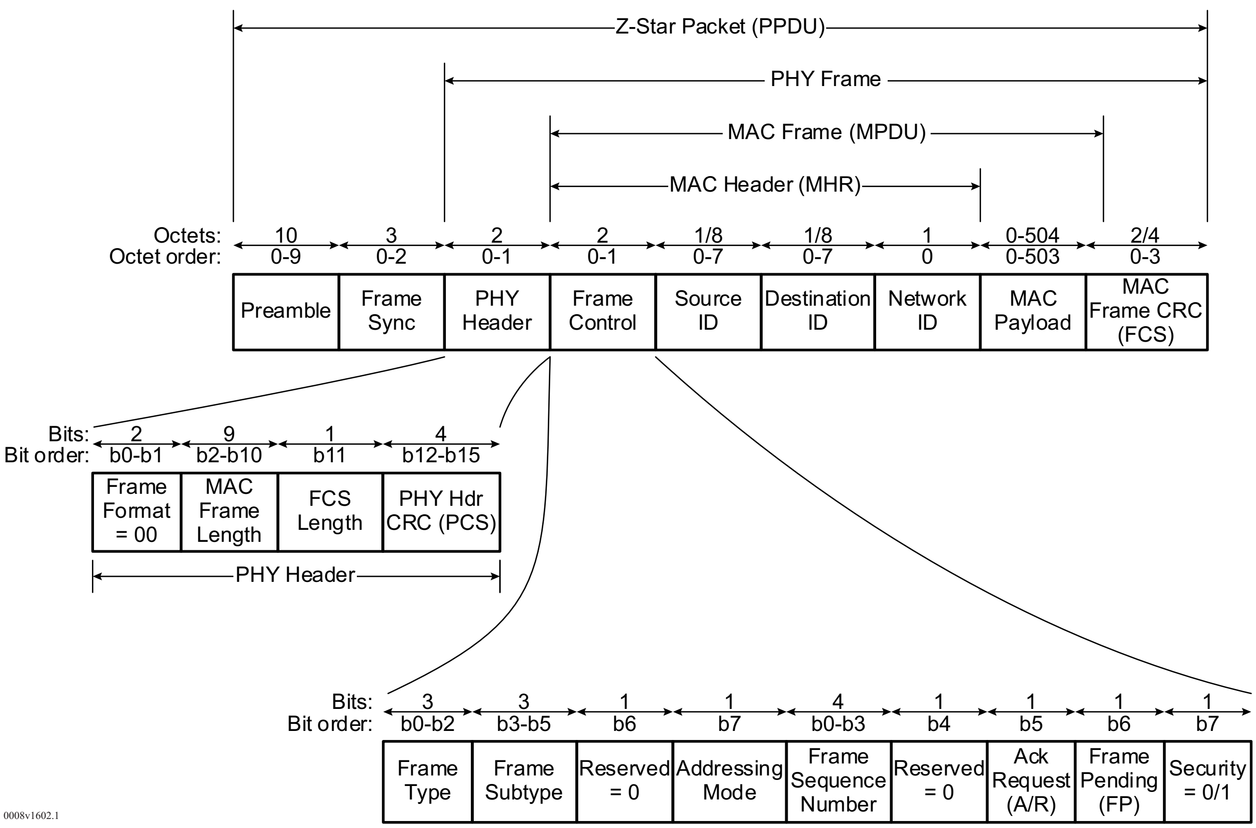
## 3.1.4 Z-Star Packet Mode

In Z-Star packet mode, packets are transmitted with a MAC header, a PHY header, either a 16-bit or 32-bit CRC (also known as a Frame Check Sequence (FCS)), and an option for using FEC. The basic packet format is shown in Figure 5, page 8. Z-Star packet mode supports the MAC layer of the Z-Star protocol as defined in the Z-Star protocol specification. The ZL70550 hardware performs the following Z-Star MAC functions:

- Automatic CSMA algorithm with random back off (LBT)
- Transmitting a packet with or without automatic acknowledgment reception
- Programmable automatic retransmissions
- Data request (node request to hub for data)
- Sniff with automatic packet reception or sleep (supports mesh networking)

The ZL70550 Z-Star MAC is a highly optimized and ultra-low-power protocol supporting a node/hub star network ideally suited for wireless sensor networks (WSNs) or Internet of things (IoT) applications. It is also highly flexible to support point-to-point transactions or other topologies. The combination of the highly optimized Z-Star MAC protocol and the best-in-class, ultra-low-power radio make the ZL70550 device the radio of choice where power efficiency is paramount.

***Figure 5 •*** **Packet Format, Z-Star Packet Mode**



# 4 Electrical Specifications

Voltages are with respect to ground (VSS) unless otherwise stated.

## 4.1 Absolute Maximum Ratings

***Table 2 •*** **Absolute Maximum Ratings**

| Parameter | Symbol | Limits Min. | Limits Max. | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage | $V_{SUP}$ | −0.3 | 3.6 | V | Note 1 |
| Digital I/O supply voltage | $V_{DDIO}$ | −0.3 | 3.6 | V | Note 1 |
| Digital I/O voltage | $V_{IOD}$ | VSS − 0.3 | $V_{DDIO}$ + 0.3 | V | Note 2 |
| Analog I/O voltage | $V_{IOA}$ | VSS − 0.3 | $V_{SUP}$ + 0.3 | V | Note 3 |
| RF I/O voltage | $V_{IORF}$ | VSS − 0.3 | 2 × $V_{DDA}$ | V | Note 4 |
| Storage temperature | $T_{STG}$ | −40 | 85 | °C | Unpowered |
| Electrostatic discharge (human body model) | $V_{HBM}$ | | 500 | V | RF and crystal pads; Note 5 |
| | | | 1500 | V | All other pads; Note 5 |
| Electrostatic discharge (charged-device model) | $V_{CDM}$ | | 250 | V | All pads |

1. Application of voltage beyond the stated absolute maximum rating may cause permanent damage to the device or cause reduced reliability.
2. Applies to digital interface pins including GP3..0, IRQ, RESET_B, SPI_CLK, SPI_MISO, SPI_MOSI, SPI_SEL_B, IO_MAP, SCAN_TEST, and TEST_SEL.
3. Applies to analog interface pins, including RBIAS, XTAL1, and XTAL2.
4. Applies to RF interface pins, including RF+, RF−, TX+, TX−, RX+, and RX−.
5. Applied one at a time. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

### 4.1.1 Recommended Operating Conditions

The recommended operating conditions define the nominal conditions for the device. This means that a specified parameter is valid for the recommended operating conditions stated in Table 3, page 9, unless otherwise noted.

***Table 3 •*** **Recommended Operating Conditions**

| Parameter | Symbol | Limits Min. | Limits Typ. | Limits Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $VDD_{OP}$ | 1.8 | | 3.5 | V | |
| Operating temperature | $T_{OP}$ | −40 | 25 | 85 | °C | |

# 4.2 Electrical Characteristics

## 4.2.1 Voltage Regulators

***Table 4 •*** **Voltage Regulators**

| Parameter | Symbol | Limits | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage range | $V_{DDA}$ | 1.46 | 1.52 | 1.57 | V | Note 1 |
| Output voltage range | $V_{DDD}$ | 1.20 | 1.25 | 1.30 | V | Note 1 |

1. Do not connect external circuits to these pins. VDDA and VDDD are regulated supplies for the internal analog and digital circuits, respectively, of the ZL70550 device.

## 4.2.2 Digital Interface

***Table 5 •*** **Digital I/O AC and DC Specifications**

| Parameter | Symbol | Limits | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| High-level output voltage | $V_{OH}$ | VDD − 0.2 | | V | |
| Low-level output voltage | $V_{OL}$ | | VSS + 0.2 | V | |
| High-level input voltage | $V_{IH}$ | $V_{DDIO}$ × 0.85 | $V_{DDIO}$ | V | |
| Low-level input voltage | $V_{IL}$ | $V_{SSD}$ | $V_{DDIO}$ × 0.15 | V | |
| High-level output current | $I_{OH}$ | | 1 | mA | |
| Low-level output current | $I_{OL}$ | | 1 | mA | |
| Input leakage current | $I_{LEAK}$ | −10 | 10 | nA | |
| Output rise time (20% to 80%) | $T_R$ | | 35 | ns | Load of 120 pF at 1 mA |
| Output fall time (80% to 20%) | $T_F$ | | 35 | ns | Load of 120 pF at 1 mA |

## 4.2.3 Performance Characteristics

The specified performance of the ZL70550 device is valid over a supply range of 1.8V to 3.5V.

### 4.2.3.1 General RF Parameters

***Table 6 •*** **General Characteristics**

| Parameter | Limits Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Operating frequency range | 779 | | 965 | MHz | |
| Reference frequency | | 24 | | MHz | See Note 1 |
| Symbol rate | | 200 | | kbit/s | 300-kHz channel width (24MHz / 20 / 6) |
| | | 100 | | kbit/s | 300-kHz channel width (24MHz / 20 / 12) |
| | | 50 | | kbit/s | 300-kHz channel width (24MHz / 20 / 24) |
| Channel separation | | 300 | | kHz | Note 2 |
| Crystal oscillator startup time | | | 1 | ms | |
| Modulation index | 0.45 | 0.5 | 0.55 | | Based on a raw data rate of 200kbit/s |

1. In order to save power and reduce the number of external components, the crystal oscillator has a 3-pF load instead of a typical 8-pF or 10-pF load (refer to Table 11, page 14). The 3-pF load is representative of the pin and PCB parasitic capacitance.
2. This is not an occupied bandwidth. It is based on the typical channel bandwidth; however, other channel bandwidths can be programmed.

### 4.2.3.2 Current Consumption

***Table 7 •*** **Current Consumption**

| Parameter | Symbol | Limits Min. | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| SLEEP state current | $I_{SLEEP}$ | | 10 | 50 | nA | Partial register retention only |
| IDLE state current | $I_{IDLE}$ | | 200 | 300 | µA | Crystal oscillator running only |
| RX state current | $I_{RX}$ | | 2.4 | | mA | LNA gain=8’h0F, LNA bias=8’h05 |
| | | | 3.2 | | mA | LNA gain=8’h0F, LNA bias=8’h29 |
| TX state current (CW on 916MHz) | $I_{TX}$ | | 5.3 | | mA | 0dBm into a 50-Ω load |
| | | | 2.75 | | mA | −10dBm into a 50-Ω load |
| RSSI sniff current | $I_{SNIFF}$ | | 2.4 | | mA | |

### 4.2.3.3 Synthesizer

***Table 8 •*** **Synthesizer**

| Parameter | Symbol | Limits Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Phase noise at 100 kHz | $\Phi_{SYNTH\_100k}$ | | −92 | | dBc/Hz | CW observed from PA |
| Reference spurs | $\Psi_{SYNTH\_CLRS}$ | | −60 | | dBc | At 300 kHz (25 °C);<br>CW from PA |

### 4.2.3.4 Transmitter

***Table 9 •*** **Transmitter RF Characteristics**

| Parameter | Condition | Limits Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Output power | PA = maximum setting | | 0 | | dBm | Measured on ADK (50 Ω match); no SAW filter (for typical values refer to Figure 7, page 15) |
| | PA = minimum setting | | −25 | | | |
| Spurious emissions | | | | −35 | dBm | |
| TX-RX or RX-TX turnaround time | | | 850 | | µs | Programmable<br>Highest data rate<br>See Note 1 |

1. Last bit of previous packet to first bit of header.

### 4.2.3.5 Receiver

***Table 10 •*** **Receiver RF Characteristics**

| Parameter | Limits Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Sensitivity at 25°C, 1.8V | | −106 | | dBm | 50kbit/s with $I_{RX}$=3.2mA (LNA gain=8'h0F, LNA bias=8'h29) with FEC |
| | | −103 | | dBm | 50kbit/s with $I_{RX}$=2.4mA (LNA gain=8'h0F, LNA bias=8'h21) with FEC |
| | | −99 | | dBm | 200kbit/s with $I_{RX}$=3.2mA (LNA gain=8'h0F, LNA bias=8'h29) without FEC |
| | | −95 | | dBm | 200kbit/s with $I_{RX}$=2.4mA (LNA gain=8'h0F, LNA bias=8'h05) without FEC |
| Maximum input power | −34 | | | dBm | 200kbit/s with $I_{RX}$=2.4mA (LNA gain=8'h0F, LNA bias=8'h21) with FEC |
| Cascaded voltage gain | | 30 | | dB | LNA and mixer; programmable, with five settings in 3-dB to 4-dB steps ($I_{RX}$=2.4mA) |
| IF center frequency | | 600 | | kHz | (300kHz × 2) |
| RSSI range | 40 | | | dB | Linear range (±1 LSB)<br>Digital, 32 levels of 2dB |
| RSSI resolution | | 2 | | dB | Note 1 |
| RSSI accuracy | | ±2 | | dB | Note 2 |
| Listen Before Talk (LBT) minimum level | | | −100 | dB | |
| Adjacent channel rejection | | 11 | | dB | Relative to sensitivity<br>Desired channel 3dB above the sensitivity limit; 300-kHz channel spacing with a modulated interferer |
| Alternate channel rejection | | 25 | | dB | Relative to sensitivity<br>Desired channel 3dB above the sensitivity limit; 600-kHz channel spacing with a modulated interferer |
| Blocker rejection | 11 | | | dB | At ±2MHz, EN300 200 limits |
| | 31 | | | dB | At ±10MHz, EN300 200 limits |
| 1-dB compression | | −41 | | dBm | LNA gain=8'h0F |
| Third-order input intercept point | | 3.5 | | mVrms | LNA gain=8'h07 |

1. Nominal ADC quantization. The average RSSI results have seven bits rather than five if the averaging length is four or more. The accuracy in this case is ±0.5dB due to the dithering/averaging of noise at lower levels where LBT thresholds are set.
2. Calibrated at one LNA gain, one temperature and one input level (for LBT).

### 4.2.3.6 Crystal Oscillator

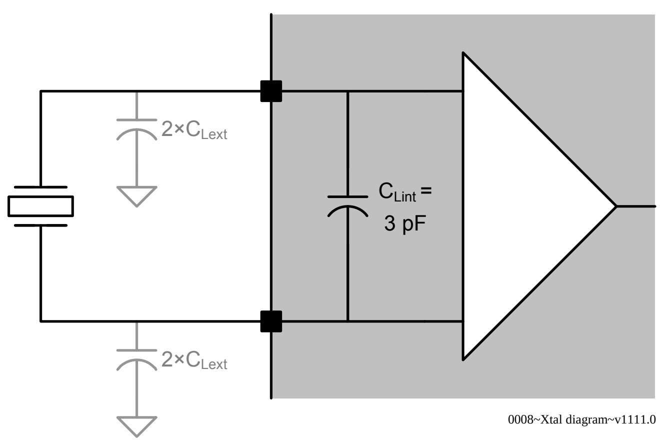
All frequency-related specifications are based on the crystal oscillator performance, which, in turn, is dependent on the crystal specifications. The ZL70550 device specifications assume that the crystal specifications listed in the following table are met or exceeded (refer to Table 11, page 14). The crystal oscillator is trimmable to ±5ppm at room temperature when attached to a crystal meeting the specifications in Table 11, page 14.

***Table 11 •*** **Crystal Specifications**

| Parameter | Limits Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Frequency | | 24 | | MHz | |
| Frequency tolerance | −30 | | 30 | ppm | |
| Stability with temperature | −25 | | 25 | ppm | Over operating temperature |
| Operating temperature range | −40 | 25 | 85 | °C | |
| Equivalent series resistance | 12 | | 130 | ohm | |
| Motional resistance | 0 | 1 | 17 | ohm | |
| Shunt capacitance | 1.4 | 1.65 | 1.9 | pF | Note 1 |
| Motional capacitance | 3.2 | 3.35 | 3.5 | fF | Note 1 |
| Load capacitance | | 3 | | pF | Note 2 |
| Drive level | | | 50 | µW | |
| Aging | −3 | | 3 | ppm | First year only; none thereafter |

1. A low shunt capacitance and high motional capacitance is best as it results in a larger trim range. It is particularly important if external capacitors are used, as those reduce the trim range.
2. In order to save power, the crystal oscillator presents a 3-pF load instead of the typical 8-pF or 10-pF load. A slight frequency pull, on the order of 100ppm to 150ppm, would result if using a standard crystal without additional external load capacitors. Such a deviation has no effect on the operation of the device and is generally not a problem for most applications, providing all ZL70550 devices have the same frequency pull (within trimmable range). If the deviation is not acceptable and power is critical, a special cut crystal may be used (that is, slightly slower to compensate for the pull). Microsemi is engaging with crystal manufacturers in developing custom crystals that operate at 24MHz with only a 3-pF load. Alternatively, if power is not as critical, external capacitors can be added (as shown in Figure 6, page 14) to bring the total load capacitance to the crystal load specification. For instance, for a crystal with an 8-pF load specification (CL), $CL_{EXT}$ = 8pF − 3pF = 5pF, so two 10-pF capacitors need to be added, one on each end of the crystal. It must be noted that this results in a reduced trim range.

***Figure 6 •*** **Crystal Oscillator with Optional Additional External Load Capacitors**

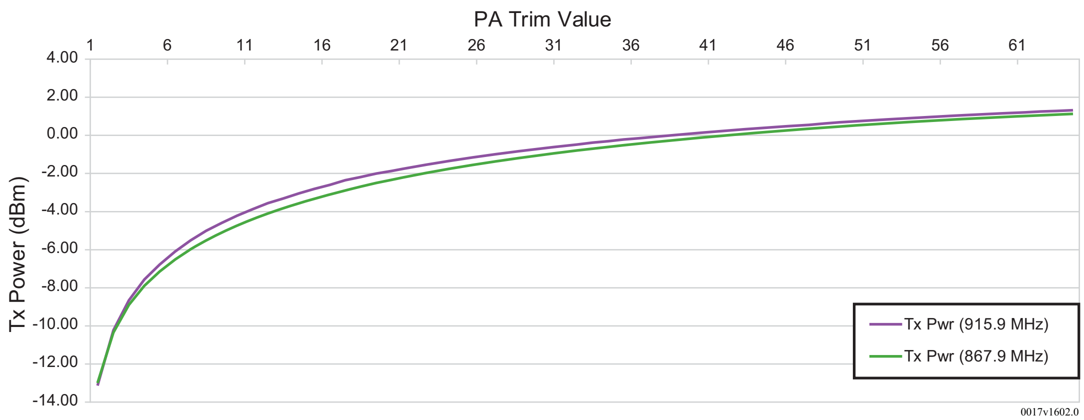


## 4.3 Transmit Power Characteristics

The following figures illustrate the relationship between TX power, PA trim setting, and current consumption (refer to Figure 7, page 15, and Figure 8, page 15). These measurements were made on the REMOTE550 board from a ZL70550 Application Development Kit (ADK) at room temperature and with a supply voltage of 1.8 V. The figures include the losses of the matching network (approximately 2 dB to 3 dB).

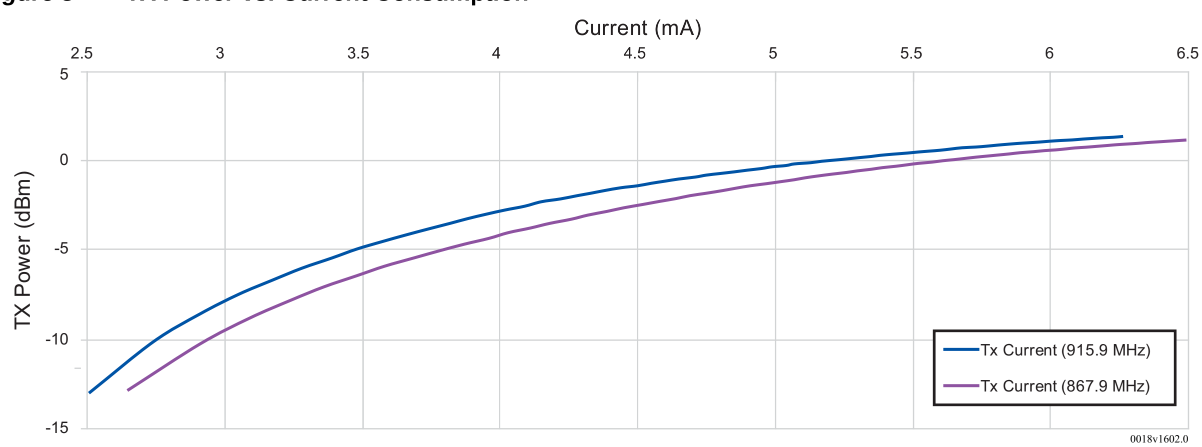
### 4.3.1 Transmit Power vs. PA Trim Value

***Figure 7 •*** **TX Power vs. PA Trim Value**




### 4.3.2 Transmit Power vs. Current Consumption

***Figure 8 •*** **TX Power vs. Current Consumption**



# 5 Pin Descriptions

The ZL70550 device is available in two package options, a 32-pin QFN and a 29-pin CSP. The pins are described in this section.

## 5.1 Pin Diagrams

The following illustrations are representations of the QFN and CSP packages, respectively, for the ZL70550 device.

***Figure 9 •*** **Footprint (top view) for 32-Pin QFN**

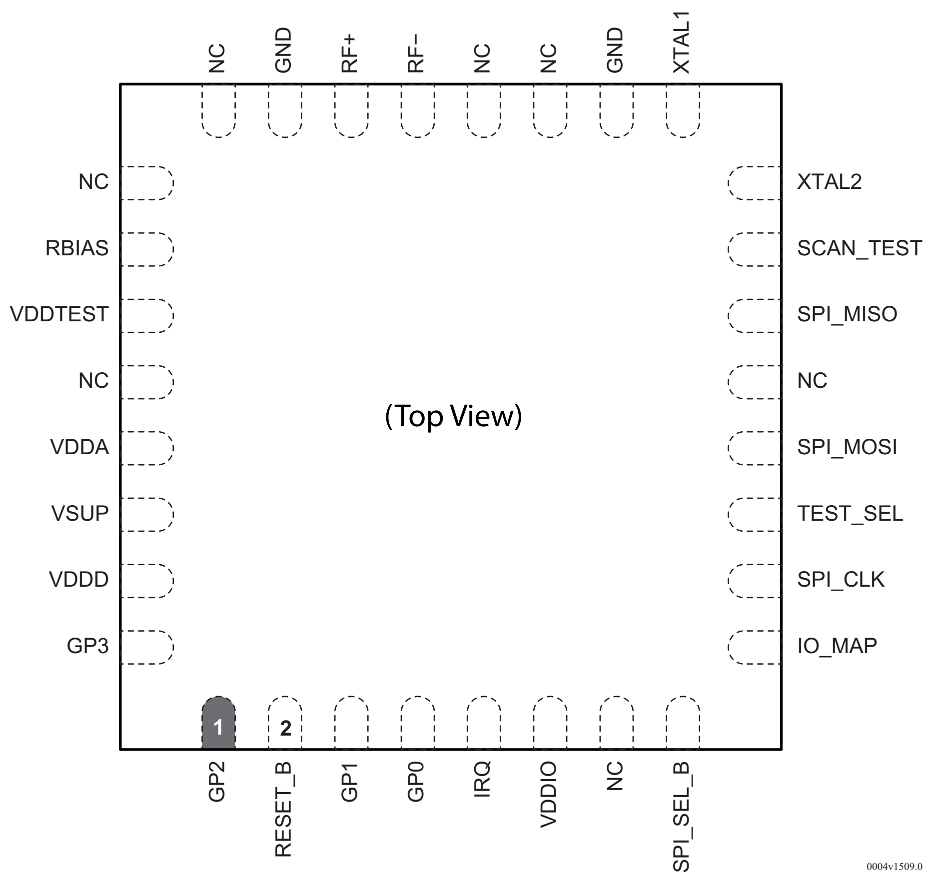
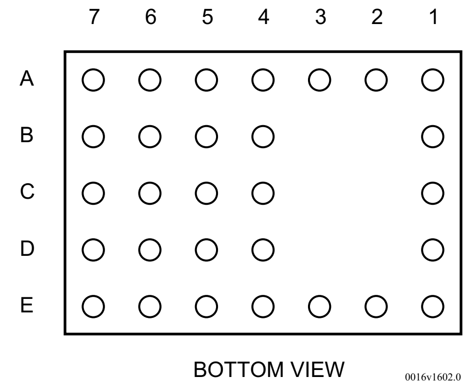


**Figure 10 • Footprint (bottom view) for 29-Pin CSP Package**




## 5.2 Pin Lists

The pinouts for the QFN and CSP packages of the ZL70550 device are listed in Table 12, page 18, and Table 13, page 18, respectively.

Connect the internal ground paddle to the ground plane of the PCB. A minimum of four vias between the SMD pad and the ground plane are recommended to ensure reliable performance.

For the QFN, the ground paddle is the primary ground for the device in addition to pins 18 and 23 (refer to Table 12, page 18).

*Table 12 •* **Pinout for 32-Pin QFN**

| Pin Name[1] | Pin Number | Pin Name[1] | Pin Number |
|---|---|---|---|
| GP2 | 1 | GND | 18 |
| RESET_B | 2 | NC | 19 |
| GP1 | 3 | NC | 20 |
| GP0 | 4 | RF− | 21 |
| IRQ | 5 | RF+ | 22 |
| VDDIO | 6 | GND | 23 |
| NC | 7 | NC | 24 |
| SPI_SEL_B | 8 | NC | 25 |
| IO_MAP | 9 | RBIAS | 26 |
| SPI_CLK | 10 | VDDTEST | 27 |
| TEST_SEL | 11 | NC | 28 |
| SPI_MOSI | 12 | VDDA | 29 |
| NC | 13 | VSUP | 30 |
| SPI_MISO | 14 | VDDD | 31 |
| SCAN_TEST | 15 | GP3 | 32 |
| XTAL2 | 16 | Paddle | N/A |
| XTAL1 | 17 | | |

1. *NC denotes reserved pin. Do not use; do not connect.*

**Table 13 • Pinout for 29-Pin CSP**

| Pin Name | Pin Number | Pin Name | Pin Number |
|---|---|---|---|
| RX+ | A1 | GP0 | C6 |
| RBIAS | A2 | IRQ | C7 |
| VDDTEST | A3 | TX− | D1 |
| VSSA | A4 | SCAN_TEST | D4 |
| VDDA | A5 | TEST_SEL | D5 |
| VDDD | A6 | IO_MAP | D6 |
| GP3 | A7 | VDDIO | D7 |
| TX+ | B1 | VSSA2 | E1 |
| GP1 | B4 | XTAL1 | E2 |
| VSUP | B5 | XTAL2 | E3 |
| GP2 | B6 | SPI_MISO | E4 |
| RESET_B | B7 | SPI_MOSI | E5 |
| RX− | C1 | SPI_CLK | E6 |
| VSSD | C4 | SPI_SEL_B | E7 |
| VSSD2 | C5 | | |

## 5.3 Functional Pin Descriptions

The following table shows the functional pin descriptions for the ZL70550 device.

***Table 14 •*** **Overview of ZL70550 Interconnects**

| Symbol | I/O | Type | Description |
|---|---|---|---|
| ***Interconnects Available on All Package Options*** | | | |
| GP0 | I/O | A/D | Analog and digital test bus input and output. General-purpose use for digital I/O. |
| GP1 | I/O | A/D | Analog and digital test bus input and output. General-purpose use for digital I/O. |
| GP2 | I/O | A/D | Analog and digital test bus input and output. General-purpose use for digital I/O. |
| GP3 | I/O | A/D | Analog and digital test bus input and output. General-purpose use for digital I/O. |
| 7IO_MAP | I | D | Connect to ground. Used for device testing only. |
| IRQ | O | D | Interrupt output. |
| NC | N/A | N/A | No connection (do not ground pin). |
| RBIAS | I | A | Bias setting resistor used to trim the internal current reference. Use a 49.9-kohm resistor (±1%) to ground. |
| RESET_B | I | D | Asynchronous reset (active low) with a minimum low period of 100 ns. When low, the ZL70550 is in reset and all circuits are off. When transitioning from low to high, all registers are set to their power-on-reset values, the crystal oscillator starts up, all other circuits are disabled, and the ZL70550 enters into the **IDLE** state. |
| SCAN_TEST | I | D | Connect to ground. Used for device testing only. |
| SPI_CLK | I | D | SPI bus clock input. |
| SPI_MISO | O | D | SPI bus data output. This output is tri-stated when SPI_SEL_B is high and driven when SPI_SEL_B is low. |
| SPI_MOSI | I | D | SPI bus data input. |
| SPI_SEL_B | I | D | SPI bus select input (active low). When low, the SPI_MISO output buffer is enabled. |
| TEST_SEL | I | D | Connect to ground. Used for device testing only. |
| VDDA | O | A | 1.52-volt regulator output used to power most on-chip analog circuits. Connect a 100-nF X7R ceramic capacitor between VDDA and ground. |
| VDDD | O | A/D | 1.25-volt regulator output used to power most on-chip digital circuits. Connect a 100-nF X7R ceramic capacitor between VDDD and ground. |
| VDDIO | I | A/D | Power supply input to the internal level shifters (1.8 volts to 3.5 volts). Controls the digital signaling level for all ZL70550 digital I/O. |
| VDDTEST | I | A | Connect to ground. Used for device testing only. |
| VSUP | I | A/D | Supply voltage (1.71 volts to 3.6 volts). |
| XTAL1 | I | A | Crystal connection to the gate (input) of the crystal oscillator. Can also be driven with an external clock source. |
| XTAL2 | O | A | Crystal connection to the drain (output) of the crystal oscillator. |

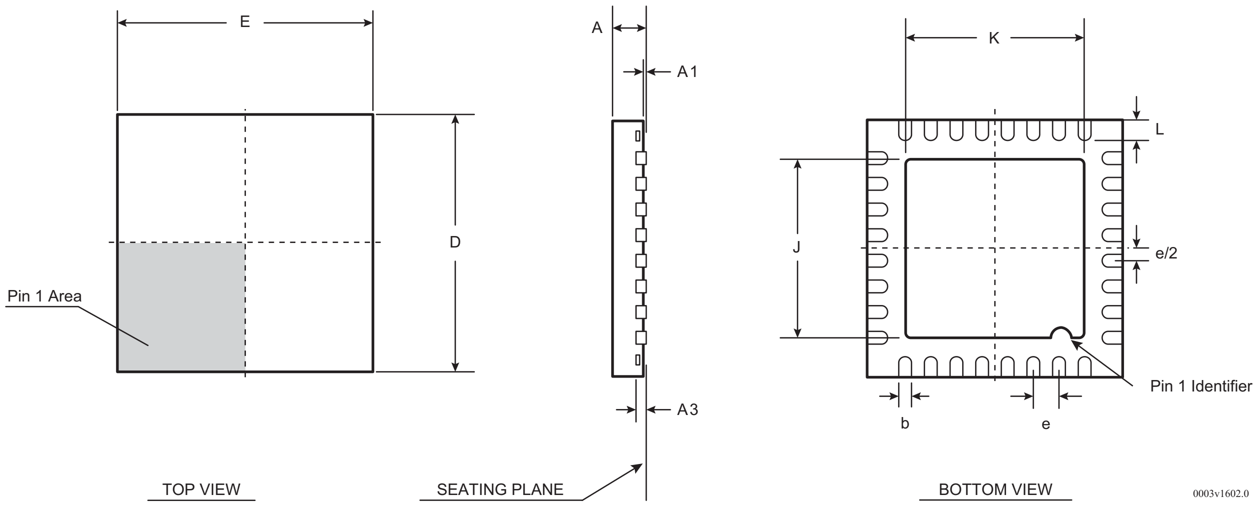
**_Table 14 •_ Overview of ZL70550 Interconnects _(continued)_**

| Symbol | I/O | Type | Description |
|---|---|---|---|
| ***RF and Ground Connections on QFN Package*** | | | |
| Paddle | I | A/D | Ground connection. |
| GND | I | A/D | Ground connection. |
| RF+ | I/O | A | RF positive (TX/RX). TX+ and RX+ are bonded together. |
| RF− | I/O | A | RF negative (TX/RX). TX− and RX− are bonded together. |
| ***RF and Ground Connections on CSP Package*** | | | |
| RX+ | I | A | Receiver RF positive input. This input is AC coupled and is connected to an internal shunt capacitor that can be used for automatic tuning to antennas or matching networks that connect directly to the receiver inputs. |
| RX− | I | A | Receiver RF negative input.This input is AC coupled and is connected to an internal shunt capacitor that can be used for automatic tuning to antennas or matching networks that connect directly to the receiver inputs. |
| TX+ | O | A | Transmitter RF positive output. Requires external biasing to VDDA. |
| TX− | O | A | Transmitter RF negative output. Requires external biasing to VDDA. |
| VSSA | I | A | Ground connection. |
| VSSA2 | I | A | Ground connection. |
| VSSD | I | A | Ground connection. |
| VSSD2 | I | A | Ground connection. |

# 6 Package Information

## 6.1 Drawing and Markings for 32-Pin QFN Package

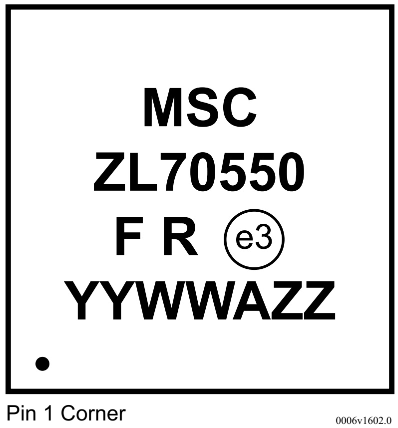
***Figure 11 •*** **Package Drawing and Package Dimensions for 32-Pin QFN**




| | Common Dimensions | | |
|---|---|---|---|
| **Symbol** | **Minimum** | **Nominal** | **Maximum** |
| A | 0.8 | 0.9 | 1.0 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.2 | |
| b | 0.20 | 0.25 | 0.30 |
| D | | 5.00 | |
| E | | 5.00 | |
| e | | 0.50 | |
| J | 3.40 | 3.50 | 3.60 |
| K | 3.40 | 3.50 | 3.60 |
| L | 0.35 | 0.40 | 0.45 |

**Notes**:
1. Dimensioning and tolerances conform to ASME Y14.5M. – 1994.
2. All dimensions are in millimeters.
3. Not to scale.

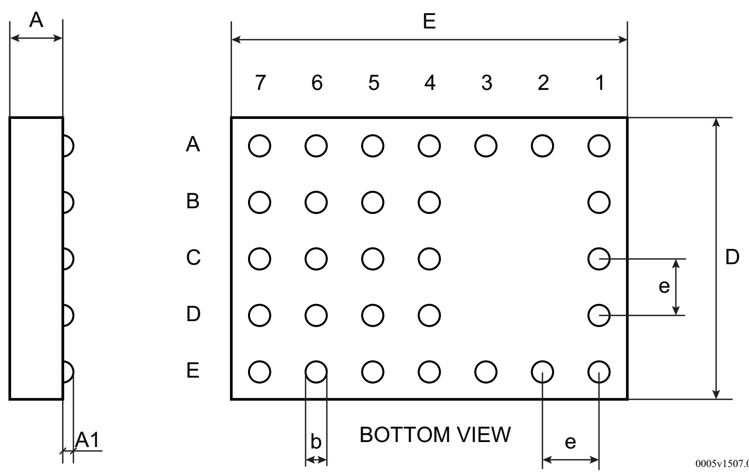
*Figure 12 •* **Markings for 32-Pin QFN**




**Notes**:
1. YY = Last two digits of year of encapsulation
2. WW = Week number of encapsulation
3. ZZ = Assembly lot sequence code
4. A = Assigned Assembly Site Identifier
5. F = Fab code
6. R = Product revision code
7. e3 = Denotes Pb-free

## 6.2 Drawing and Markings for 29-Pin CSP Package

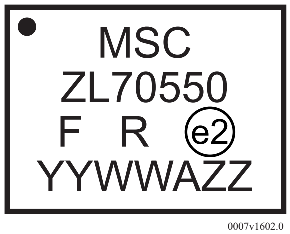
*Figure 13 •* **Package Drawing and Package Dimensions for 29-Pin CSP**




| | **Common Dimensions (mm)** | | |
|---|---|---|---|
| **Symbol** | **Minimum** | **Nominal** | **Maximum** |
| A | | 0.317 | |
| A1 | | 0.115 | |
| b [1] | | 0.150 | |
| D | | 1.99 | |
| E | | 3.085 | |
| e | | TBD BSC | |

**Notes**:
1. UBM diameter
2. Ball positions are currently being updated.

***Figure 14 •*** **Markings for 29-Pin CSP**




**Notes**:
1. YY = Last two digits of year of encapsulation
2. WW = Week number of encapsulation
3. ZZ = Assembly lot sequence code
4. A = Assigned Assembly Site Identifier
5. F = Fab code
6. R = Product revision code
7. e2 = Denotes Pb-free
8. Orientation marker corresponds to pin A1

# 7 Ordering Information

The ZL70550 RF transceiver is available in two package options.

***Table 15 •*** **Ordering and Package Overview**

| Ordering Code | Temp Range (°C) | Package | Delivery Form | Pb-Free |
|---|---|---|---|---|
| ZL70550LDF1 (contact Microsemi for availability) | −40 to 85 | 32-pin QFN | Tape and reel | YES [1] |
| ZL70550UGB4 (contact Microsemi for availability) | −40 to 85 | 29-pin CSP | Tape and reel | YES [2] |

1. Matte tin.
2. Sn/Ag (97.5 percent tin, 2.5 percent silver).