CGH27030S

30 W, DC - 6.0 GHz, 28 V, GaN HEMT

Cree's CGH27030S is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT) designed specifically for high efficiency, high gain and wide bandwidth capabilities, which makes the CGH27030S ideal for LTE, 4G Telecom and BWA amplifier applications. The CGH27030S operates from a 28 volt rail. The transistor is available in a 3mm x 4mm, surface mount, dual-flat-no-lead (DFN) package.

Package Type: 3x4 DFN
PN: CGH27030S

Typical Performance 1.8 - 2.2 GHz (T_C = 25˚C) , 28 V

Parameter	1.8 GHz	2.0 GHz	2.2 GHz	Units
Small Signal Gain	20.0	20.4	19.5	dB
Adjacent Channel Power @ P_{OUT} =5 W	-39.5	-42.1	-39.1	dBc
Drain Efficiency @ P_{OUT} = 5 W	31.8	32.8	33.8	%
Input Return Loss	-4.2	-6.4	-7.7	dB

Note:
Measured in the CGH27030S-TB1 application circuit.
Under 7.5 dB PAR single carrier WCDMA signal test model 1 with 64 DPCH.

Typical Performance 2.3 - 2.7 GHz (T_C = 25˚C) , 28 V

Parameter	2.3 GHz	2.5 GHz	2.7 GHz	Units
Small Signal Gain	21.1	20.6	20.0	dB
Adjacent Channel Power @ P_{OUT} =3.2 W	-32.0	-36.4	-33.6	dBc
Drain Efficiency @ P_{OUT} = 3.2 W	37.8	36.2	35.0	%
Input Return Loss	-7.3	-7.9	-7.2	dB

Note:
Measured in the CGH27030S-TB2 application circuit.
Under 7.5 dB PAR single carrier WCDMA signal test model 1 with 64 DPCH.

Features for 28 V in CGH27030S-TB1

- 1.8 - 2.2 GHz Operation
- 30 W Typical Output Power
- 18 dB Gain at 5 W P_{AVE}
- -39 dBc ACLR at 5 W P_{AVE}
- 33% efficiency at 5 W P_{AVE}
- High degree of APD and DPD correction can be applied

Features for 28 V in CGH27030S-TB2

- 2.3 - 2.7 GHz Operation
- 30 W Typical Output Power
- 18.5 dB Gain at 5 W P_{AVE}
- -39 dBc ACLR at 5 W P_{AVE}
- 36% efficiency at 5 W P_{AVE}
- High degree of APD and DPD correction can be applied

Rev 1.0 – May 2014

Absolute Maximum Ratings (not simultaneous) at 25˚C Case Temperature

Parameter	Symbol	Rating	Units	Notes
Drain-Source Voltage	V_{DSS}	84	Volts	25˚C
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts	25˚C
Storage Temperature	T_{STG}	-65, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	7.2	mA	25˚C
Maximum Drain Current[1]	I_{DMAX}	3.0	A	25˚C
Soldering Temperature[2]	T_S	245	˚C	
Case Operating Temperature[3]	T_C	-40, +150	˚C	
Thermal Resistance, Junction to Case[4,5]	$R_{\theta JC}$	3.43	˚C/W	85˚C

Note:

[1] Current limit for long term, reliable operation

[2] Refer to the Application Note on soldering at www.cree.com/rf/document-library

[3] T_C = Case temperature for the device. It refers to the temperature at the ground tab underneath the package. The PCB will add additional thermal resistance. See also, the Power Dissipation De-rating Curve on page 12.

[4] Measured for the CGH27030S at P_{DISS} = 21.6 W

[5] The R_{TH} for Cree's demonstration amplifier, CGH27030S-TB1, with 33 x 0.011 via holes designed on a 20 mil thick Rogers 4350 PCB, is 3.29°C. The total R_{TH} from the heat sink to the junction is 3.43°C + 3.29°C = 6.72°C/W.

Electrical Characteristics (T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[1]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.8	-3.0	-2.3	V_{DC}	V_{DS} = 10 V, I_D = 7.2 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.7	–	V_{DC}	V_{DS} = 28 V, I_D = 0.20 mA
Saturated Drain Current	I_{DS}	5.8	7.0	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	84	–	–	V_{DC}	V_{GS} = -8 V, I_D = 7.2 mA
RF Characteristics[2,3] (T_C = 25˚C, F_0 = 2.2 GHz unless otherwise noted)						
Gain	G	–	18.3	-	dB	V_{DD} = 28 V, I_{DQ} = 0.20 A, P_{OUT} = 37 dBm
WCDMA Linearity[4]	ACLR	–	-39	–	dBc	V_{DD} = 28 V, I_{DQ} = 0.20 A, P_{OUT} = 37 dBm
Drain Efficiency[4]	η	–	33.7	-	%	V_{DD} = 28 V, I_{DQ} = 0.20 A, P_{OUT} = 37 dBm
Output Mismatch Stress	VSWR	-	10 : 1	-	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 0.20 A, P_{OUT} = 37 dBm
Dynamic Characteristics						
Input Capacitance[5]	C_{GS}	–	8.6	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance[5]	C_{DS}	–	2.0	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.4	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:

[1] Measured on wafer prior to packaging

[2] Scaled from PCM data

[3] Measured in Cree's production test fixture. This fixture is designed for high volume test at 2.7 GHz

[4] Single Carrier WCDMA, 3GPP Test Model 1, 64 DPCH, 45% Clipping, PAR = 7.5 dB @ 0.01% Probability on CCDF

[5] Includes package and internal matching components

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Typical Performance in CGH27030S-TB1

Figure 1. - Small Signal Gain and Return Losses vs Frequency
V_{DD} = 28 V, I_{DQ} = 0.20 A

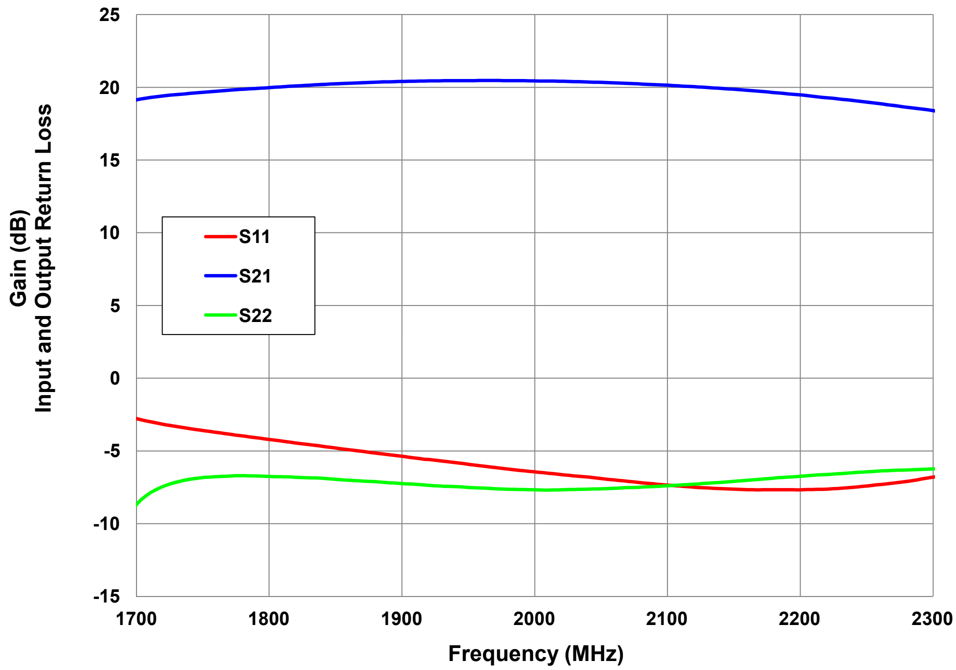
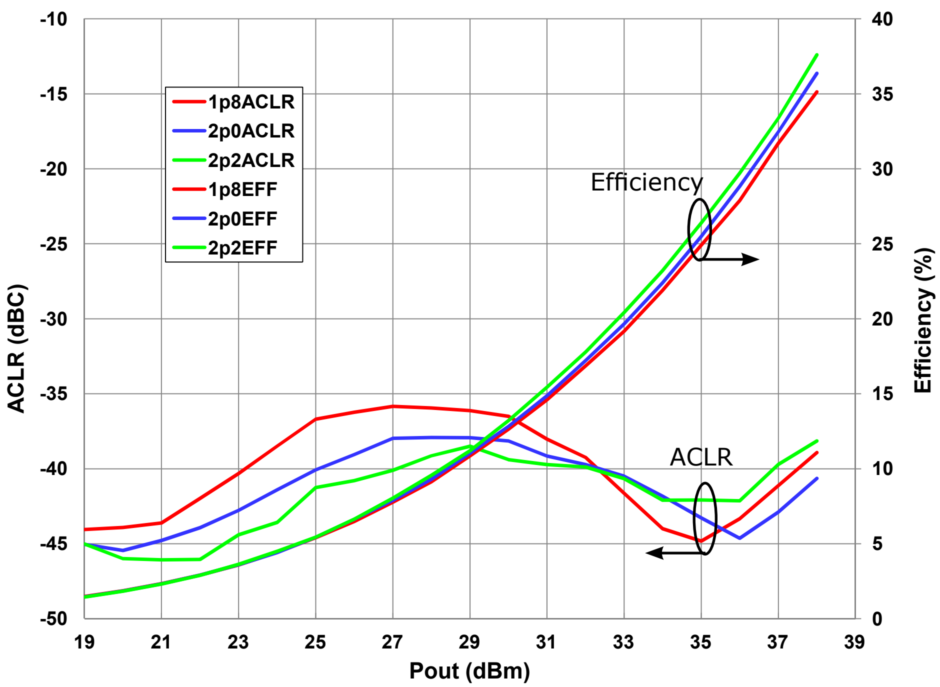


Figure 2. - Typical Drain Efficiency and ACLR vs. Output Power
V_{DD} = 28 V, I_{DQ} = 0.20 A, 1c WCDMA, PAR = 7.5 dB



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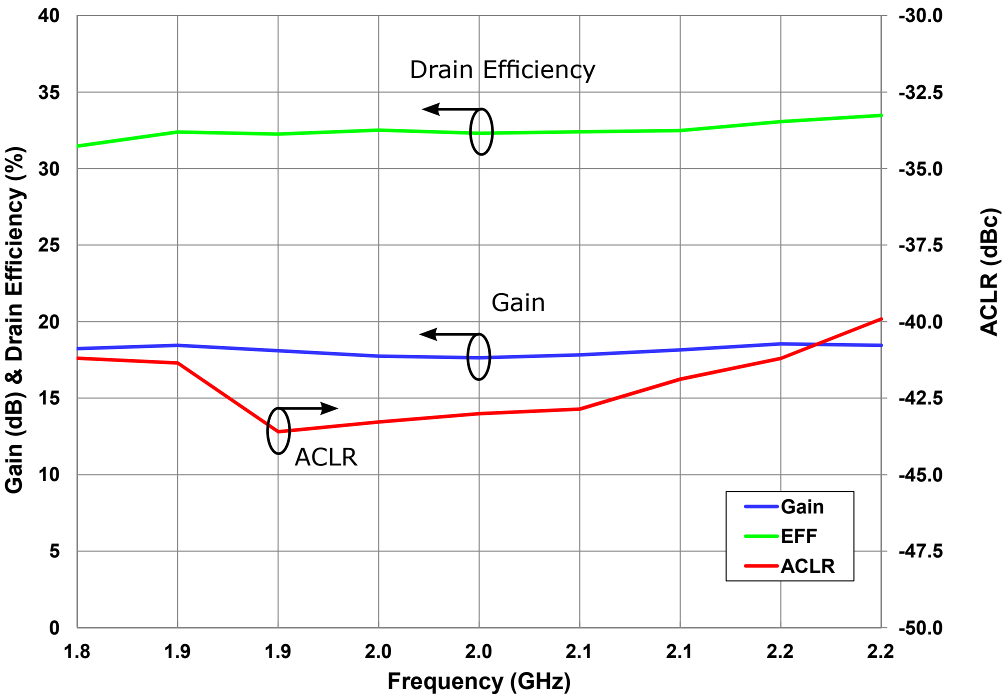
Typical Performance in CGH27030S-TB1

Figure 3. - Typical Gain, Drain Efficiency and ACLR vs Frequency
V_{DD} = 28 V, I_{DQ} = 0.20 A, P_{AVE} = 5 W, 1c WCDMA, PAR = 7.5 dB



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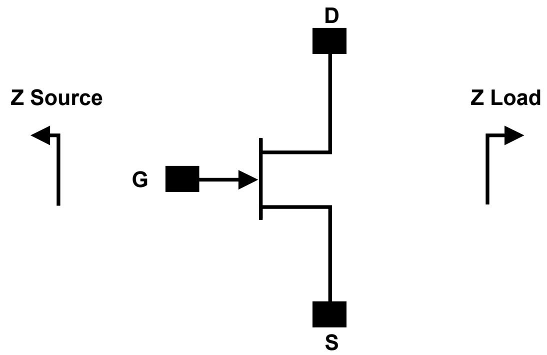
Source and Load Impedances for Application Circuit CGH27030S-TB1



Frequency (MHz)	Z Source	Z Load
1800	3.2 - j1.6	11 + j0.2
2000	3.6 - j0.6	10.5 + j1.8
2200	3.3 - j0.1	11 + j3.3

Note[1]: V_{DD} = 28 V, I_{DQ} = 0.20 A in the DFN package.
Note[2]: Impedances are extracted from the CGH27030S-TB1 application circuit and are not source and load pull data derived from the transistor.

CGH27030S-TB1 Application Circuit Bill of Materials

Designator	Description	Qty
R1	RES, 1/16 W, 0603, 1%, 100 OHMS	1
R2	RES, 1/16 W, 0603, 1%, 5.1 OHMS	1
C1	CAP, 6.8 pF, ±0.25 pF, 0603, ATC	1
C2	CAP, 2.4 pF, ±0.01 pF, 0603, ATC	1
C3, C8, C9, C10	CAP, 10.0 pF, ±0.5 pF, 0603, ATC	3
C12	CAP, 100.0 pF, 5%, 0603, ATC	1
C5	CAP, 470 pF, 5%, 100 V, 0603	1
C6, C13	CAP, 33000 pF, 0805, 10%, 100 V, X7R	2
C14	CAP, 1.0 UF, 100 V, 10%, X7R, 1210	1
C7	CAP, 10 UF, 16 V, TANTALUM	1
C15	CAP, 33 UF, 20%, G CASE	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST	2
Q1	CGH27030S, QFN	1

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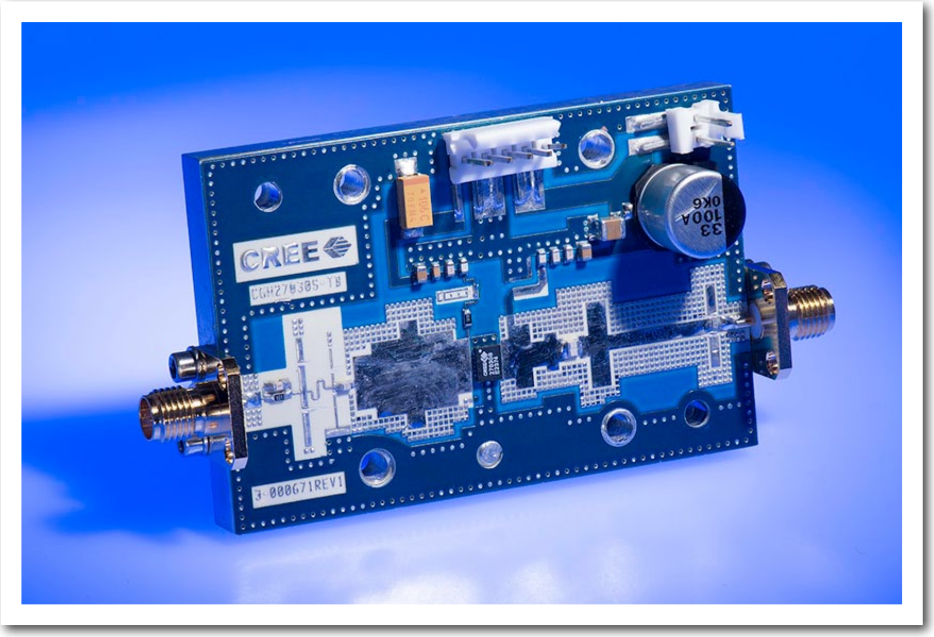
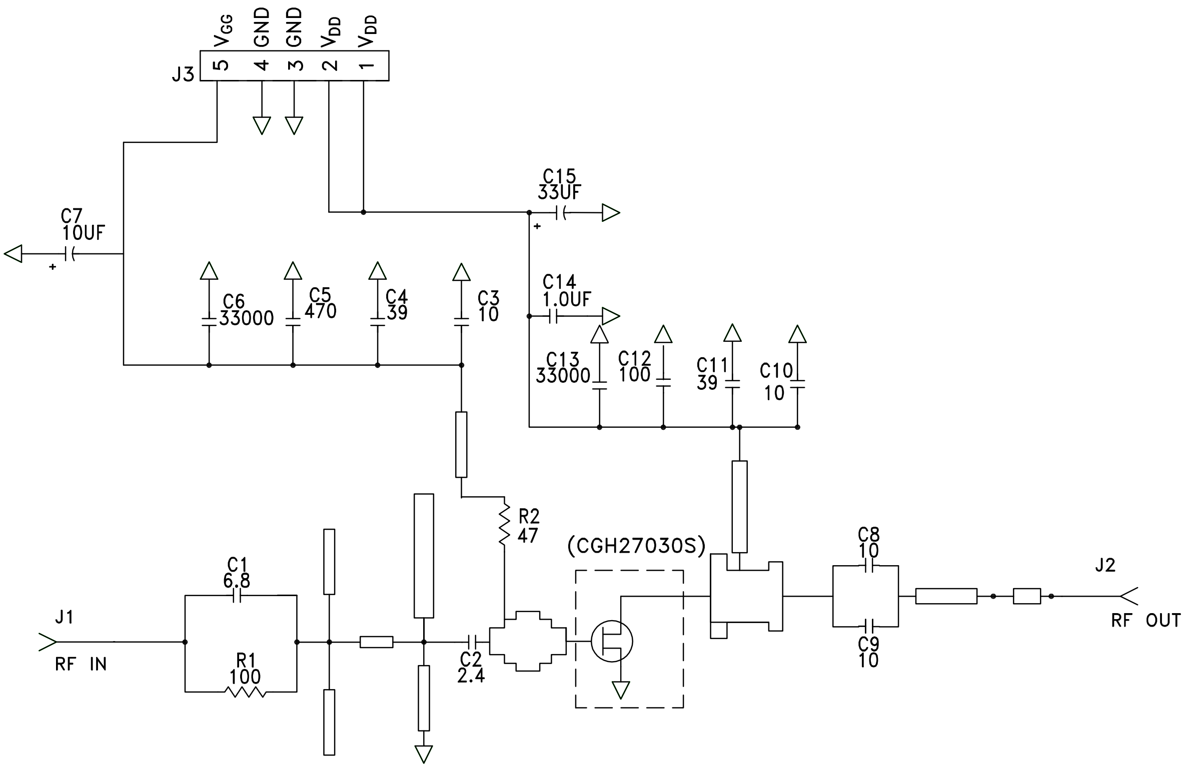
CGH27030S-TB1 Application Circuit, 28 V, 1.8-2.2 GHz



CGH27030S-TB1 Application Circuit Schematic, 28 V, 1.8-2.2 GHz



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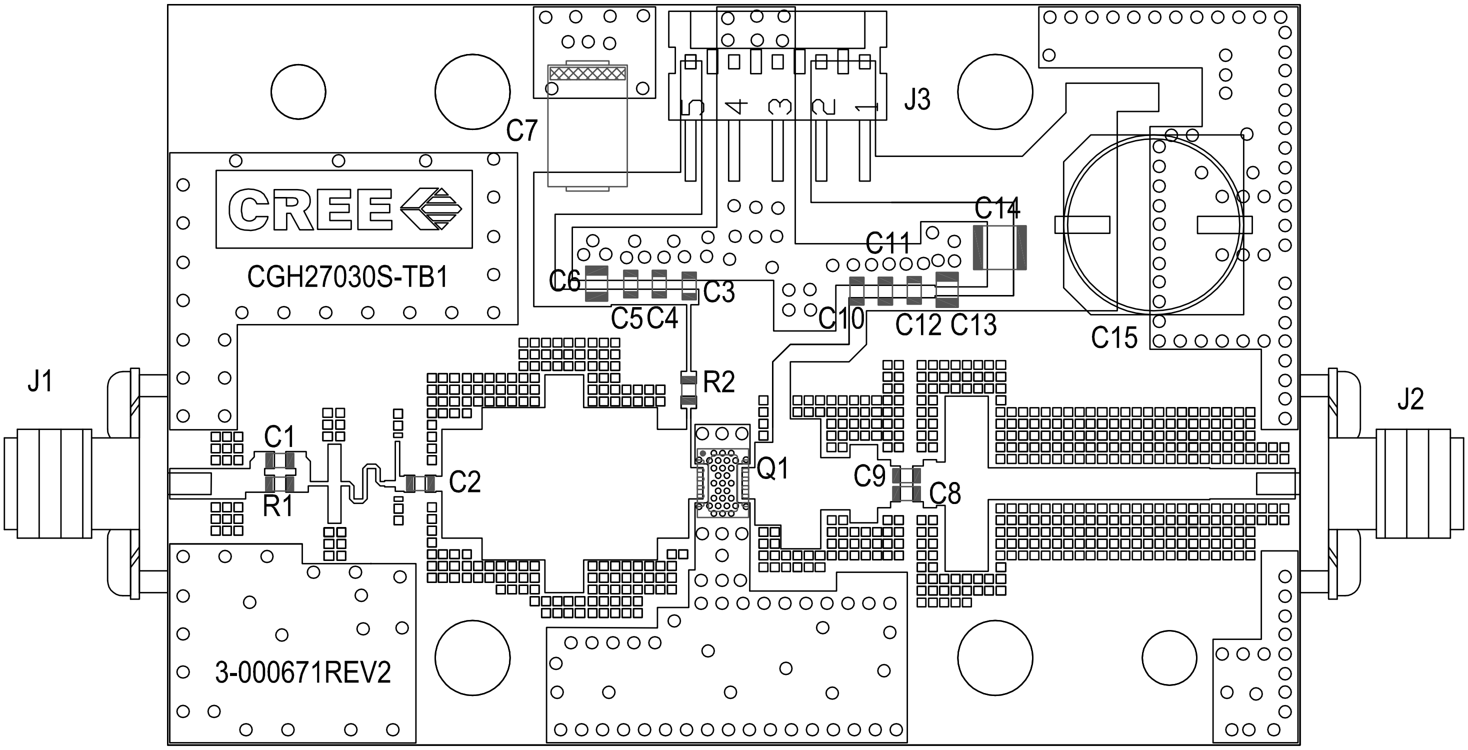
CGH27030S-TB1 Application Circuit, 28 V, 1.8-2.2 GHz



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Typical Performance in Application Circuit CGH27030S-TB2

Figure 4. - Small Signal Gain and Return Losses vs Frequency
V_{DD} = 28 V, I_{DQ} = 0.20 A

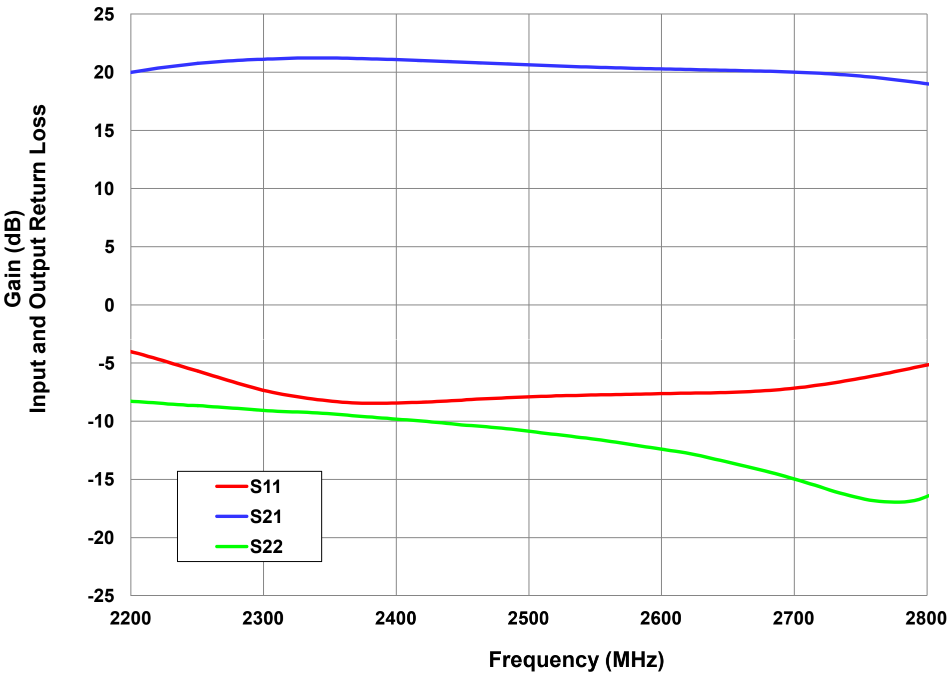
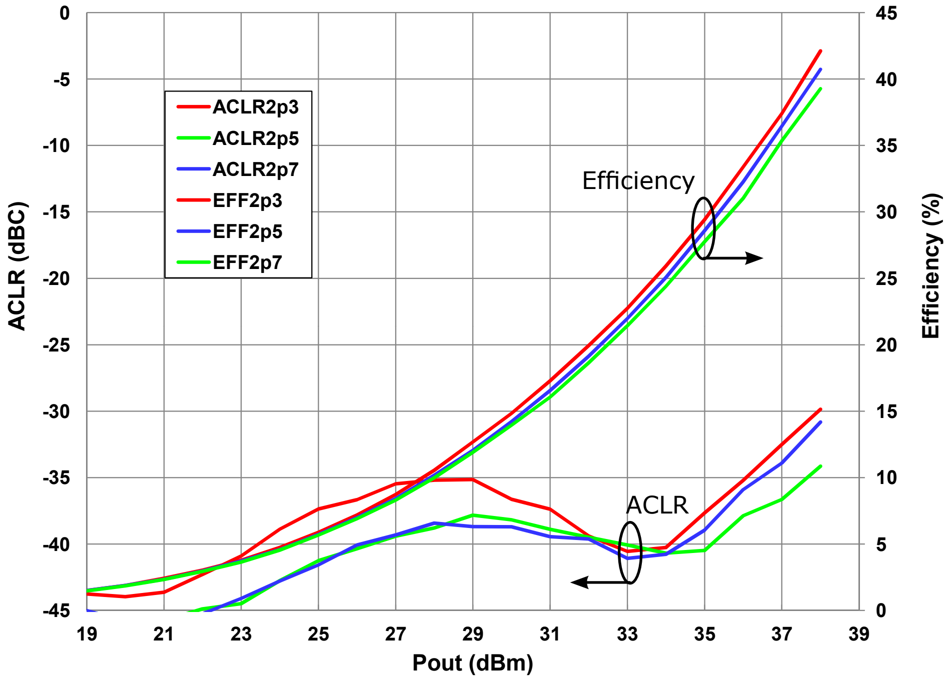


Figure 5. - Typical Drain Efficiency and ACLR vs. Output Power
V_{DD} = 28 V, I_{DQ} = 0.20 A, 1c WCDMA, PAR = 7.5 dB



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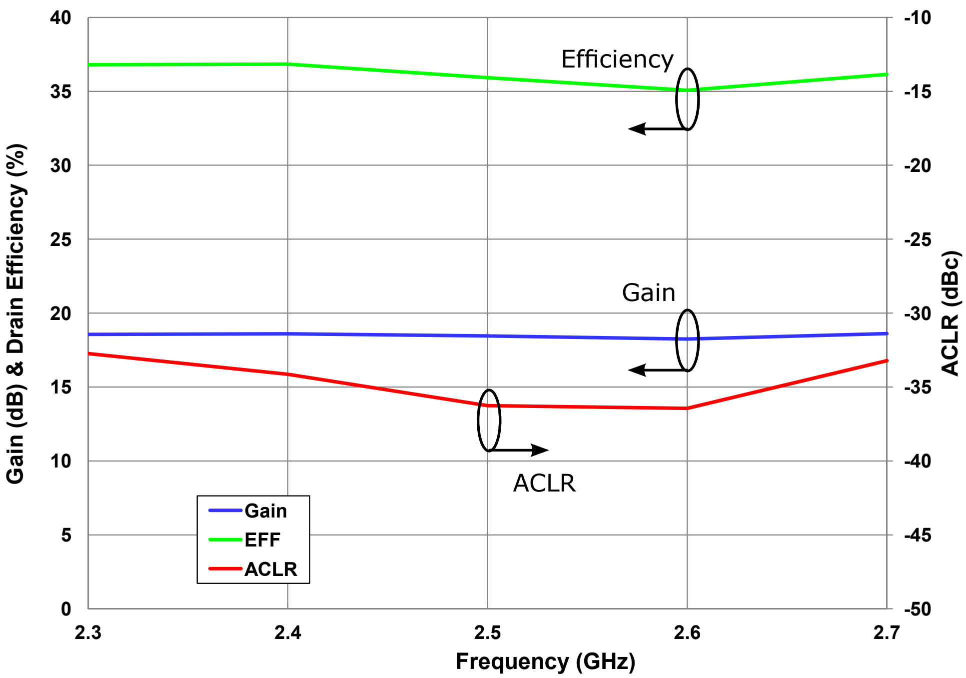
Typical Performance in Application Circuit CGH27030S-TB2

Figure 6. - Typical Gain, Drain Efficiency and ACLR vs Frequency
V_{DD} = 28 V, I_{DQ} = 0.20 A, P_{AVE} = 5 W, 1c WCDMA, PAR = 7.5 dB



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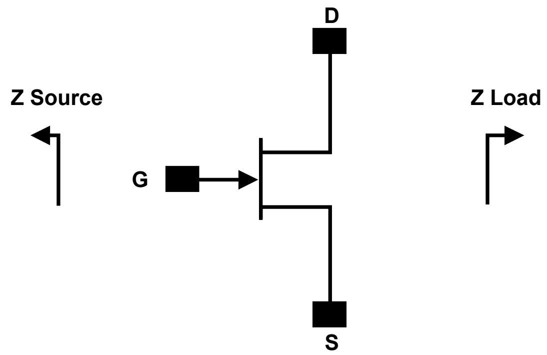
Source and Load Impedances for Application Circuit CGH27030S-TB2



Frequency (MHz)	Z Source	Z Load
2300	1.7 - j0.5	7.7 + j7.7
2500	2.2 - j0.2	8.0 + j6.8
2700	1.5 - j0.1	6.6 + j6.3

Note[1]: V_{DD} = 28 V, I_{DQ} = 0.20 A in the DFN package.
Note[2]: Impedances are extracted from the CGH27030S-TB2 application circuit and are not source and load pull data derived from the transistor.

CGH27030S-TB2 Application Circuit Bill of Materials

Designator	Description	Qty
R1, R2	RES, 22.6, OHM, +/-1%, 1/16W, 0603	2
C1	CAP, 3.3 pF, ±0.1 pF, 0603, ATC	1
C2	CAP, 0.9 pF, ±0.1 pF, 0603, ATC	1
C3	CAP, 1.2 pF, ±0.1 pF, 0603, ATC	1
C4	CAP, 1.5 pF, ±0.1 pF, 0603, ATC	1
C5, C9	CAP, 8.2 pF, ±0.25 pF, 0603, ATC	2
C6, C10	CAP, 470 pF, 5%, 100 V, 0603, X	2
C7, C11	CAP, 33000 pF, 0805, 100 V, X7R	2
C12	CAP, 1.0 UF, 100 V, 10%, X7R, 1210	1
C8	CAP, 10 UF 16 V TANTALUM	1
C14	CAP, 27 pF, ±5%, 0603, ATC	1
C13	CAP, 33 UF, 20%, G CASE	1
J1, J2	CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST	1
Q1	CGH27030S, QFN	2

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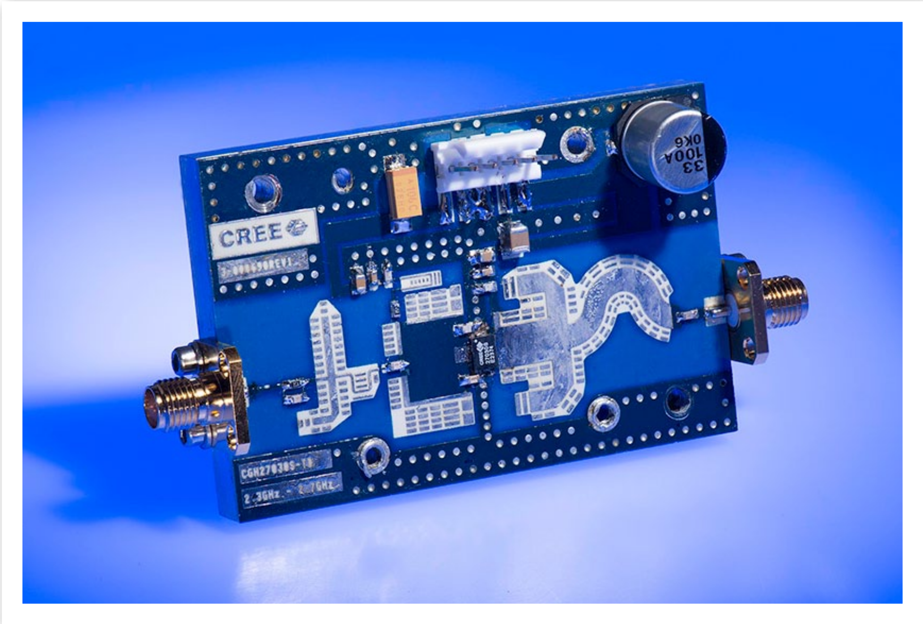
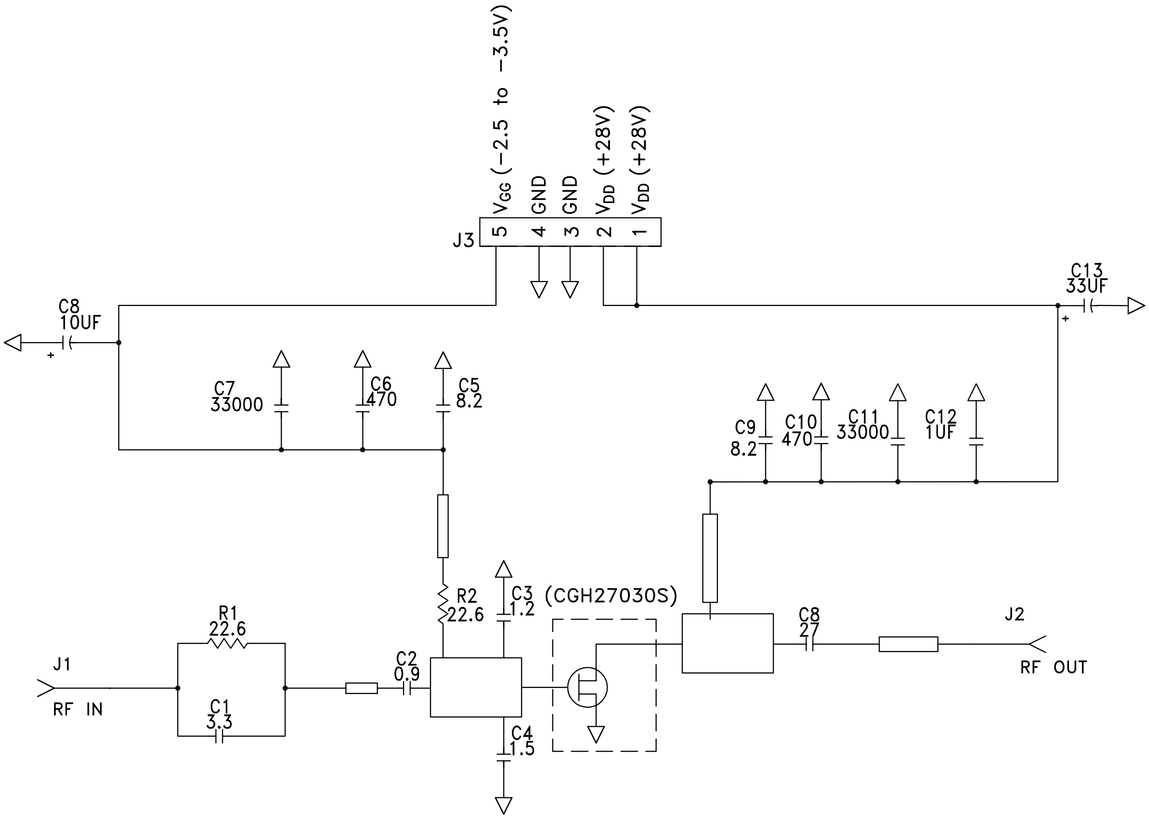
CGH27030S-TB2 Application Circuit, 28 V, 2.3-2.7 GHz



CGH27030S-TB2 Application Circuit Schematic, 28 V, 2.3-2.7 GHz



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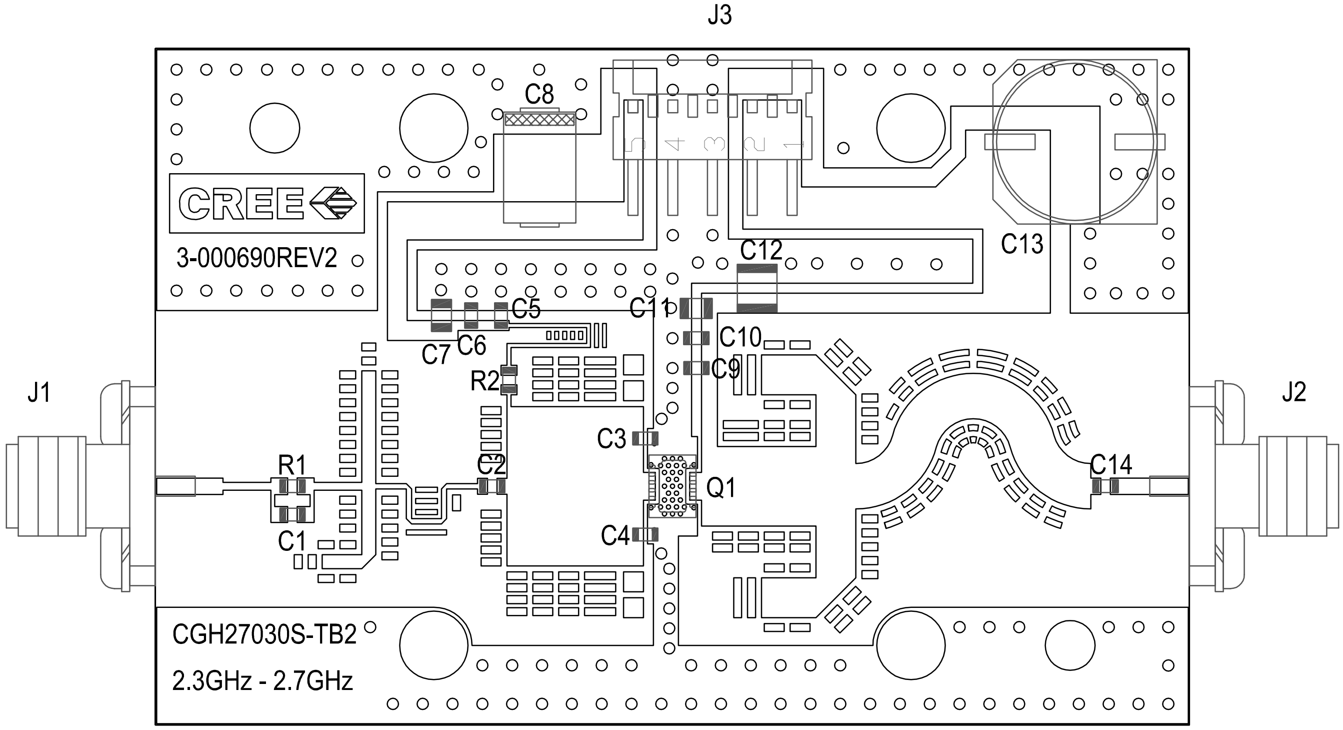
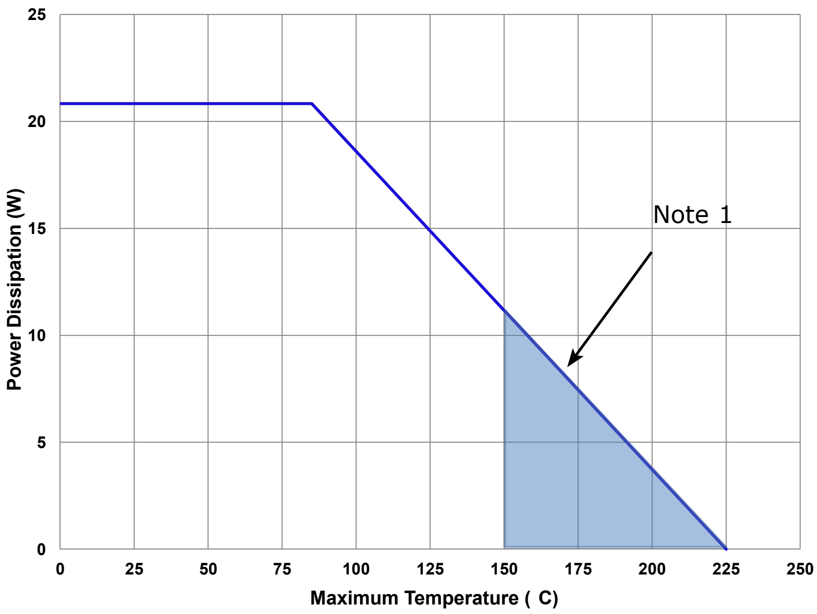
CGH27030S-TB2 Application Circuit, 28 V, 2.3-2.7 GHz



CGH27030S Power Dissipation De-rating Curve

Figure 7. - CGH27030S Transient Power Dissipation De-Rating Curve



Note 1. Area exceeds Maximum Case Temperature (See Page 2)

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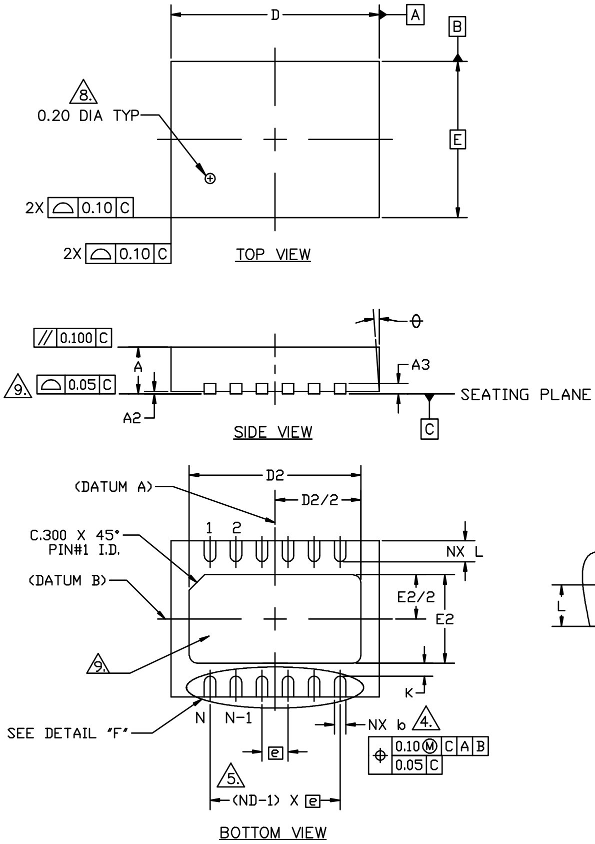
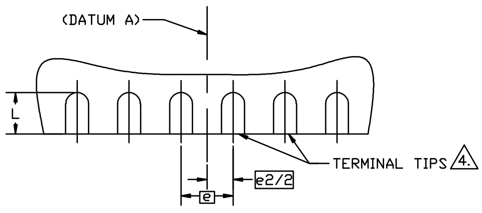
Product Dimensions CGH27030S (Package 3 x 4 DFN)



NOTES :

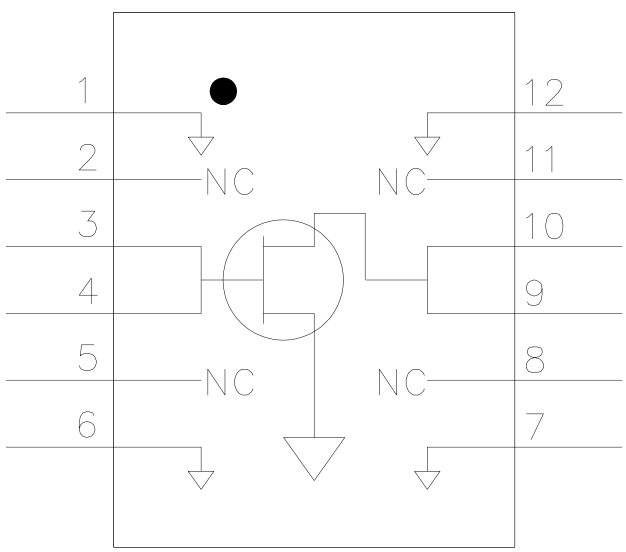
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN .15 AND .30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE
6. MAXIMUM PACKAGE WARPAGE IS .05 mm.
7. MAXIMUM ALLOWABLE BURRS IS .076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.



EVEN TERMINALS
DETAIL "F"
SCALE: 2:1

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3		0.203 REF.		
θ	0	—	12	2
D		4.00 BSC		
E		3.00 BSC		
e		0.50 BSC		
N		6		3
ND		12		5
L	0.35	0.40	0.45	
b	0.17	0.22	0.27	4
D2	3.20	3.30	3.40	
E2	1.60	1.7	1.80	
K	0.20	—	—	

Pin	Input/Output
1	GND
2	RF IN
3	RF IN
4	RF IN
5	RF IN
6	GND
7	GND
8	RF OUT
9	RF OUT
10	RF OUT
11	RF OUT
12	GND



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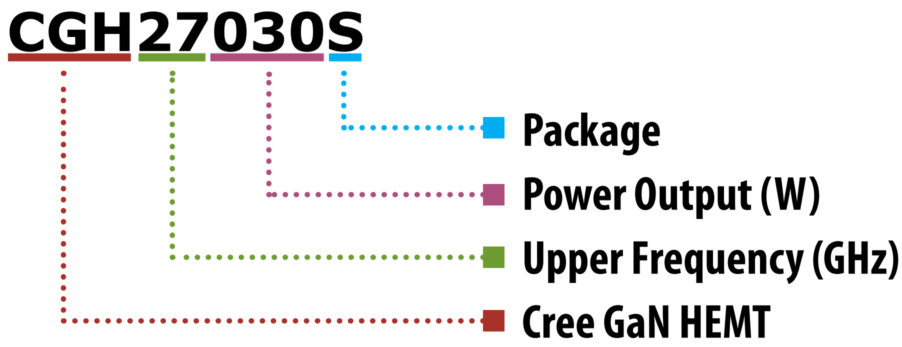
Part Number System



Parameter	Value	Units
Upper Frequency[1]	2.7	GHz
Power Output	30	W
Package	Surface Mount	-

Table 1.

Note[1]: Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples:	1A = 10.0 GHz 2H = 27.0 GHz

Table 2.

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