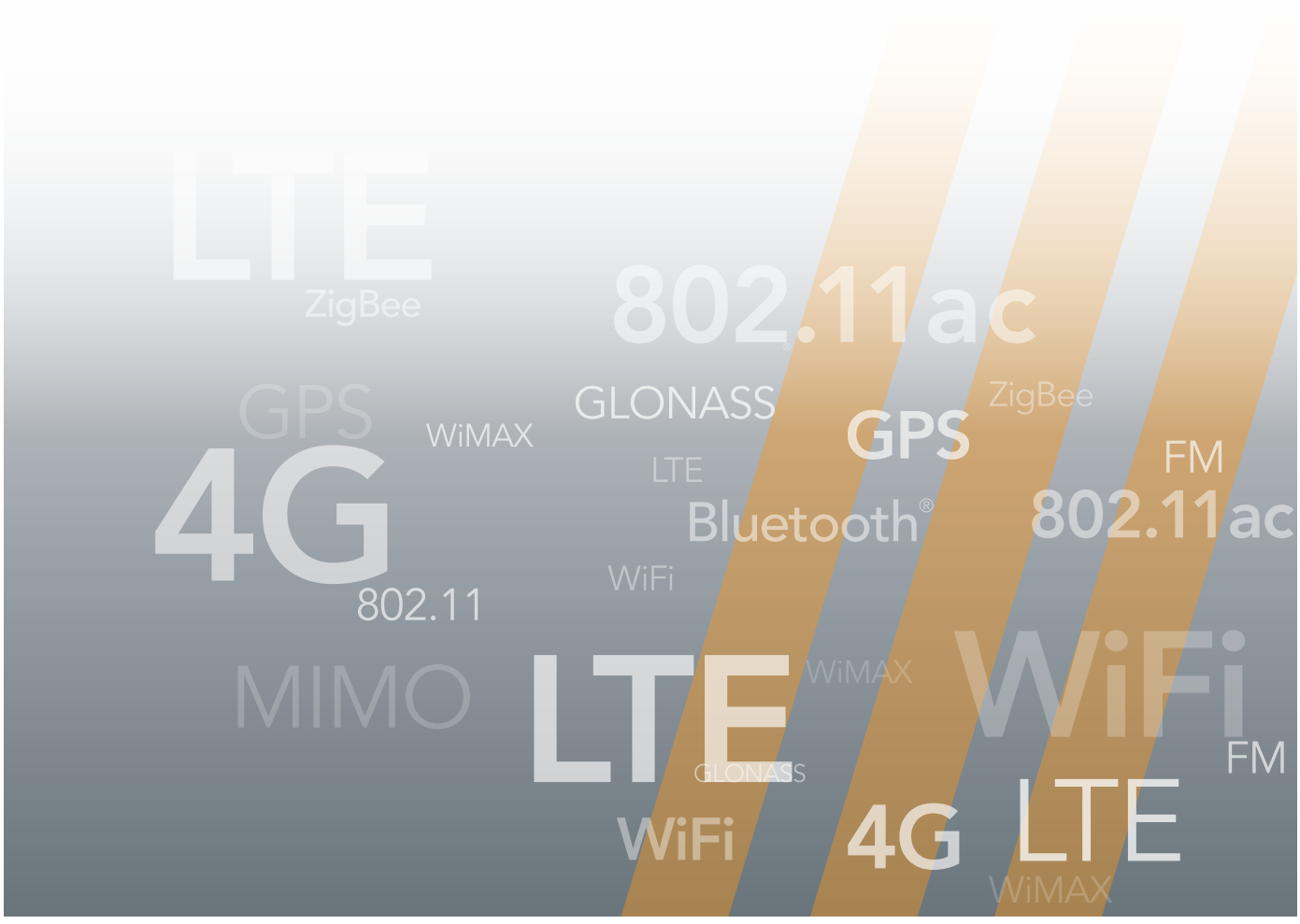
z5211

TECHNICAL SPECIFICATIONS

z5211
Waveform Generator
PXI, PXIe



LITEPOINT

Port Descriptions

Front Panel

Label	Type	Description
CH1 CH2	BNC	Channel *N* output
POD 1 POD 2	Custom	Channel *N* accessory connector
EXT IN	SMB (PXI/PXIe)	External input for trigger or reference
EXT OUT	SMB (PXI/PXIe)	External output for trigger, reference or event

Outputs

Specification	Value
Channels	2 Analog Outputs
Connectors	BNC
Analog Bandwidth	DC to 10 MHz (±0.1 dB Passband flatness) DC to 25 MHz (-1 dB bandwidth) DC to 50 MHz (-3 dB bandwidth)
Lowpass Filters	50 MHz, 5-pole Bessel 10 MHz, 5-pole Bessel 1 MHz, 5-pole Bessel 100 kHz, 5-pole Bessel
Slew Rate[1]	> 2 kV/µs into 50 Ω (50 MHz filter)
Rise/Fall Time	<7 ns for 10 V step into 50 Ω (50 MHz filter)
Range Adjust[2] Into 50 Ω Into High Impedance	 7.5 mVpp to 14 Vpp 15 mVpp to 28 Vpp Range independently adjustable for each output channel
DC Offset Adjust Into 50 Ω Into High Impedance	 ≤ ±7 V ≤ ±14 V
Output Voltage Limit[3] Into 50 Ω Into High Impedance	 $\lvert V_{AMP} + V_{OFFS} \rvert \leq 7$ V $\lvert V_{AMP} + V_{OFFS} \rvert \leq 14$ V
Output Current Limit	±140 mA recommended operating maximum ±350 mA short circuit maximum
Range Resolution[4]	0.5 mVpp
Range Accuracy[4] (25°C ambient)	< ±(0.5% of range + 10 mVpp)
Range Drift[4]	< ±1.5 mVpp per °C
Output Impedance	50 Ω typical

[1] Harmonic distortion increases for range/bandwidth combinations above 400 Vpp-MHz

[2] Full-scale range adjustment preserves function generator 14-bit DAC resolution and dynamic range

[3] V_{AMP} = range/2, V_{OFFS} = DC offset

[4] Specification shown for high-impedance load; divide specifications by 2 for 50 Ω load

Digital-to-Analog Converter (DAC)

DAC Resolution & Ranges

Range (Vpp) High Impedance/No Load	Range (Vpp) 50 Ω Load	DAC Resolution
28.0 to 1.0	14.0 to 0.5	14 bits
0.9995 to 0.5	0.4995 to 0.25	13 bits
0.4995 to 0.25	0.2495 to 0.125	12 bits
0.2495 to 0.125	0.1245 to 0.0625	11 bits
0.1245 to 0.0625	0.062 to 0.031	10 bits
0.062 to 0.031	0.0305 to 0.0155	9 bits
0.0305 to 0.015	0.015 to 0.0075	8 bits

Specification	Value
DAC Resolution	14 bits (0.0061% of full-scale range)
Waveform Length	4 Samples to 32 MiSamples per channel
DAC Clock	DAC sample clocks generated by Direct Digital Synthesizers. All channels have independent or common DAC sample clocks.
DAC Clock Rate	200 Samples/s to 200 MSamples/s
DAC Clock Resolution	< 0.01 ppm or > 8 digits (i.e. 0.116 Hz from 20 MS/s to 200 MS/s)
DAC Clock Sweep	Swept DAC clock rate: linear or log sweep See Sweep Mode for additional details
DAC Clock Output	External Output: 100 Hz to 100 MHz common clock source
DAC Clock Jitter	< 20 ps
Channel-to-Channel Skew	< 500 ps (50 MHz filter)
Channel-to-Channel Isolation	≥60 dB
RMS Noise (with DAC clock above filter cutoff)	≤ 1mV into 50 Ω (50 MHz filter)

Spectral Purity (sine)

Output Level	Output Frequency	Harmonic	Non-Harmonic
≤ +20 dBm	100 kHz	< -73 dBc	< -52 dBc
	20 MHz	< -50 dBc	< -52 dBc
	50 MHz	< -38 dBc	< -52 dBc
> +20 dBm	100 kHz	< -70 dBc	< -52 dBc
	20 MHz	< -30 dBc	< -52 dBc
	50 MHz	< -20 dBc	< -52 dBc

Horizontal

Specification	Value
Timebase Reference	10 MHz
Timebase Reference Source	Internal TCXO, External Input, Backplane (PXI/PXIe)
Internal TCXO Timebase	±2.5 ppm accuracy
Timebase Output	External Output

Operation Modes

Continuous Mode

Specification	Value
Functionality	Generate output continuously when initiated

Burst Mode

Specification	Value
Functionality	Generate a discrete number of cycles upon trigger event
Number of Cycles	1 to 65535, programmable A cycle is one waveform period, or one arbitrary waveform sequence

Binary Modulation Mode

Specification	Value
Functionality	Toggle between two preloaded waveforms based upon modulation state. Enables Amplitude, Phase, Frequency Shift Keying, or Gated Output
Modulation Source	External Input, Bus Trigger 0-7, Star Trigger (PXI/PXIe), Internal Trigger, Software

Sweep Mode

Specification	Value
Functionality	Sweeps DAC clock rate for swept output signal frequency Programmable start frequency & stop frequency Programmable up, down, or up & down modes
Sweep Types	Linear or Logarithmic
Sweep Range	1000:1 maximum sweep frequency range (start-to-stop ratio)
Sweep Time	1 ms to 100 s sweep time programmable 1 µs resolution

Trigger

Specification	Value
Trigger Source	External Input, Pattern, Software, TTL Trigger 0-7, Star Trigger, Internal Trigger
Trigger Slope/Polarity	Positive or Negative
Trigger Modes	Edge, Pattern
Pattern Trigger Mode	Pattern match true or false
Pattern Sources	External Input, TTL Trigger 0-7, Star Trigger
Trigger Delay	Programmable delay after trigger event before start of waveform 0 to 6.5535 ms programmable 100 ns resolution
Trigger Latency	< (20 DAC clock periods + 100 ns)
Trigger Detection Jitter	±½ DAC clock period
Internal Trigger	Programmable internal trigger source, 1 µs to 100 s period 100 ns resolution
Trigger Timestamp	100 ns resolution, 1 second rollover

Arm

Specification	Value
Functionality	Arm to qualify Trigger Event
Source	External Input, TTL Trigger 0-7, Star Trigger, Software
Polarity	Positive or Negative

External Input (front panel)

Specification	Value
Functionality	Trigger Input, Timebase Reference Input, External Arm, External Modulation Input
Absolute Maximum Input (no damage)	≤ ± 5 V (DC + peak AC), CAT I
Input Trigger Level Adjustment	-2 V to +2 V 0.5 mV resolution ≤ 20 mV accuracy 20 mV overdrive (input hysteresis)
Input Bandwidth (-3 dB)	≥ 250 MHz
Input Impedance	1 MΩ ‖ 30 pF or 50 Ω ≤ ±2% accuracy
Connector	SMB

Sync Outputs

Specification	Value
Channels	2
Outputs	External Output, Bus Trigger 0-7
Time Resolution	5 ns to 500 µs (200 MHz to 2 kHz) Synchronized to DAC clock
Polarity	Programmable high or low pulses
Timing	Programmable location and width (in DAC clock samples)

External Output (front panel)

Specification	Value
Functionality	Sync Output, Trigger Output, Timebase Reference Output, Common DAC Clock/2 Output, Event Output, Programmable Clock Output, Programmable Pulse Output, Constant Level
Output Event Source	Arm Event, Trigger Event, Generation Complete Event, Operation Complete Event, Master Summary Status Event
Polarity	High or Low Truth
Programmable Event Pulse Width	20 ns to 163 ms 10 ns resolution
Programmable Clock	Period: 26.667 ns to 100 seconds 50% Duty Cycle
Programmable Pulse Pulse Repetition Interval Pulse Width	 26.667 ns to 100 seconds 16.667 ns
Output Level	TTL Compatible into ≥ 200 Ω ≥ ±24 mA Output Drive
Common DAC Clock/2	Half the common DAC sample clock 100 Hz to 100 MHz
Output Enable	Tri-State Output Capability
Connector	SMB

Backplane Triggers

Specification	Value
Functionality	Multi-Instrument Synchronization Trigger, Event Output Signals
Triggers	TTL Trigger 0-7
Direction	Input or Output
Source	Arm Event, Trigger Event, Generation Complete Event, Operation Complete Event, Master Summary Status Event, Constant Level
Polarity	High or Low Truth
Programmable Event Pulse Width	20 ns to 163 ms 10 ns resolution

Standard Functions

Sine

Specification	Value
Frequency	0.001 Hz to 50 MHz
Initial Phase	0° to 360°

Square

Specification	Value
Frequency	0.001 Hz to 20 MHz
Duty Cycle	0 to 100%
Initial Phase	0° to 360°

Triangle

Specification	Value
Frequency	0.001 Hz to 20 MHz
Initial Phase	0° to 360°

Ramp (Sawtooth)

Specification	Value
Frequency	0.001 Hz to 20 MHz
Initial Phase	0° to 360°
Shape	Ramp Up or Down

DC

Specification	Value
Amplitude	±100% of Maximum Range

Haversine

Specification	Value
Frequency	0.001 Hz to 50 MHz
Initial Phase	0° to 360°

Havercosine

Specification	Value
Frequency	0.001 Hz to 50 MHz
Initial Phase	0° to 360°

Half Cycle Sine

Specification	Value
Frequency	0.001 Hz to 50 MHz
Initial Phase	0° to 360°

Pulse

Specification	Value
Frequency	0.001 Hz to 20 MHz
Pulse Width	0 to (Period – 1 Data Clock cycle)
Rise/Fall Time	(1 Data Clock cycle) to (Period – 2 Data Clock cycles)
Initial Delay	0 to (Period – 2 Data Clock cycles)

Sinc Pulse

Specification	Value
Frequency	0.001 Hz to 50 MHz
Sinc Frequency	Frequency to 50 MHz
Initial Phase	0° to 360°

Gaussian Pulse

Specification	Value
Frequency	0.001 Hz to 50 MHz
Standard Deviation	(1 Data Clock cycle) to (Period/2)
Initial Phase	0° to 360°

Lorentz Pulse

Specification	Value
Frequency	0.001 Hz to 50 MHz
Half Width	(1 Data Clock cycle) to (Period/2)
Initial Phase	0° to 360°

Noise

Specification	Value
Period	1 µs to 1000 s
Noise Type	Uniform White

AM

Specification	Value
Center Frequency	100 Hz to 50 MHz
Modulation Source	Internal
Modulation Frequency	1 Hz to smaller of 1 MHz or Center Frequency
Modulation Depth	0 to 100%
Modulation Shape	Sine, Square, Triangle, Ramp Up, Ramp Down

FM

Specification	Value
Center Frequency	100 Hz to 50 MHz
Modulation Source	Internal
Modulation Frequency	1 Hz to smaller of 1 MHz or Center Frequency
Frequency Deviation	1 Hz to smaller of 1 MHz or Center Frequency
Modulation Shape	Sine, Square, Triangle, Ramp Up, Ramp Down

Multi-Tone

Specification	Value
Frequencies	100 Hz to 50 MHz
Tone Resolution	100 Hz minimum
Number of Tones	1 to 16

Serial Data

Specification	Value
Bit Rate Frequency	0.001 Hz to 20 MHz
Word Length	4 to 64 bits

Arbitrary Waveforms

Specification	Value
Functionality	DAC Sample-by-Sample arbitrary Waveform Synthesis

Waveform Sequences

Specification	Value
Sequence	Predefines up to 8 sequences of arbitrary waveforms 2 to 4,096 waveform stages in sequence Each waveform repeated 1 to 65535 times within stage Waveform stages from waveform library and reference channels Each waveform stage has unique waveform handle and loop number Amplitude, offset and DAC sample rate apply to entire sequence
Waveform Library	Predefined set of arbitrary waveforms Up to 4,096 waveforms in waveform library Total arbitrary waveform library memory limited to 8 MiSamples (16 MiB)

Reference Channels

Specification	Value
Reference Channels	Quantity 4
Reference Storage	Non-volatile memory storage
Reference Data	32 KiSample maximum waveform size 32-bit resolution

Waveform Operations

Specification	Value
Upload	Waveform memory written by host Ping-pong buffers enable upload during active waveform generation
Download	Waveform memory read by host
Copy	Waveform memory copied front one location or type to another
Invert	Waveform DAC codes inverted (2s compliment)
Scale	Waveform DAC codes linearly adjusted by scale factor
Waveform Data Formats	16-bit signed integer 32-bit floating point Intel or Motorola Byte Order

Instrument Stored States

Specification	Value
Functionality	Non-volatile storage of instrument setup configuration
Stored States	14 State 0 is Reset State Power-On State programmable

LED Indicators

Specification	Value
RDY (Ready)	OFF: Hardware Failure ON: Unit has passed power-up self-diagnostics TOGGLE: Unit has an error pending in error queue
HST/LAN (Host)	OFF: Interface fault ON: Normal interface operation TOGGLE: Device identify enabled
TRG (Trigger)	OFF: Trigger event not detected ON/PULSE: Trigger complete event detected
ACT (Active)	OFF: Instrument Idle ON/PULSE: Waveform generation initiated

PXI Interface

Specification	Value
PXI Slot Compatibility	PXI Standard Slot and PXIe Hybrid Slot Compatible
PXI Timing & Triggering Signals (XJ4 Connector)	PXI_TRIG[0:7] input/output PXI_STAR input PXI_CLK10 input

PXIe Interface

Specification	Value
PXIe Slot Compatibility	PXI Standard Slot and PXIe Hybrid Slot Compatible
PXI Timing & Triggering Signals (XJ4 Connector)	PXI_TRIG[0:7] input/output PXI_STAR input PXI_CLK10 input
PXIe Timing & Triggering Signals (XJ3 Connector)	PXI_DSTARA input (unused) PXI_STAR input PXI_CLK10 input

Status Reporting

Specification	Value
IEEE-488.2 Device Status	Reporting Structure including Status Byte, Standard Event Registers, Questionable Registers, Operation

Power & Cooling

Power Supplies

Model	Platform	Voltage	Typical Current	Maximum Current
z5211	PXI	+3.3 VDC +5 VDC +12 VDC -12 VDC	3.28 A 0.49 A 0.21 A 0.00 A	4.72 A 0.75 A 0.67 A 0.00 A
	PXIe	+3.3 VDC +5 VDC +12 VDC -12 VDC	3.28 A 0.49 A 0.21 A 0.00 A	4.72 A 0.75 A 0.67 A 0.00 A

Total Cooling & Power Consumption

Model	Platform	Typical Cooling & Power	Maximum Cooling & Power
z5211	PXI	15.8 W	27.5 W
	PXIe	15.8 W	27.5 W

Physical & Environmental

Size & Weight

Specification	Value
Physical Size	Single-Wide 3U PXI/PXIe Instrument 8.25" x 0.79" x 5.25" (L x W x H) 20.96 cm x 2.01 cm x 13.34 cm (L x W x H)
Weight	1 lb or 450 g

Temperature Range

Specification	Value
Operating	0°C to +50°C ambient
Storage	-40°C to +75°C
Over-Temperature	Automatic shutdown if internal temperature exceeds +65°C
Calibration Range	+20°C to +30°C ambient, after a 20 minute warm-up period, to meet all calibration specification accuracies

Relative Humidity

Specification	Value
Operating or Storage < +30 °C ≥ +30°C, ≤ +40 °C > 40 °C	 5 to 95% ± 5% non-condensing 5 to 75% ± 5% non-condensing 5 to 45% ± 5% non-condensing

Altitude

Specification	Value
Operating	Up to 5 km
Storage	Up to 15 km

Terminology

Numeric Prefixes

When referring to numeric values, this document will use SI (International System of Units) and IEC (International Electrotechnical Commission) standard prefixes. Prefix definitions are in the following table.

Prefix	Multiplier
n (nano)	1/(1000x1000x1000)
µ (micro)	1/(1000x1000)
m (milli)	1/1000
k/K (kilo)	1000
M (Mega)	1000x1000
G (Giga)	1000x1000x1000
Ki (Kibi)	1024
Mi (Mebi)	1024x1024
Gi (Gibi)	1024x1024x1024

Differential Outputs

Single-Ended is used to refer to the output on either the + or – output pin

Differential is used to refer to the output between the + and- output pins

Vd indicates Volts differential

Vppd indicates Volts peak-to-peak differential

Safety

This product is designed to meet the requirements of the following standard of safety for electrical equipment for measurement, control and laboratory use: EN 61010-1

Electromagnetic Compatibility

CE Marking EN 61326-1:1997 with A1:1998 and A2:2001 Compliant

FCC Part 15 (Class A) Compliant

Emissions

EN 55011	Radiated Emissions, ISM Group 1, Class A, distance 10 m, emissions < 1 GHz
EN 55011	Conducted Emissions, Class A, emissions < 30 MHz Immunity
EN 61000-4-2	Electrostatic Discharge (ESD), 4 kV by Contact, 8 kV by Air
EN 61000-4-3	RF Radiated Susceptibility, 10 V/m
EN 61000-4-4	Electrical Fast Transient Burst (EFTB), 2 kV AC Power Lines
EN 61000-4-5	Surge
EN 61000-4-6	Conducted Immunity
EN 61000-4-8	Power Frequency Magnetic Field, 30 A/m
EN 61000-4-11	Voltage Dips and Interrupts

CE Compliance

This product meets the necessary requirements of applicable European Directives for CE Marking as follows:

73/23/EEC Low Voltage Directive (Safety)
89/336/EEC Electromagnetic Compatibility Directive (EMC)

See Declaration of Conformity for this product for additional regulatory compliance information.

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