Low Jitter LVPECL Clock Oscillator

PURE SPECTRUM

CONNOR WINFIELD

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Description:

The Connor-Winfield PBxxx series are 5.0x7.0mm Surface Mount, LVPECL output logic, Fixed Frequency Crystal Controlled Oscillator (XO) designed for applications requiring tight frequency stability, wide temperature range with very low jitter. Operating at 3.3V supply voltage, the PBxxx series provides LVPECL Differential Outputs with enable / disable function. The surface mount package is designed for high-density mounting and is optimum for mass production.

Features:

Model PBxxx - Series
5 x 7mm Surface Mount Package
3.3 Vdc Operation
LVPECL Differential Outputs
Frequency Stabilities Available:
+/-20 ppm,+/-25 ppm, +/-50 ppm or +/-100 ppm
Temperature Ranges Available:
0 to 70°C, -40 to 85°C, 0 to 85°C or -20 to 70°C
Low Jitter <0.1ps RMS
Tri-State Enable/Disable on Pad 1
Tape and Reel Packaging
RoHS Compliant / Lead Free ✓RoHS

Applications:

40GB Ethernet and 100GB Ethernet reference clocks.
Fiber channel
High speed Data conversion, ADC, DAC
Storage Area Networks, SANs

Absolute Maximum Ratings

Parameter	Minimum	Nominal	Maximum	Units	Notes
Storage Temperature	-55	-	125	°C	
Supply Voltage (Vcc)	-0.5	-	4.6	Vdc	
Input Voltage	-0.5	-	Vcc + 0.5	Vdc	

Operating Specifications

Parameter	Minimum	Nominal	Maximum	Units	Notes
Output Frequency; (Fo)	125	-	170	MHz	
Total Frequency Tolerance	(See Ordering Information for full part number)				
Model PBx43	-20	-	20	ppm	1
Model PBx13	-25	-	25	ppm	1
Model PBx23	-50	-	50	ppm	1
Model PBx33	-100	-	100	ppm	1
Operating Temperature Range	(See Ordering Information for full part number)				
Model PB1x3	0	-	70	°C	
Model PB2x3	-40	-	85	°C	
Model PB3x3	0	-	85	°C	
Model PB4x3	-20	-	70	°C	
Freq. Stability vs. Supply Voltage Change:	-	±0.5	-	ppm	2
Supply Voltage: (Vcc)	3.135	3.3	3.465	Vdc	
Supply Current: (Icc)	-	40	50	mA	
Jitter:					
Period Jitter	-	3.0	5.0	ps RMS	
Integrated Phase Jitter (BW = 12 KHz to 20 MHz)	-	0.060	0.100	ps RMS	
SSB Phase Noise: Fo = 156.25 MHz					
@ 10 Hz offset	-	-64	-	dBc/Hz	
@ 100 Hz offset	-	-95	-	dBc/Hz	
@ 1 KHz offset	-	-126	-	dBc/Hz	
@ 10 KHz offset	-	-149	-	dBc/Hz	
@ 100 KHz offset	-	-159	-	dBc/Hz	
@ 1 MHz offset	-	-161	-	dBc/Hz	
Start-Up Time:	-	-	2	ms	

LVPECL Output Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Load:	-	50	-	Ohm	4
Output Voltage:					
(High) (Vcc = 3.3 V) (Voh)	2.275	-	-	V	
(Low) (Vcc = 3.3 V) (Vol)	-	-	1.680	V	
Duty Cycle: at 50% Level	45	50	55	%	5
Rise / Fall Time: 20% to 80%	-	0.3	1.0	ns	

Ordering Information

PB	2	2	3	- 156.25M
Type PB Series LVPECL Low Jitter Clock Series 5x7 mm	Temperature Range 1 = 0 to 70°C 2 = -40 to 85°C 3 = 0 to 85°C 4 = -20 to 70°C	Frequency Stability 4 = ±20 ppm 1 = ±25 ppm 2 = ±50 ppm 3 = ±100 ppm	Supply Voltage 3 = 3.3 Vdc, OE Pad 1	Output Frequency Frequency Format -xxx.xM Min -xxx.xxxxxxM Max *Amount of numbers after the decimal point. M = MHz

Example: Part Number
PB223-156.25M = LVPECL Output,-40 to 85, +/-20ppm, 3.3Vdc, OE Pad 1, Output Frequency 156.25 MHz

RoHS COMPLIANT

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OE Input Characteristics

Parameter	Minimum	Nominal	Maximum	Units	Notes
Enable Input Voltage: (High) (Vih)	90%Vcc	-	-	Vdc	3
Disable Input Voltage: (Low) (Vil)	-	-	10%Vcc	Vdc	3
Enable Time:	-	-	2	ms	
Disable Time:	-	-	200	ns	
Standby Current: (When Osc. is disabled)	-	12	-	mA	

Package Characteristics

Package:	Hermetically sealed ceramic package and metal cover

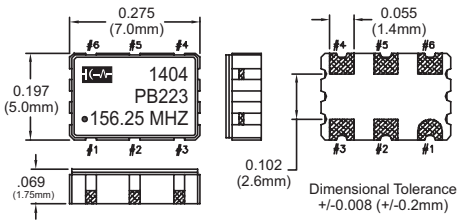
Environmental Characteristics

Vibration:	Vibration per Mil Std 883E Method 2007.3 Test Condition A.
Shock:	Mechanical Shock per Mil Std 883E Method 2002.4 Test Condition B.
Soldering Process;	RoHS compliant lead free. See soldering profile on page 2.

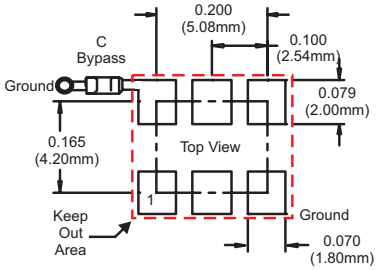
Notes:

1. *Includes calibration @ 25°C, frequency stability vs. change in temperature, supply voltage and load variations, shock and vibration and 20 years aging.*
2. *Frequency stability vs. change in supply voltage, Vcc±5% @ 25°C.*
3. *When the oscillator is disabled the outputs are at high impedance. Outputs are enabled with no connection on E/D pad.*
4. *Outputs must be terminated into 50 ohms to Vcc – 2V or Thevenin equivalent.*
5. *Duty cycle measured at 50% output voltage swing.*

Package Outline



Suggested Pad Layout



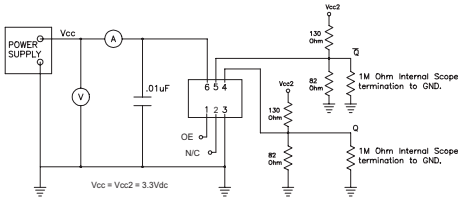
Pad Connections

1:	Enable / Disable (OE)
2:	N/C
3:	Ground
4:	Output Q
5:	Complementary Output $\overline{Q}$
6:	Supply Voltage (Vcc)

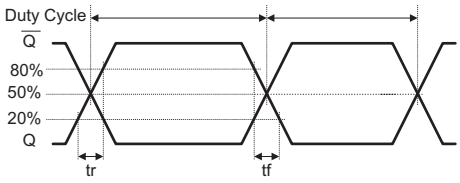
OE Enable / Disable Function

Function:	Output
Low:	Disabled (High Impedance)
High or Open:	Enabled

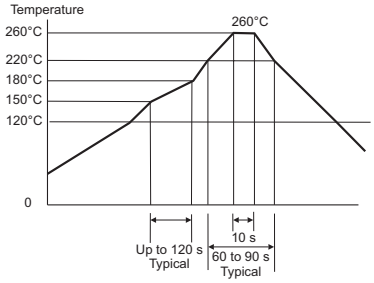
Test Circuit



Output Waveform

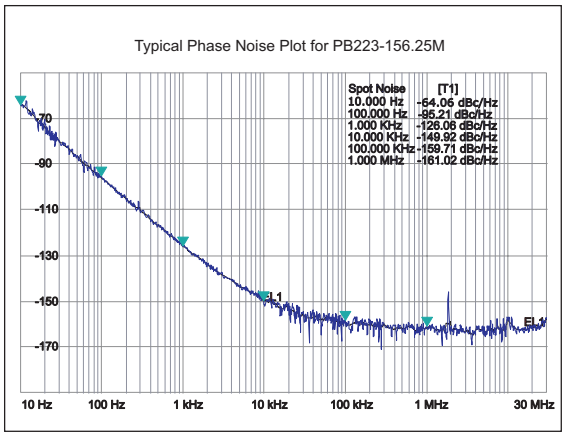


Solder Profile

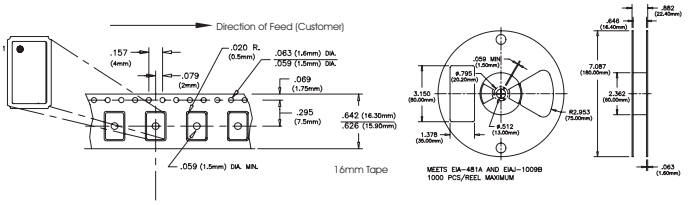


Meets IPC/JEDEC J-STD-020C

Phase Noise Plot



Tape and Reel Dimensions



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