M21528-13

Dual 3G/HD/SD-SDI Multi-rate Video Cable Driver

Rev V5

Applications

- 3G/HD/SD Video Switchers
- 3G/HD/SD Video Routers
- 3G/HD/SD Distribution Amplifiers
- DVB-ASI Equipment
- SMPTE 259C/D, 292M, 424M, DVB ASI 270Mb/s

Features

- Dual channel cable driver
- Two pairs of non-inverting, SMPTE compliant outputs
- Typical output jitter of 12 ps peak–to–peak at 2.97 Gbps
- Exceptional Output Return Loss with no matching network
- Very low power design; 40 mW/channel @1.8V
- Selectable slew rate for SD and 3G/HD operation
- Input equalization for up to 36" of FR4 + 2 connectors
- Integrated, selectable 75Ω or 50Ω output termination
- Integrated 50Ω input termination
- Integrated 2x2 crosspoint switch with broadcast mode
- On-chip regulators for operation from 1.8V to 3.3V DC supply
- Universal DC coupling at the input, from 1.2V to 3.3V
- Cable detect with automatic power down and power up upon cable disconnect and re-connect
- Loss of input signal detection
- Independent channel mute and power down
- Industrial operating temperature range: -40°C to 85°C
- 4 kV HBM and 500V CDM ESD rating
- 4 mm x 4 mm 24 pin QFN package
- Green and RoHS compliant

The M21528 is a very low power, highly integrated, dual cable driver for SMPTE compliant digital video applications. It can drive 2 pairs of 75Ω coaxial cables, or 50Ω equivalent loads, at SDI data rates from 270 Mbps to 2.97 Gbps. The device is capable of outputting SDI signals with typical jitter values of 12 ps peak–to–peak, when operating at 2.97 Gbps.

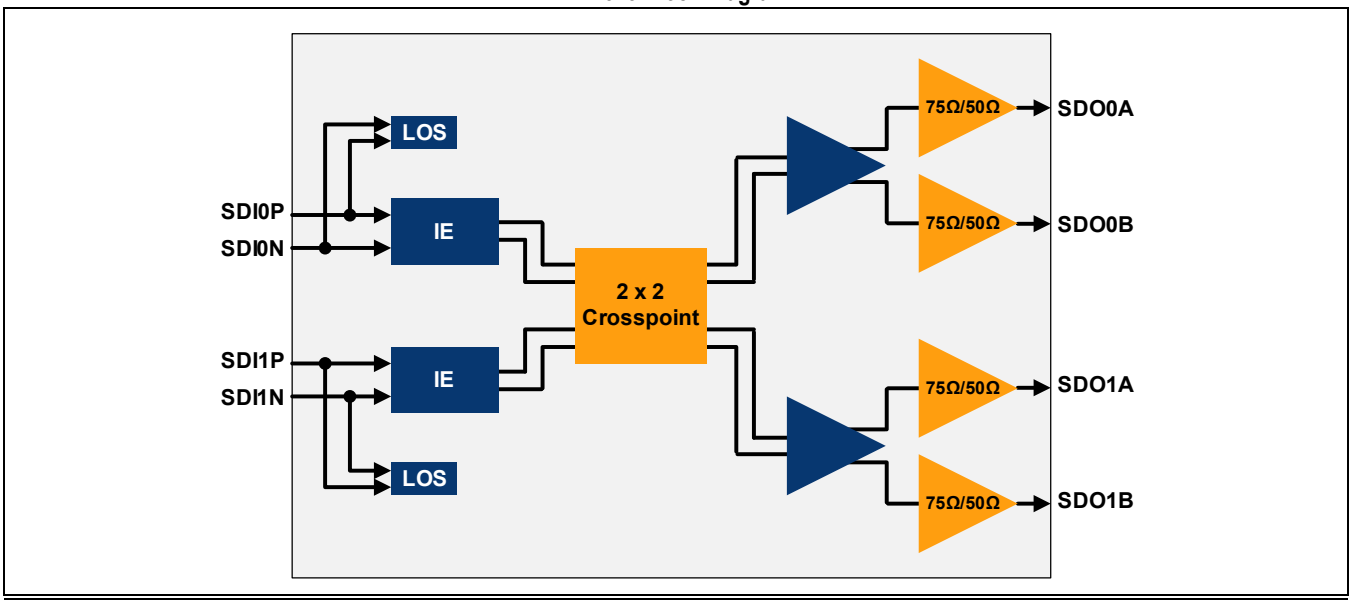
The dual cable driver includes a 2x2 input crosspoint and integrated input and output termination resistors. The M21528, with input equalization for up to 36" of FR4 trace in addition to two connectors and exceptional Output Return Loss (ORL), is ideal for high speed, 3G-SDI, designs.

The device features integrated supply regulators, allowing it to be powered from 1.8V, 2.5V, or 3.3V supply voltages. When operating at 1.8V, it consumes only 40 mW per channel at 2.97 Gbps. Furthermore, the power rails for the input and output circuitry are electrically isolated on-chip and as such may be connected to different voltage rails on the board. This feature enables the M21528 to be DC coupled to any upstream device in the 1.2V to 3.3V range.

The integrated 2x2 crosspoint allows for either input to be routed to either output, eliminating the need for an external multiplexer. Additionally, one input may be routed to both outputs. The cable driver also provides cable detect and Loss of Signal (LOS) functionality. It can be configured to automatically power down at cable disconnect or loss of input signal.

The M21528 is offered in a green and RoHS compliant 24 pin QFN package.

M21528 Block Diagram



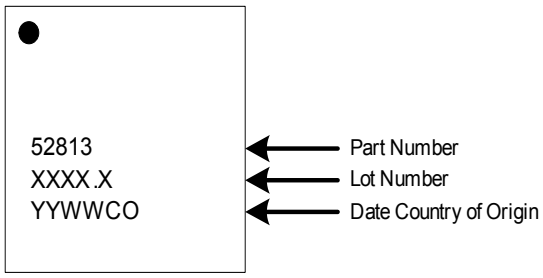
Ordering Information

Part Number	Package	Operating Temperature
M21528G-13	4 mm x 4 mm 24-pin QFN (RoHS compliant)	–40 °C to 85 °C
* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.		

Revision History

Revision	Level	Date	Description
V5	Release	May 2016	Updated Section 4.2 to recommend self-biasing only for DC coupled application.
V4	Release	December 2015	Added footnotes to Figure 3-7.
V3	Release	May 2015	Revised Z_CTRL resistor value for 75Ω output impedance in Table 3-1. Revised Section 4.3. Updated Marking Diagram. Updated Figure 3-7 with new package diagram.
E (V2)	Release	March 2010	Corrected Figure 3-7 center pad dimensions. Revised Table 1-5; DRIN min, JAO 3G, HD max.
D (V1)	Release	December 2009	Added marking diagram. Added Eye Diagams in Section 2.0. Revised typical and Maximum values in Table 1-3. Revised Table 1-4. Revised Figure 3-2 and Figure 3-3.
C (V1P)	Preliminary	May 2009	Added Note 5 to Table 1-5. Removed Note 2 from Table 3-1 (2-state/I-Digital inputs have an internal 100KΩ resistor to $AV_{DD}I$). Revised Figure 4-3, Figure 4-4, Figure 4-5. Added input/output circuits in Section 3.0.
B (V2A)	Advance	February 2009	Major revisions throughout document.
A (V1A)	Advance	June 2008	Initial Release.

M21528 Marking Diagram



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1.0 Electrical Characteristics

Unless noted otherwise, specifications apply for typical recommended operating conditions shown in Table 1-2, with $AV_{DD}O$ = 1.8V, $AV_{DD}I$ = 1.2V, CML inputs at 800 mV differential (RL = 50Ω), PRBS 2^{15} – 1 test pattern at 2.97 Gbps.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
$AV_{DD}I$	Analog supply for input circuitry	1	-0.5	—	3.6	V
$AV_{DD}O0/1$	Analog supply for output circuitry	1	-0.5	—	3.6	V
T_{ST}	Storage Temperature	1	-65	—	150	ºC
ESD	Human Body Model (HBM)	1	-4	—	4	KV
ESD	Charge Device Model (CDM)	1	-500	—	500	V
LU	Latch Up @ 85ºC	1	-200	—	200	mA
HSIC	Maximum High-speed input current	1	-100	—	100	mA
HSOC	Maximum High-speed output short circuit current	1	-100	—	100	mA
V_{INMAX}	Input voltage range	1	-0.5	—	$AV_{DD}I$+0.5	V

NOTES:

1. Exposure to these conditions over extended periods of time may affect device reliability

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
$AV_{DD}I$	Analog supply for input circuitry	—	1.14	1.2, 1.8, 2.5, or 3.3	3.465	V
$AV_{DD}O0/1$	Analog supply for output circuitry	—	1.71	1.8, 2.5, or 3.3	3.465	V
T_{CASE}	Operating temperature	1	-40	25	+85	ºC
ESD	Human Body Model (HBM)	—	-4	—	4	kV

NOTES:

1. Case temperature.

Table 1-3. Power Consumption Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
P_{DISS}	Total power consumption	$AV_{DD}I$ = 1.2V $AV_{DD}O$ = 1.8V Both channels active, 4 outputs on	1	—	78	122	mW
		$AV_{DD}I$ = 1.2V $AV_{DD}O$ = 1.8V Both channels active, one output per channel on	1	—	61	95	mW
		$AV_{DD}I$ = 1.2V $AV_{DD}O$ = 1.8V One channel active, one output on	1	—	49	86	mW
$I\_AV_{DD}I$	Total $AV_{DD}I$ supply current	$AV_{DD}I$ = 1.2V	1	—	1	3.0	mA
$I\_AV_{DD}I$	Total $AV_{DD}I$ supply current	$AV_{DD}I$ = 1.8V	1	—	3	7.0	mA
$I\_AV_{DD}I$	Total $AV_{DD}I$ supply current	$AV_{DD}I$ = 3.3V	1	—	10	17.0	mA
$I\_AV_{DD}O$	Total $AV_{DD}O$ supply current	Both channels active	1,2	—	43	68.0	mA
$I\_AV_{DD}O$	Total $AV_{DD}O$ supply current	Only channel 0 active	1,2	—	43	68.0	mA
$I\_AV_{DD}O0$	Total $AV_{DD}O0$ supply current	Only channel 1 active	1,2	—	27	49.0	mA
θ_{JA}	Junction to ambient Thermal Resistance		3	—	63	—	°C/W

NOTES:

1. Recommended operating condition—see Table 1-2.
2. Current consumption does not change with $AV_{DD}O$ = 1.8V, 2.5V or 3.3V.
3. Airflow = 0 m/s.

Table 1-4. Digital Input Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_{IH}	Input Logic High	—	0.85 x $AV_{DD}I$	—	$AV_{DD}I$ + 0.5	V
V_{IF}	Input Logic Floating State	—	0.25 x $AV_{DD}I$	—	0.75 x $AV_{DD}I$	V
V_{IL}	Input Logic Low	—	0	—	0.15 x $AV_{DD}I$	V
I_{IH}	Input Current—Logic High	—	-100	—	100	µA
I_{IL}	Input Current—Logic Low	—	-100	—	100	µA

Table 1-5. High Speed Input/Output Electrical Specifications

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
V_O	Output Voltage Range	1	730	800	850	mV
t_r/t_f	SD Rise/Fall Time (20–80%)	1,3,4	400	600	800	ps
t_r/t_f	3G/HD Rise/Fall Time (20–80%)	1	—	70	90	ps
t_r-t_f	SD Rise/Fall Time Mismatch	1,3,4	—	—	125	ps
t_r-t_f	3G/HD Rise/Fall Time Mismatch	1,3	—	—	30	ps
DCD	Duty Cycle Distortion, SD	1,4	—	—	100	ps
DCD	Duty Cycle Distortion, 3G, HD	1,3	—	—	30	ps
JAO_{PP}	Additive Output Jitter, SD	1,2,4	—	60	100	ps
JAO_{PP}	Additive Output Jitter, 3G, HD	1,2	—	12	29	ps
S_{22}	Output Return Loss (5 MHz to 1.5 GHz)	6,8	20	—	—	dB
S_{22}	Output Return Loss (5 MHz to 3.0 GHz)	5,8	11	—	—	dB
S_{22}	Output Return Loss (5 MHz to 3.0 GHz)	6,8	14	—	—	dB
DR_{IN}	Input Data rate	—	270	—	2970	Mbps
V_{ID}	Differential Input Voltage (p–p)	7	400	—	1600	mV
V_{IC}	Input Common mode range	—	AV_{DD}I – 0.6	—	AV_{DD}I + 0.1	V
IE	Input Equalizer Gain Off (EN_EQ = 0)	—	—	0	—	dB
	Input Equalizer Gain Med (EN_EQ = F)	—	—	4	—	dB
	Input Equalizer Gain High (EN_EQ = H)	—	—	6	—	dB
R_{INT}	Input Termination to AV_{DD}I	—	40	50	60	Ω

NOTES:

1. Measured AC coupled into 1m coaxial cable, terminated with appropriate 75Ω or 50Ω load.
2. Measured with PRBS 2^{15}-1 test pattern.
3. For data rates above 360 Mb/s, the cable driver must be in HD mode (SD/xHD = 0).
4. SD/xHD = 1, measured at 270 Mb/s.
5. Without external matching network.
6. With external matching network $R_{matching}$=75Ω, $L_{matching}$=1nH, only applicable to 75Ω mode.
7. EQ_EN = L (input equalization off) PD_MODE = F (LOS enabled), point blank.
8. As measured on MACOM EVM at BNC connector with output impedance set to 75Ω.

2.0 Typical Performance Characteristics

Figure 2-1. Eye Diagram at 270 Mbps

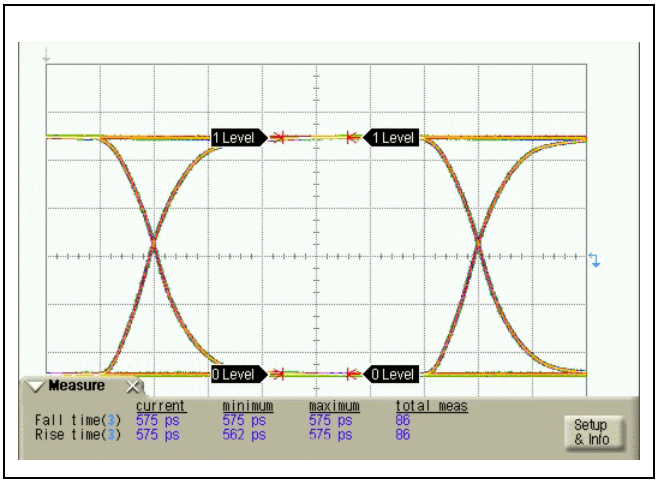


Figure 2-2. Eye Diagram at 1485 Mbps

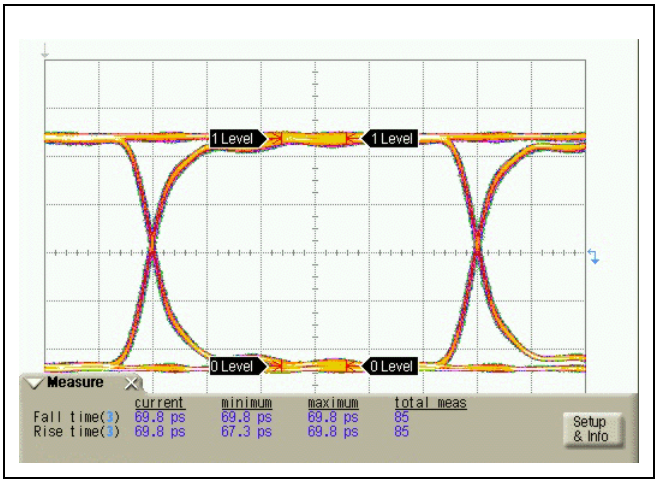
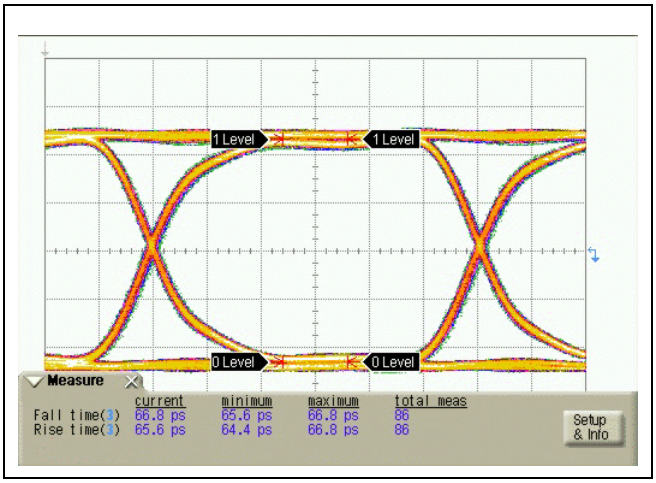


Figure 2-3. Eye Diagram at 2970 Mbps



3.0 Pinout Diagram, Pin Description, and Package Drawing

Figure 3-1. Pinout Diagram (Top View)

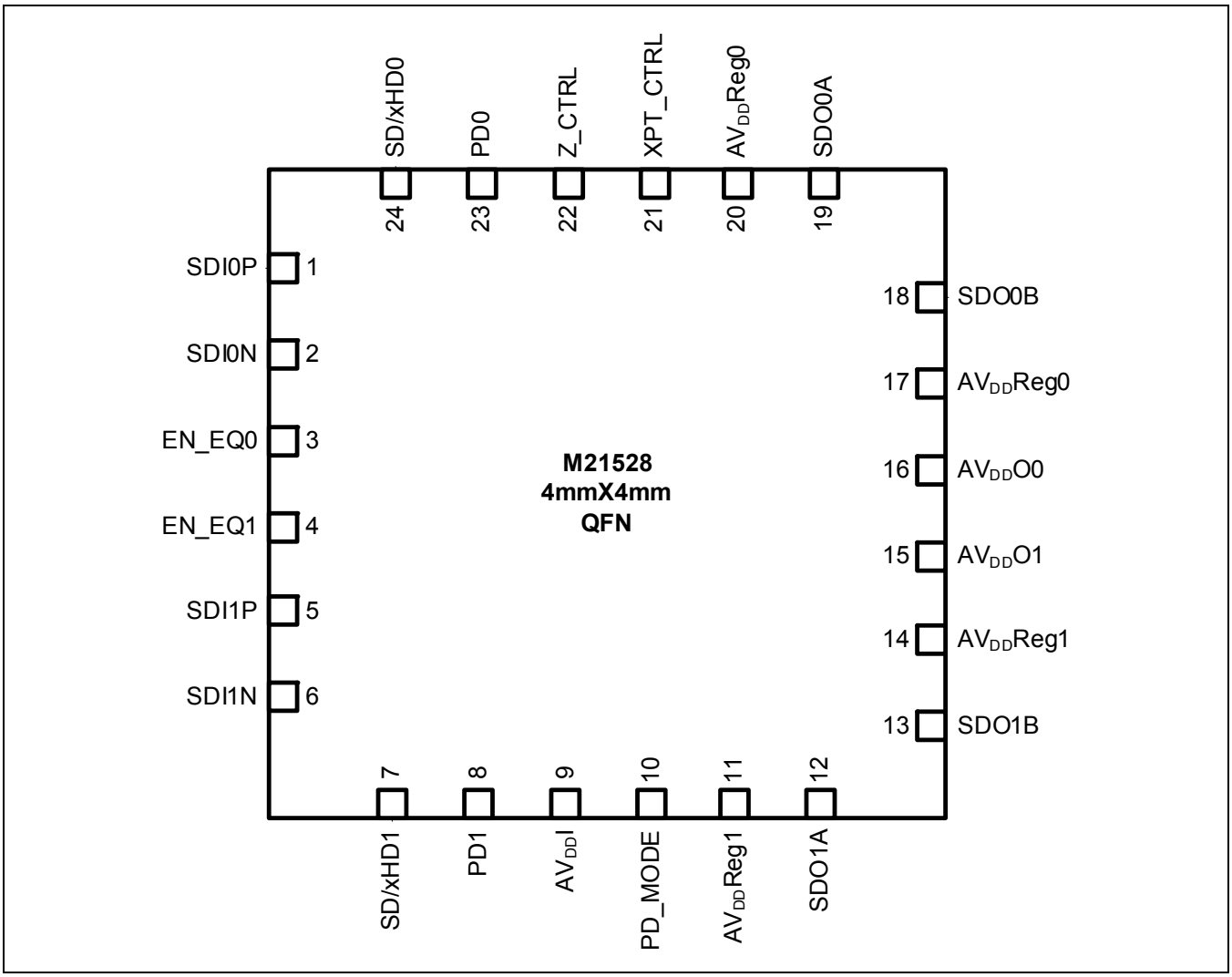


Table 3-1. Pin Description (1 of 2)

Pin Name	Pin Number	Type	Description
AV_{SS}	Center Ground Paddle	Power	Chip Ground
AV_{DD}I	9	Power	Positive supply for inputs circuitry
AV_{DD}Reg0	17,20	Power	Regulator0 bypass capacitor connection, positive supply for output0
AV_{DD}Reg1	11,14	Power	Regulator1 bypass capacitor connection, positive supply for output1
AV_{DD}O0	16	Power	Positive supply for reglator0
AV_{DD}O1	15	Power	Positive supply for reglator1
SDO0A	19	O-Analog	High speed serial output, channel0, output A
SDO0B	18	O-Analog	High speed serial output, channel0, output B
SDO1A	12	O-Analog	High speed serial output, channel1, output A
SDO1B	13	O-Analog	High speed serial output, channel1 output B
SDI0P/N	1,2	I-Analog	High speed serial video data input, channel0
SDI1P/N	5,6	I-Analog	High speed serial video data input, channel1
Z_CTRL	22	I-Analog	Sets output impedance through an external Z_CTRL resistor connected to AV_{SS} Z_CTRL=665Ω to set 75Ω output impedance Z_CTRL=250Ω to set 50Ω output impedance
SD/xHD0	24	I-DIGITAL	Output slew rate control for channel 0 L = SDO0 has 3G/HD slew rate H = SDO0 has SD slew rate
SD/xHD1	7	I-DIGITAL	Output slew rate control for channel 1 L = SDO1 has 3G/HD slew rate H = SDO1 has SD slew rate
PD0	23	3-state/I-DIGITAL	Power down control for channel 0 L = SDO0A on, SDO0B power down F = Both outputs on H = Power down both outputs
PD1	8	3-state/I-DIGITAL	Power down control for channel 1 L = SDO1A on, SDO1B power down F = Both outputs on H = Power down both outputs
XPT_CTRL	21	3-state/I-DIGITAL	Crosspoint control L = SDI0 to SDO1, SDI1 to SDO0 F = SDI0 to SDO0, SDI1 to SDO1 H = SDI0 to SDO0 and SDO1

Table 3-1. Pin Description (2 of 2)

Pin Name	Pin Number	Type	Description
PD_MODE	10	3-state/I-DIGITAL	Power down and cable detect control L = Cable detect disabled, PD upon LOS disabled F = Cable detect enabled, PD upon LOS enabled H = Cable detect enabled, PD upon LOS disabled
EN_EQ0	3	3-state/I-DIGITAL	Input equalization control for channel 0 L = No Input Equalization on SDI0P/N F = Medium Input Equalization on SDI0P/N H = High Input Equalization on SDI0P/N
EN_EQ1	4	3-state/I-DIGITAL	Input equalization control for channel 1 L = No Input Equalization on SDI1P/N F = Medium Input Equalization on SDI1P/N H = High Input Equalization on SDI1P/N

NOTES:

1. 3-state inputs have a default of F (floating).
2. A Z_CTRL resistance of 665Ω will also provide 800mVpp output swing.

Figure 3-2. Differential Input (SDIP, SDIN)

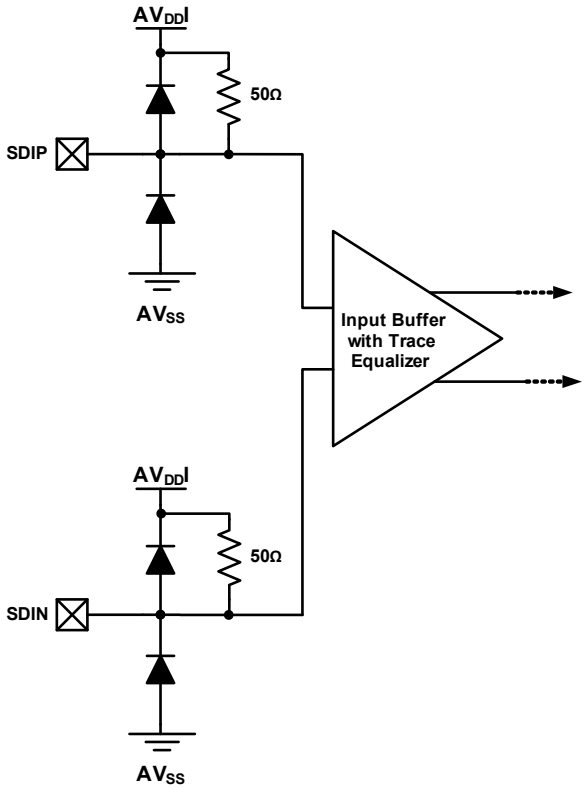


Figure 3-3. Single-Ended Output (SDO0A, SDO0B, SDO1A, SDO1B)

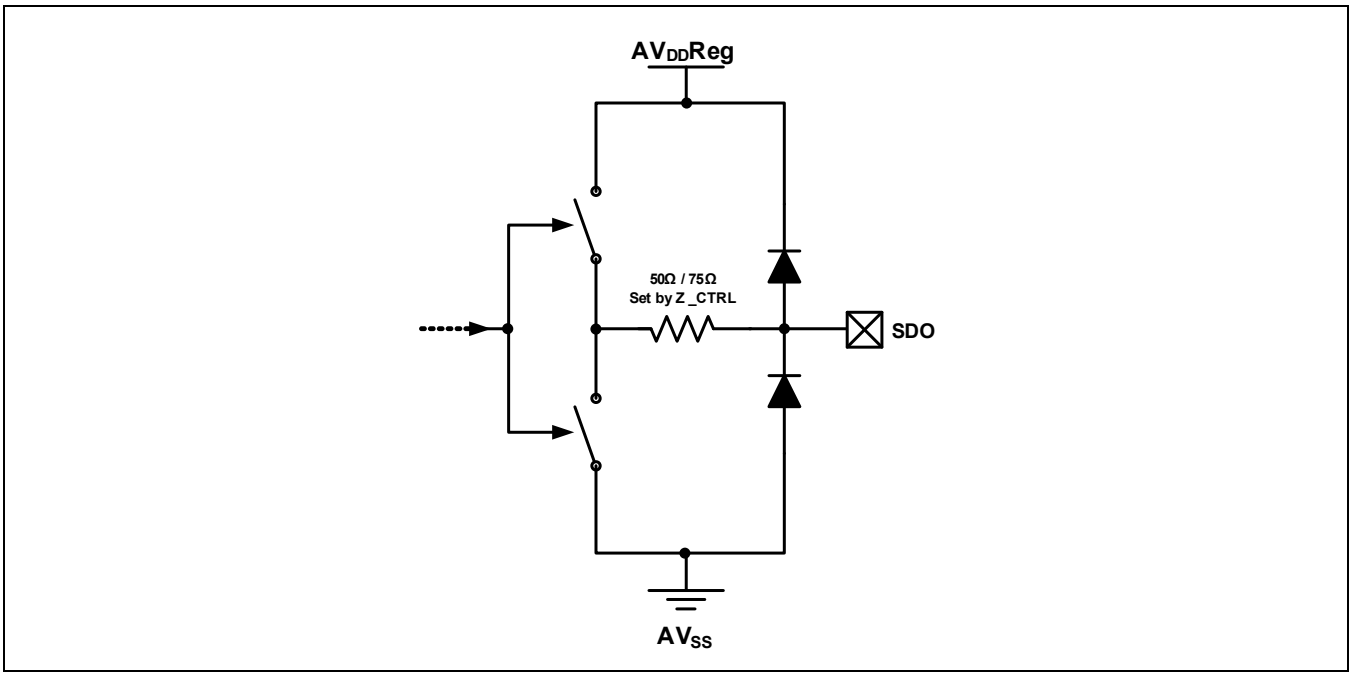


Figure 3-4. Digital Input Pin (SD/xHD0, SD/xHD1)

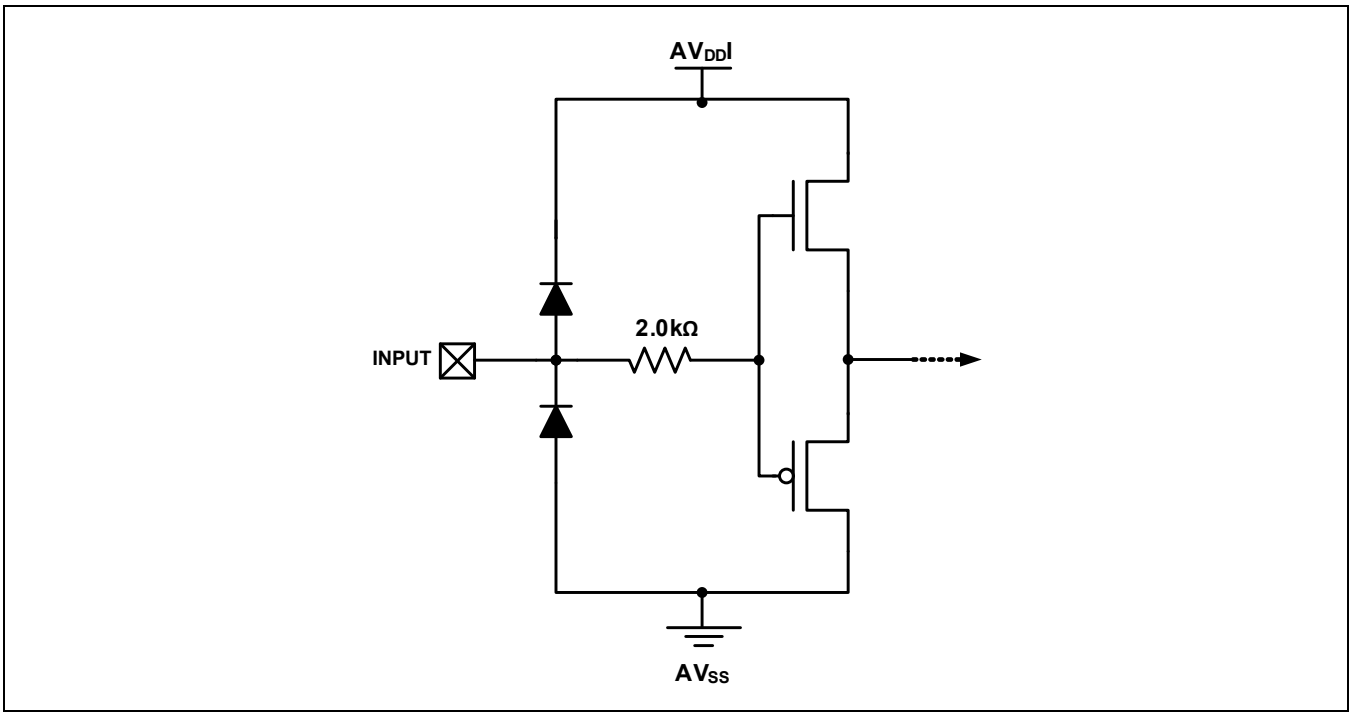
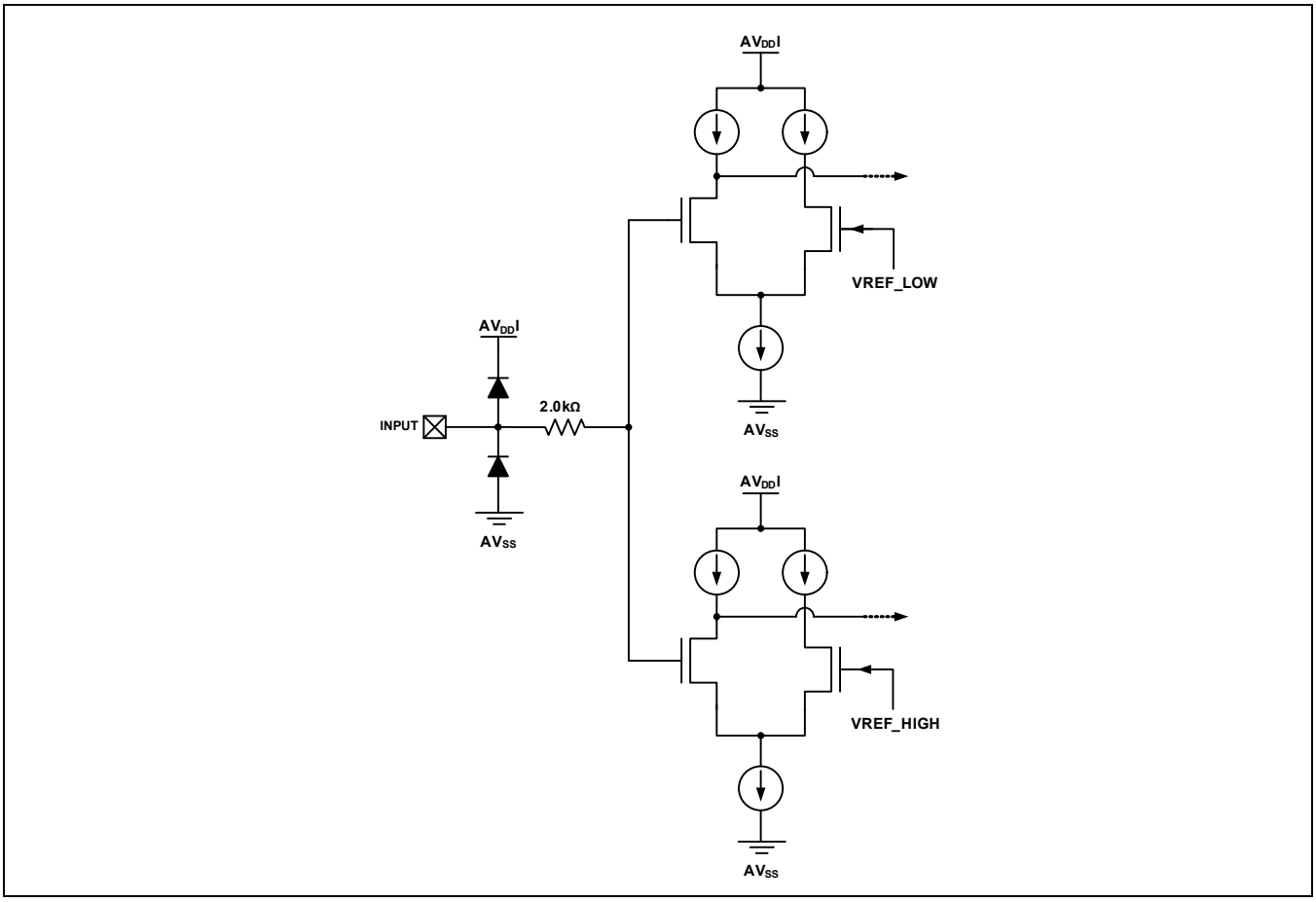


Figure 3-5. State Logic Input (PD0, PD1, XPT_CTRL, PD_MODE, EN_EQ0, EN_EQ1)



The M21528 is assembled in 24 pin 4 mm x 4 mm Quad Flat No-Lead (QFN) package. The exposed die paddle serves as the IC ground (AV_{SS}), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB ground. A cross-section of the QFN package can be found in Figure 3-6.

Figure 3-6. QFN Package Cross Section

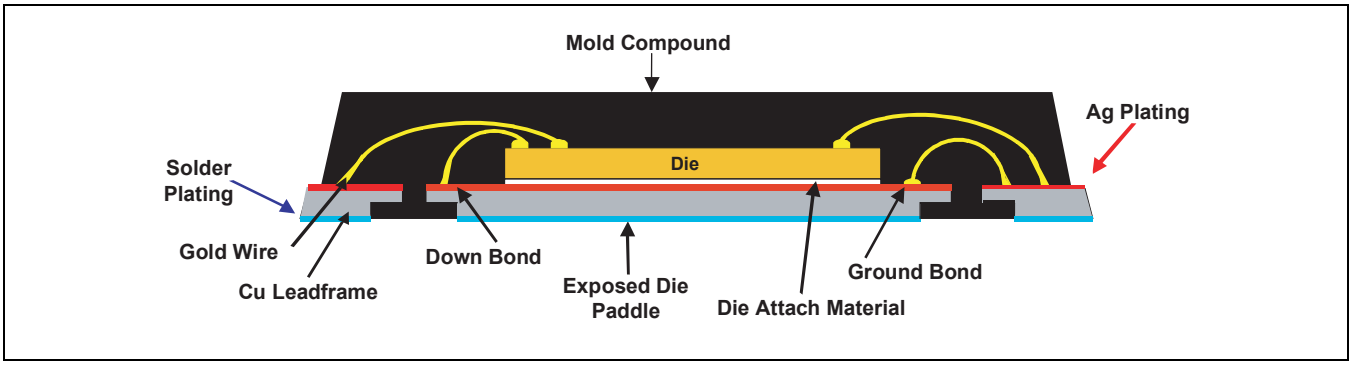
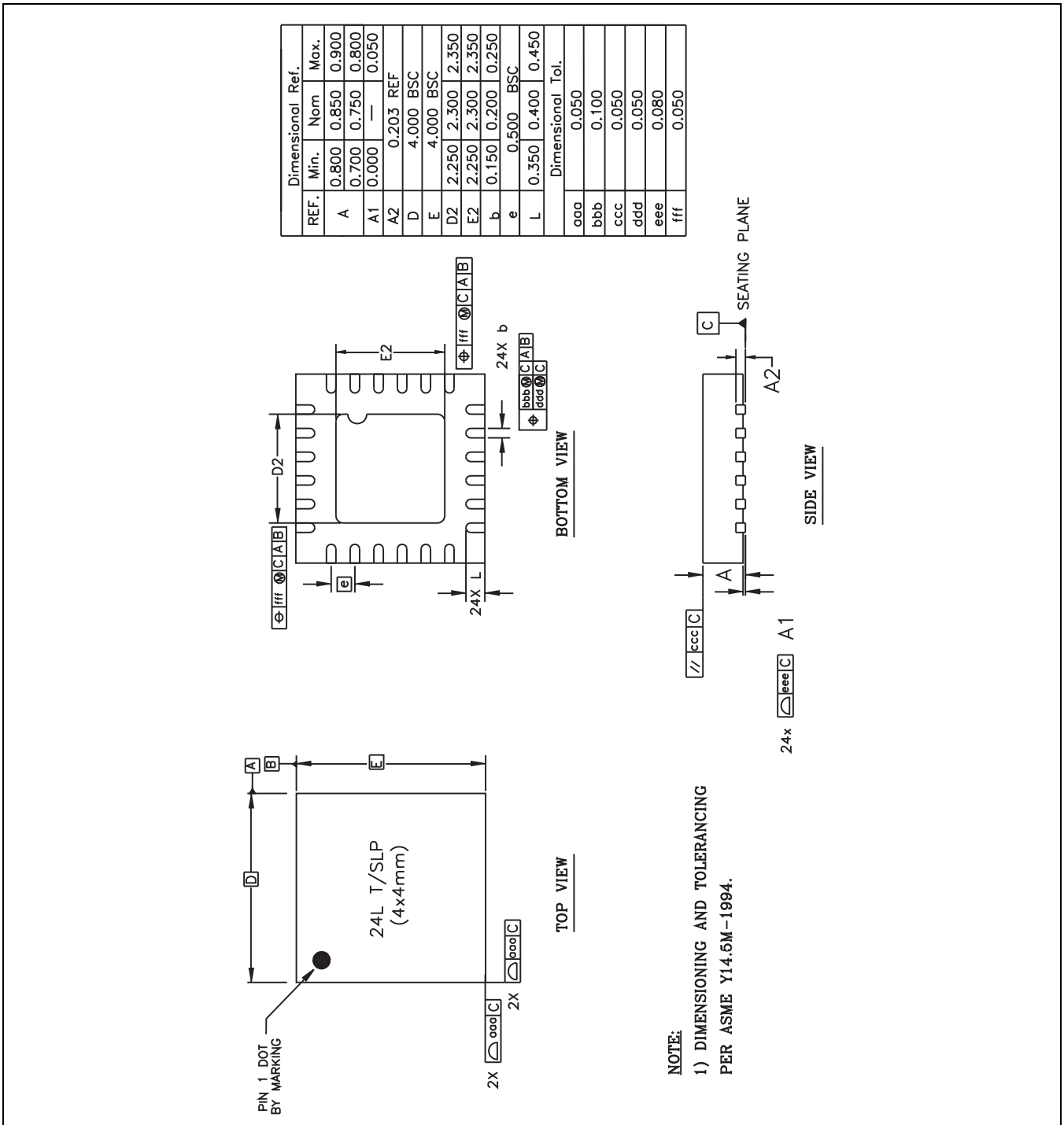


Figure 3-7. Package Drawing



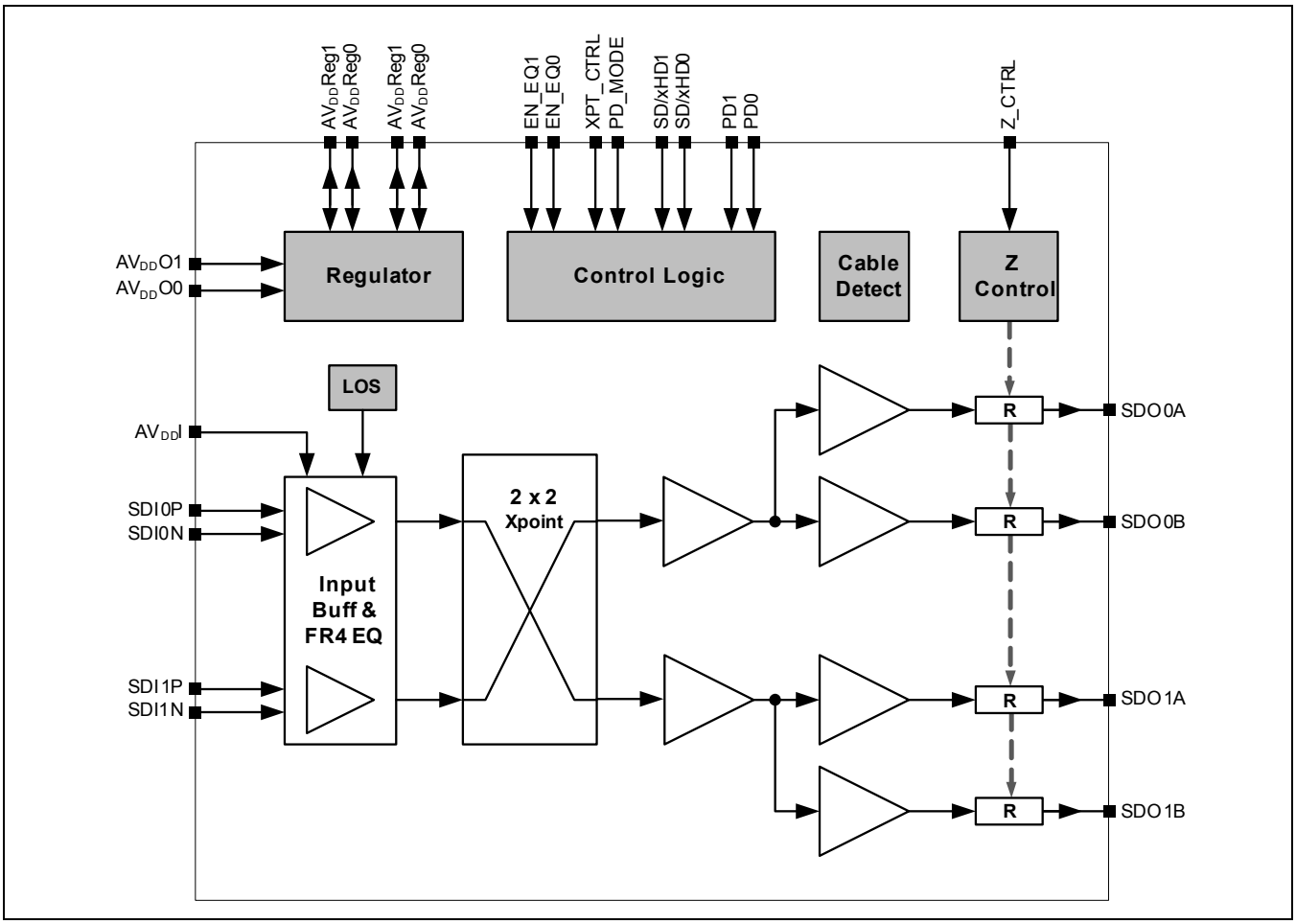
1. For dimension reference A, Min. is 0.800, Nom. is 0.850 and Max. is 0.900.
2. New Unisem package and old Amkor package have the same footprint dimensions.

4.0 Functional Description

4.1 Block Diagram

Figure 4-1 is the functional block diagram of the M21528. The subsequent sections provide additional detail on the operation of the device.

Figure 4-1. M21528 Functional Block Diagram



4.2 Input Description

The M21528 has differential inputs, with integrated 50Ω pull ups to $AV_{DD}I$. $AV_{DD}I$ may be supplied from a 1.2V, 1.8V, 2.5V, or 3.3V supply. The input buffers are compatible with PCML, LVDS or LVPECL signal levels.

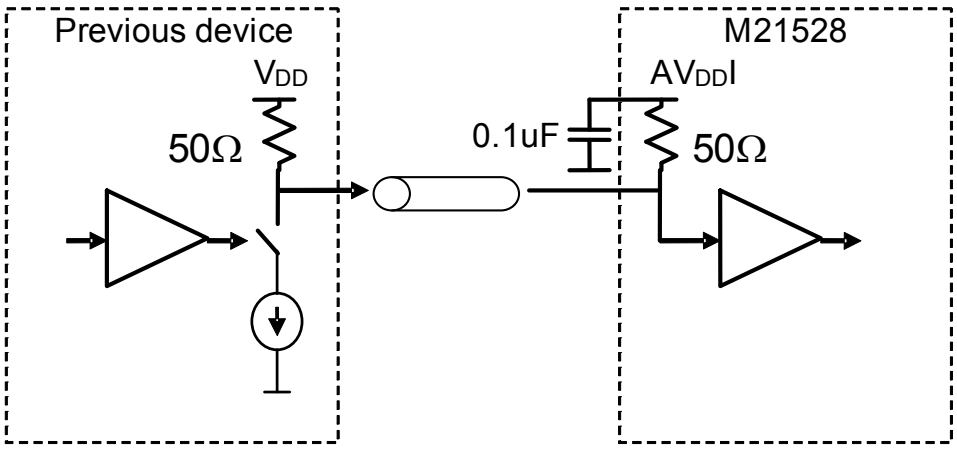
To improve signal integrity in large systems, all inputs have programmable input equalization (IE) with three gain levels: 0 dB, 4 dB, 6 dB.

Setting the gain to 0dB effectively disables the IE feature. The pins EN_EQ0 and EN_EQ1 allow for the selecting the proper level of input equalization based on the board characteristics for each input. The maximum level of equalization compensates for up to 36” of FR4 trace. The operation of the EN_EQ0/1 pin is summarized in Table 4-1 below.

Table 4-1. Operation of EQ_EN0 and EQ_EN1 Pins

Pin	Level	Function
EN_EQ0	L	SDI0P/N IE EQ gain = 0 dB
	F	SDI0P/N IE EQ gain = 4 dB
	H	SDI0P/N IE EQ gain = 6 dB
EN_EQ1	L	SDI1P/N IE EQ gain = 0 dB
	F	SDI1P/N IE EQ gain = 4 dB
	H	SDI1P/N IE EQ gain = 6 dB

In 3G/HD/SD SDI applications, it is best to avoid AC coupling data interfaces between devices, if possible. DC coupling will result in increased system jitter margin. Also, DC coupling eliminates the requirement for additional components on the board. In order to accommodate DC coupling to the upstream device, a “self-biasing” scheme can be used at the input. This offers the benefit of having the V_{DD} of the previous device and the power domain(s) of the M21528 completely separated, while allowing DC coupling:



In this configuration, the minimum input common mode that can be tolerated, is 1.2V.

If, for any reason, AC coupling is necessary, then a capacitor of 4.7 µF or greater must be used.

A Loss of Signal (LOS) detector circuit monitors each input and issues an internal alarm when the input signal goes below the detection threshold. The detection threshold is 90 mVpp with +90 mV hysteresis. This means that if the input signal level drops below 90 mVpp, then the internal LOS alarm is asserted. For the alarm to be de-asserted, the input signal must increase to greater than 180 mVpp; the hysteresis prevents the internal LOS alarm from chattering.

Depending on the state of the PD_MODE pin, the LOS alarm at a particular input can power down the associated signal path and forces the corresponding output to low level.

4.3 Output Description

The M21528 contains two independent signal channels, each with two positive polarity cable driver outputs. Unlike conventional SMPTE compliant cable drivers, the M21528 uses a voltage mode implementation as opposed to current mode. This allows for significant power savings when compared to previous generation cable drivers with the added benefit of two positive polarity outputs per channel.

Internally an output buffer drives a 1.6V amplitude signal through an integrated impedance load. The impedance of the load is set by the external Z_CTRL resistor to AV_{SS}. For most applications Z_CTRL should be 665Ω, which sets the output load to 75Ω and provides 800mVpp output swing. If the application requires a 50Ω output impedance, Z_CTRL may be 250Ω. In both cases Z_CTRL must have 1% tolerance.

The M21528 can meet SMPTE ORL specifications without the need for an external matching network. However, for additional margin a matching network consisting of a 75Ω resistor and a 1 nH inductor may be used.

Each channel has a dedicated power down pin, PD0 and PD1. The operation of the PD pin is summarized in Table 4-2 below. When powered down, the signal at the output is set to low.

Table 4-2. Operation of PD0 and PD1 Pins

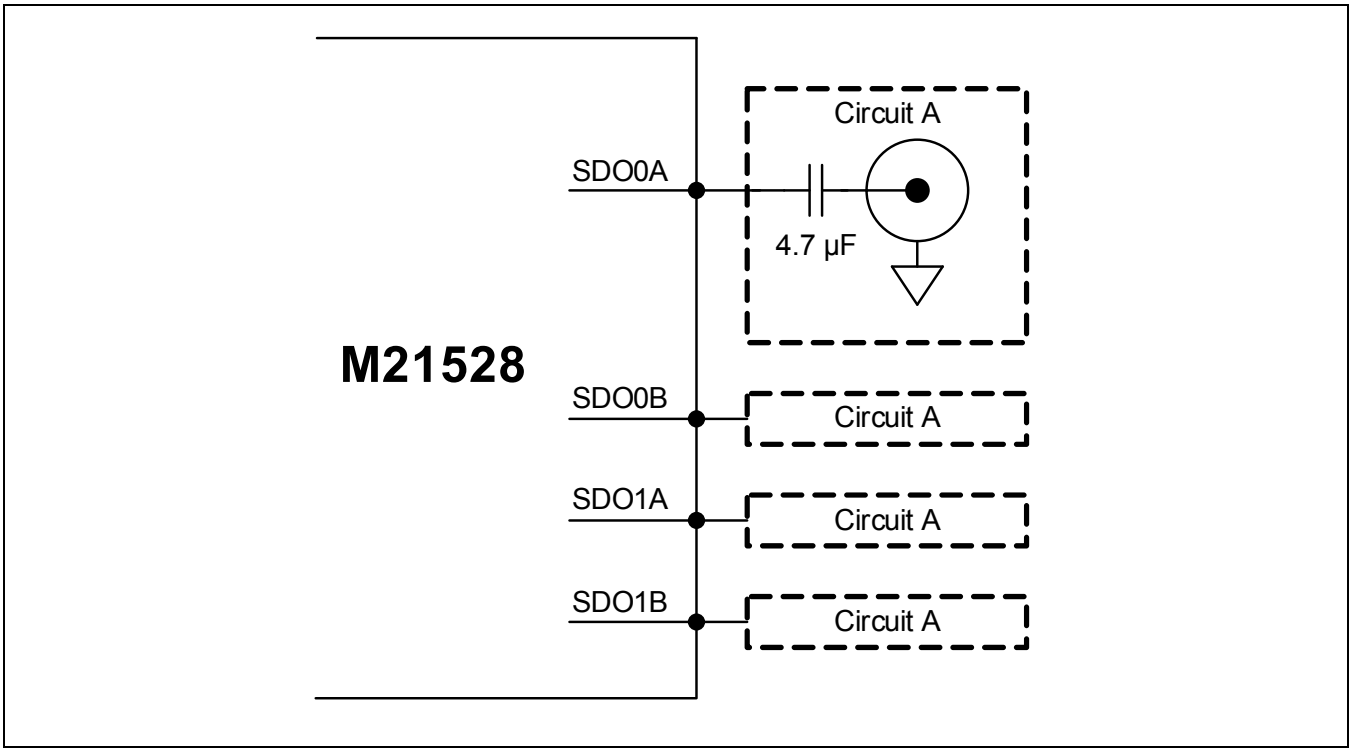
Pin	Level	Function
PD0	L	SDO0A on, SDO0B powered down
	F	Both SDO0A and SDO0B on
	H	Both SDO0A and SDO0B powered down
PD1	L	SDO1A on, SDO1B powered down
	F	Both SDO1A and SDO1B on
	H	Both SDO1A and SDO1B powered down

Figure 4-2 shows a typical output circuit.

When the cable detect function is enabled, only the outputs used need to be connected, unused outputs may be left floating.

However, if the cable detection function is disabled, unused outputs must be powered down or properly terminated.

Figure 4-2. Typical Output Circuit (all outputs connected)



4.4 Power Supply Description

The device features two internal regulators to supply the power for the output drivers for each channel. $AV_{DD}O0$ and $AV_{DD}O1$ supply the voltage to each channel's respective regulator. These pins may be connected to DC voltages ranging from 1.8V to 3.3V. Each regulator requires an external 1µF bypass capacitor to ground, which must be connected to $AV_{DD}Reg0$ and $AV_{DD}Reg1$. It is recommended to add a secondary 10 nF bypass capacitor on each regulator output as close to the pin as possible.

In addition to supplying the output stage for channel1, $AV_{DD}O1$ is also used to power the core circuitry for both channels.

A completely separate supply domain, $AV_{DD}I$, provides the supply for the high-speed serial input pins. The input termination and ESD protection for the SDI pins and the digital control input pins are referenced to this supply. The isolated domain allows DC coupling to an upstream device that is running from a different supply voltage. For example, if, in order to save power, $AV_{DD}O0/1$ are connected to 1.8V, but the cable driver must interface to a reclocker that uses a 3.3V supply, then DC coupling can be achieved by simply connecting $AV_{DD}I$ to the 3.3V rail.

Figure 4-3 to 4-5 show three examples of how the cable driver can be configured. Note that even when only one channel is enabled, both output regulators must be supplied with the correct voltage.

Figure 4-3. Supply configuration, both channels and both A and B outputs used

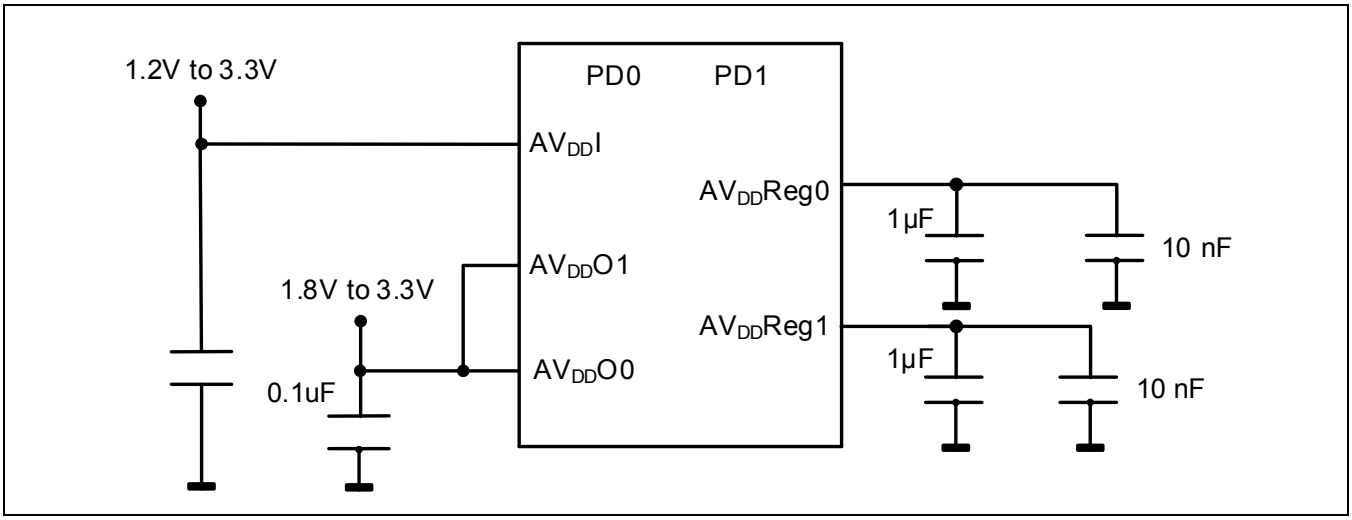


Figure 4-4. Supply configuration, channel0, outputs A and B used, channel 1 powered down

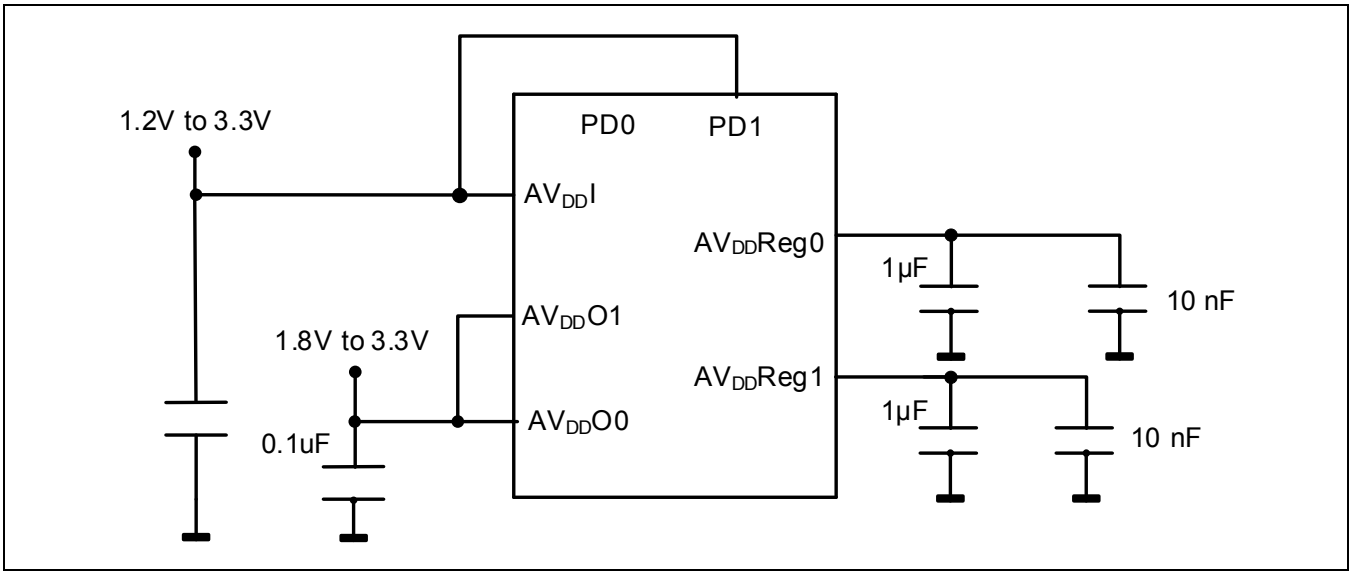
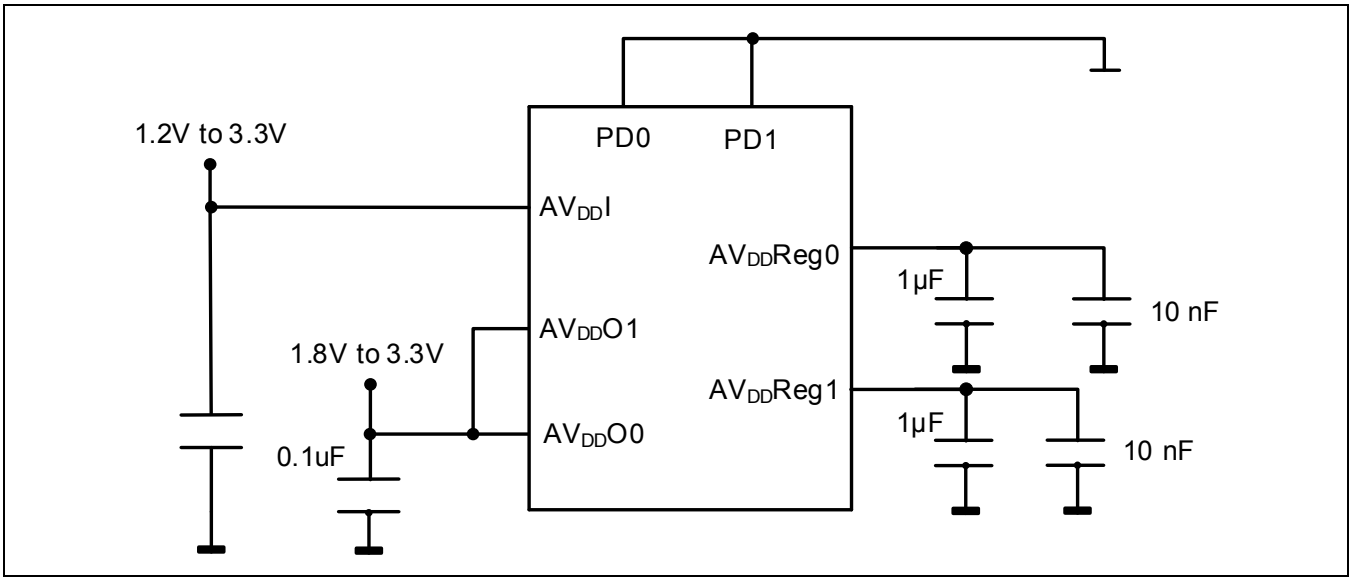


Figure 4-5. Supply configuration, both channels used, but only A outputs used



4.5 Logic Control Signals

The digital logic control signals are ESD protected and referenced to the $AV_{DD}I$. This allows the device to interface to many different logic levels from different supply domains.

Some pins have a state called “F”; this stands for “floating”. To assert this state leave the pin unconnected.

4.5.1 Slew Rate Control

Pins SD/xHD0 and SD/xHD1 control the slew rate of the associated channel outputs. To comply with the SMPTE SD specification the slew rate is slowed down to approximately 600 ps when in SD mode. Note that there is no pull-up on the SD/xHD pins, so it should not be left floating.

Table 4-3. Operation of SD/xHD0 and SD/xHD1 Pins

Pin	Level	Function
SD/xHD0	L	Set SDO0A/B Slew rate to 3G/HD Levels
	H	Set SDO0A/B Slew rate to SD Levels
SD/xHD1	L	Set SDO1A/B Slew rate to 3G/HD Levels
	H	Set SDO1A/B Slew rate to SD Levels

4.5.2 Crosspoint Control

The XPT_CTRL pin controls the 2 x 2 crosspoint at the input. It can be used to redirect the input signal to the other output or from channel 0 to make broadcast mode, so the input on channel 0 appears on both channel 0 and 1 outputs. This last mode is useful in distribution amplifiers where one input can drive fours positive outputs.

The crossover feature can be used in routers to select a second input bank. The functionality of the XPT_CTRL pin is summarized in the table below.

Table 4-4. Operation of XPT_CTRL Pin

Pin	Level	Function
XPT_CTRL	L	Crossover mode: SDI0 routed to SDO1 SDI1 routed to SDO0
	F	Default mode: SDI0 routed to SDO0 SDI1 routed to SDO1
	H	Broadcast mode: SDI0 routed to SDO0 and SDO1

4.5.3 Powerdown Mode Control

The M21528 has integrated output cable detection and input LOS detection circuitry. Depending on the setting of the PD_MODE pin, the device can automatically power down each channel when output cables are disconnected or there is no signal present at the input.

The functionality of the PD_MODE pin is summarized in the table below.

Table 4-5. Operation of PD_MODE

Pin	Level	Function
PD_MODE	L	Cable detection disabled Power down on LOS disabled
	F	Cable detection enabled Power down on LOS enabled
	H	Cable detection enabled Power down on LOS disabled

4.6 Cable Detection

The M21528 features an integrated near-end cable detector. This circuit can detect whether a cable has been disconnected from an output and whether or not it is reconnected without requiring any additional external components.

Utilizing the cable detection feature has several system level advantages such as:

- Reduced power consumption when no cable is connected to both outputs of a single channel
- Reduced EMI
- Eliminate the requirement for external termination

Depending on the state of the PD_MODE pin, when both output A and B of either channel are disconnected, the device can automatically power down the channel resulting in a 75% power reduction for that channel. Furthermore, if output B is manually powered down (PD = L), then disconnecting output A will result in completely powering down the channel (both outputs).

Due to the detection mechanism, the signal at each output within a channel will experience a phase step of approximately 15 ps when the other output's state is changed: powered down, powered up, disconnected, or re-connected.

If one output is disconnected but the other remains connected, and both outputs are toggling, the signal at the connected output may experience up to 10% overshoot for a period of approximately 500 ns. The overshoot is caused by the reflections coupled from the unconnected output to the connected one. 500 ns is the duration required by the circuit to detect the disconnection. If cable detection is disabled and the output is not properly terminated, the overshoot will persist. Therefore, it is strongly recommended to enable cable detection, or terminate both outputs properly; when both outputs of one channel are turned on.

The cable detection function may be disabled by setting PD_MODE=L.