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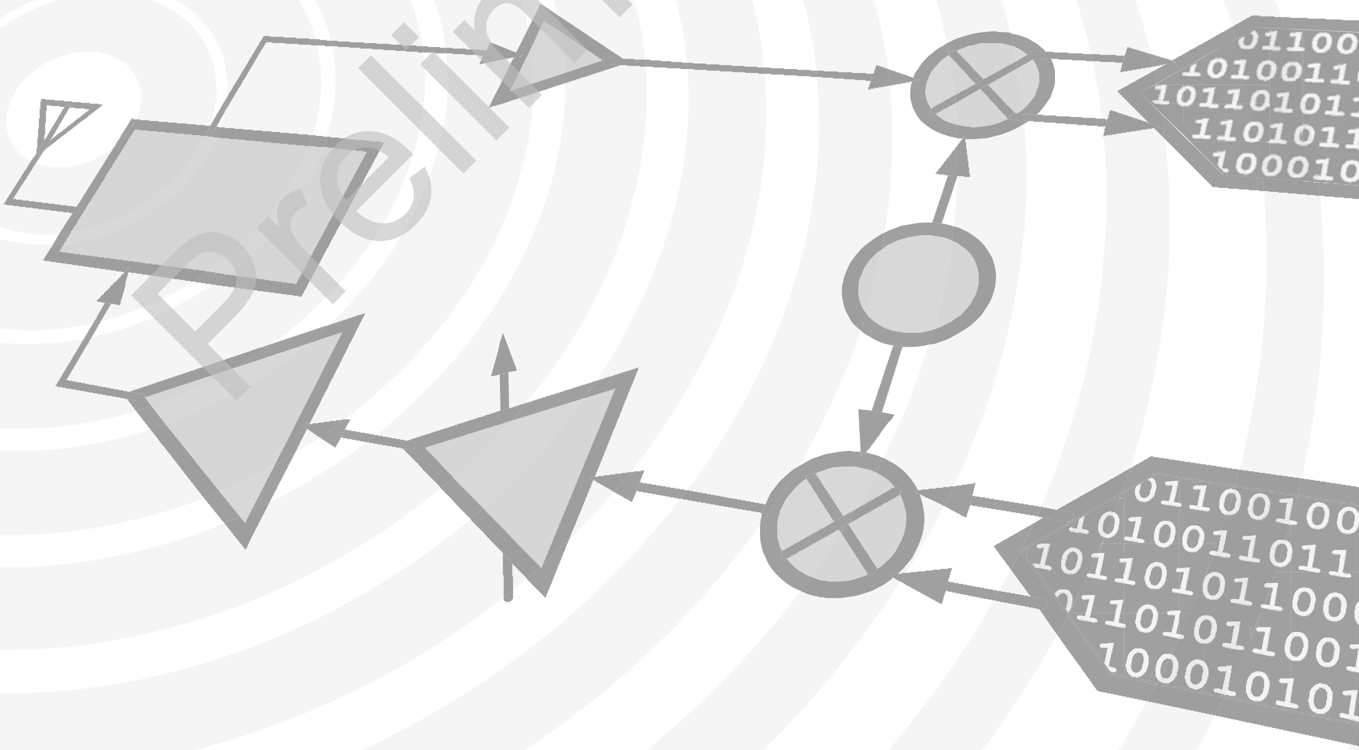

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ANALOG DEVICES

HMC5805ALS6

v00.1115

GaAs pHEMT MMIC
0.25 WATT POWER AMPLIFIER, DC - 40 GHz

Typical Applications

The HMC5805ALS6 is ideal for:

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Features

High P1dB Output Power: 22 dBm

High Psat Output Power: 24 dBm

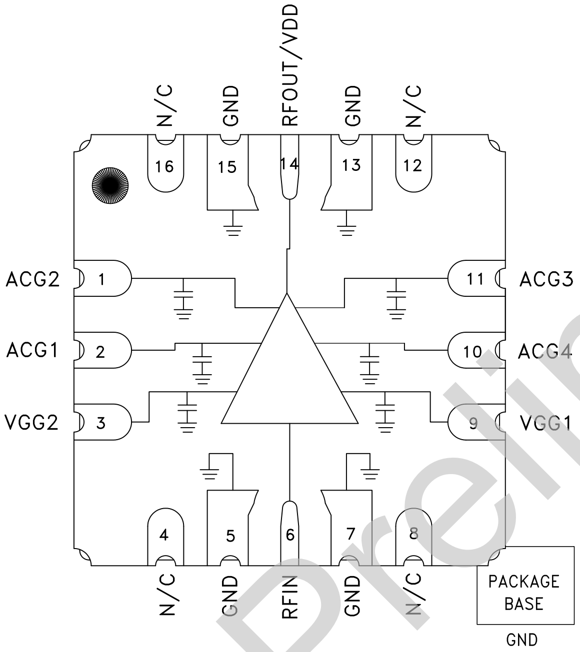
High Gain: 13.5 dB

High Output IP3: 33 dBm

Supply Voltage: +10 V @ 175 mA

16 Lead Ceramic 6x6 mm SMT Package: 36 mm^2

Functional Diagram



General Description

The HMC5805ALS6 is a GaAs pHEMT MMIC distributed power amplifier which operates between DC and 40 GHz. The amplifier provides 13 dB of gain, 33 dBm output IP3 and +22 dBm of output power at 1 dB gain compression while requiring 175 mA from a +10 V supply. The HMC5805ALS6 exhibits a slightly positive gain slope from 8 to 32 GHz, making it ideal for EW, ECM, radar and test equipment applications. The HMC5805ALS6 amplifier I/Os are internally matched to 50 Ohms and the 6x6 mm SMT package is well suited for automated assembly techniques.

Electrical Specifications, T_A = +25° C, Vdd = +10 V, Vgg2 = +3.5 V, Idd = 175 mA*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		DC - 12			12 - 35			35 - 40		GHz
Gain	11	13		11.5	13.5		7	10		dB
Gain Flatness		±0.35			±0.5			±1.0		dB
Gain Variation Over Temperature		0.02			0.03			0.05		dB/ °C
Input Return Loss		18			15			12		dB
Output Return Loss		24			13			11		dB
Output Power for 1 dB Compression (P1dB)	20	22		19	21		16	19		dBm
Saturated Output Power (Psat)		24			23.5			21		dBm
Output Third Order Intercept (IP3)		33			31			27		dBm
Noise Figure		4.5			4			7		dB
Supply Current (Idd) (Vdd= 10V, Vgg1= -0.8V Typ.)		175			175			175		mA

** Adjust Vgg1 between -2 to 0 V to achieve Idd = 175 mA typical.*

GaAs pHEMT MMIC
0.25 WATT POWER AMPLIFIER, DC - 40 GHz

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	12V
Gate Bias Voltage (Vgg1)	-3 to 0 Vdc
Gate Bias Voltage (Vgg2)	For Vdd = 12V, Vgg2 = 5.5V Idd >145mA For Vdd between 8.5V to 11V, Vgg2 = (Vdd - 6.5V) up to 4.5V For Vdd < 8.5V, Vgg2 must remain > 2V
RF Input Power (RFIN)	17 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 69 mW/°C above 85 °C)	2.1 W
Thermal Resistance (channel to ground paddle)	31.1 °C/W
Output Power into VSWR >7:1	24 dBm
Storage Temperature	-65 to 150 °C
Operating Temperature	-40 to 85 °C
ESD Sensitivity (HBM)	Class 0 Passed 150V

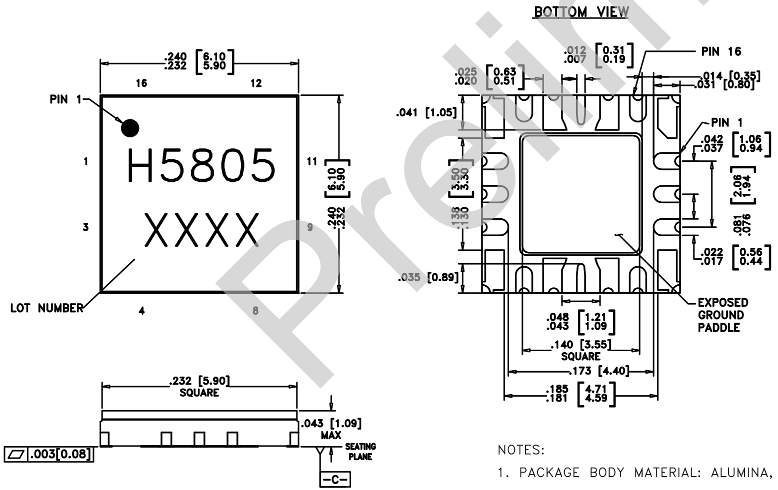
Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+9	175
+10	175
+11	175

Note: Amplifier will operate over full voltage ranges shown above. Vgg adjusted to achieve Idd = 175 mA.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA, WHITE.
2. LEAD AND GROUND PADDLE PLATING: GOLD OVER NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. CHARACTERS TO BE WHITE INK MARKED WITH .018"MIN to .030"MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
6. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.