PRELIMINARY DATA SHEET

SKY13492: 0.4 to 3.8 GHz SP16T MIPI® Antenna Switch Module

Applications

- 2G/3G/4G multimode cellular handsets (LTE, UMTS, CDMA2000, EDGE, GSM, TDD-LTE, TD-SCDMA)
- Embedded data cards

Features

- Dedicated Band 7 TRX ports: 0.85 dB insertion loss @ 2.7 GHz
- High isolation and linearity
- Broadband frequency range: 0.4 to 3.8 GHz
- Fourteen linear TRX ports: B13 2fo <–81 dBm
- Integrated low and high band GSM harmonic filters
- External MIPI select pin to enable multiple trigger controls
- Small MCM (24-pin, 2.5 x 3.3 x 0.8 mm) package (MSL3, 260 °C per JEDEC J–STD–020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

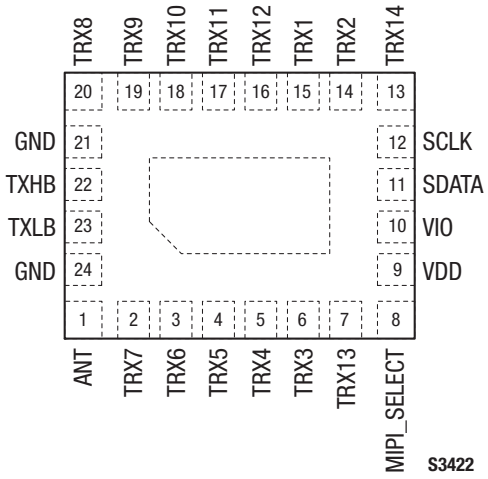


Figure 2. SKY13492 Pinout – 24-Pin MCM (Top View)

Description

The SKY13492 is a Single-Pole, Sixteen-Throw (SP16T) antenna switch with an integrated Mobile Industry Processor Interface (MIPI®) controller. Using an advanced switching technology, the SKY13492 maintains low insertion and high isolation, which makes it an ideal choice for UMTS, CDMA2000, EDGE, GSM, and LTE applications.

The design features two dedicated GSM transmit ports and three dedicated ultra low-loss TRX ports. The switch also has an excellent triple beat ratio and 2nd/3rd Order Intermodulation Distortion (IMD2/IMD3) performance.

Switching is controlled by the MIPI decoder. There is an external MIPI select pin that enables how the switch responds to power mode triggers. When this pin is grounded, the switch responds to any of the power mode triggers. When this pin is left open, the switch responds to individual power mode triggers. No external DC blocking capacitors are required on the RF paths as long as no DC voltage is applied.

The SKY13492 is manufactured in a compact, 2.5 x 3.3 x 0.8 mm, 22-pin surface mount Multi-Chip Module (MCM) package.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

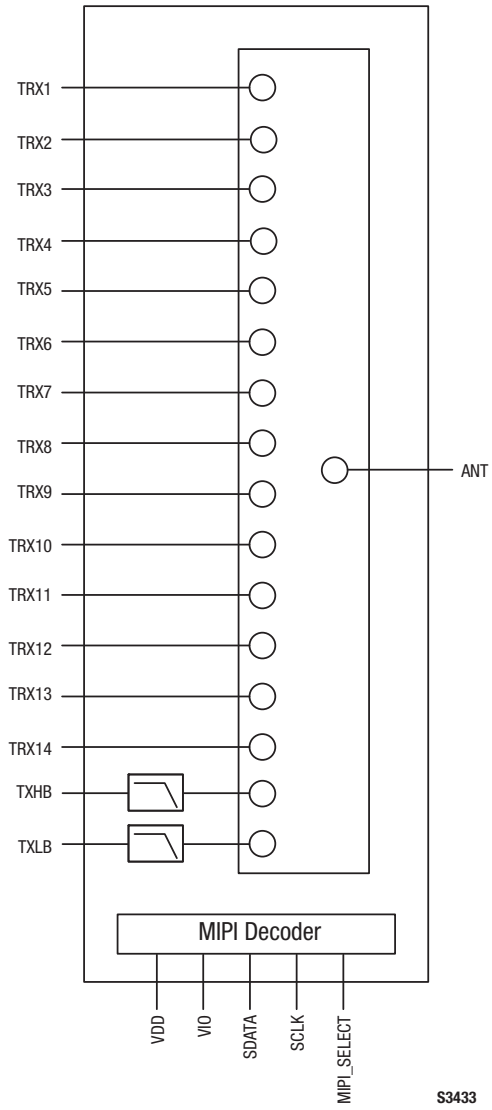


Figure 1. SKY13492 Block Diagram

Table 1. SKY13492 Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	ANT	Antenna port	13	TRX14	3G WCDMA transmit/receive port 14. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
2	TRX7	3G WCDMA transmit/receive port 7. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	14	TRX2	Ultra low–loss 3G WCDMA transmit/receive port 2. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
3	TRX6	3G WCDMA transmit/receive port 6. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	15	TRX1	Ultra low–loss 3G WCDMA transmit/receive port 1. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
4	TRX5	3G WCDMA transmit/receive port 5. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	16	TRX12	3G WCDMA transmit/receive port 12. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
5	TRX4	3G WCDMA transmit/receive port 4. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	17	TRX11	3G WCDMA transmit/receive port 11. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
6	TRX3	Ultra low-loss 3G WCDMA transmit/receive port 3. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	18	TRX10	3G WCDMA transmit/receive port 10. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
7	TRX13	3G WCDMA transmit/receive port 13. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.	19	TRX9	3G WCDMA transmit/receive port 9. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
8	MIPI_SELECT	MIPI interface select. When this pin is grounded, the switch is responds to any of the power mode triggers. When this pin is left open, the switch is RFFE MIPI compliant and responds to individual power mode triggers.	20	TRX8	3G WCDMA transmit/receive port 8. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
9	VDD	DC power supply	21	GND	Ground
10	VIO	MIPI decoder enable/reference voltage	22	TXHB	GSM transmit high band. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
11	SDATA	Data input/output	23	TXLB	GSM transmit low band. This pin is either connected directly to or disconnected from pin 1, depending on the applied control data.
12	SCLK	Clock signal	24	GND	Ground

Note: Bottom ground paddles must be connected to ground.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13492 are provided in Table 2. Electrical specifications are provided in Tables 3 and 4.

IMD2 and IMD3 test conditions for various frequencies are listed in Tables 5 and 6, respectively.

Triple Beat Ratio (TBR) test conditions for bands 2 and 5 are listed in Table 7. The isolation matrices shown in Tables 8 and 9 provide the port-to-port isolation and port-to-antenna isolation for all available RF states at three different frequencies: 915 MHz, 1910 MHz, and 2690 MHz.

Figure 3 illustrates the test setup used to measure intermodulation products. This industry standardized test is used to simulate the WCDMA Band 1 linearity of the antenna switch. A +20 dBm Continuous Wave (CW) signal, f_{FUND}, is sequentially applied to the TRX1 through TRX14 ports, while a –15 dBm CW blocker signal, f_{BLK}, is applied to the ANT port.

The resulting 3rd Order Intermodulation Distortion (IMD3), f_{RX}, is measured over all phases of f_{FUND}. The SKY13492 exhibits exceptional performance for all TRXx ports.

Table 10 describes the register content and programming read/write sequences. Refer to the *MIPI Alliance Specification for RF Front-End Control Interface (RFFE)*, v1.10 (26 July 2011) for additional information on MIPI programming sequences and MIPI bus specifications.

Figures 4 and 5 provide the timing diagrams for register write commands and read commands, respectively.

Table 11 provides the Register_0 logic. Table 12 describes the register parameters and bit values.

Table 2. SKY13492 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	2.5	6.0	V
MIPI decoder enable/reference voltage	VIO		2	V
Clock signal voltage	SCLK		VIO	V
Data signal voltage	SDATA		VIO	V
RF input power, all TRXx pins	P_{IN}		+31	dBm
Storage temperature	T_{STG}	–55	+150	°C
Operating temperature	T_{OP}	–30	+90	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry–standard ESD precautions should be used at all times.*

Table 3. SKY13492 DC Electrical Specifications (Note 1)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Supply voltage	V_{DD}		2.50	2.85	6.00	V
Supply current, active mode	I_{DD}			45	80	µA
Interface supply voltage	VIO		1.65	1.80	1.95	V
Interface signal: High Low	SDATA		 0.8 × VIO		 0.2 × VIO	 V V
Control current: High Low					 10 5	 µA µA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 4. SKY13492 RF Electrical Specifications (Note 1) (1 of 2)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_O] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Operating frequency	f		0.7		2.7	GHz
Insertion loss	IL	TXLB, 824 to 915 MHz		1.25		dB
		TXHB, 1710 to 1910 MHz		1.25		dB
		TRXx ports: 824 to 915 MHz 1710 to 2170 MHz		 0.50 0.65		 dB dB
		TRX4 to TRX14 ports, 1880 to 2690 MHz		 1.00		 dB
		TRX1/2/3 ports: 1880 to 2690 MHz 3500 to 3800 MHz		 0.85 1.10		 dB dB
Isolation (TRXx to any off TRXx port [non–adjacent ports])	Iso	Up to 1.0 GHz	35			dB
		Up to 2.0 GHz	30			dB
		Up to 2.7 GHz	25			dB
Isolation (TRXx to any off TRXx port [adjacent ports])	Iso	Up to 1.0 GHz	26			dB
		Up to 2.0 GHz	23			dB
		Up to 2.7 GHz	20			dB
On state match	VSWR	Up to 2.7 GHz			1.5:1	–
GSM harmonics: High band	2fo, 3fo	 P_{IN} = +33 dBm, 50 Ω P_{IN} = +33 dBm, 5:1 VSWR			 –55 –45	 dBm dBm
Low band		P_{IN} = +35 dBm, 50 Ω P_{IN} = +35 dBm, 5:1 VSWR			–55 –45	dBm dBm
TRXx harmonics	2fo, 3fo	P_{IN} = +27 dBm, 50 Ω, f = 704 to 2700 MHz			–55	dBm
		P_{IN} = +27 dBm, 5:1 VSWR, f = 704 to 2700 MHz			–55	dBm
TRX1 through TRX10, band 13 2nd harmonics	2fo	P_{IN} = +25 dBm, f = 787 MHz		–81		dBm

Table 4. SKY13492 RF Electrical Specifications (Note 1) (2 of 2)
(V_{DD} = 2.85 V, T_{OP} = +25 °C, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
2nd Order Intermodulation Distortion	IMD2	See test conditions in Table 5		–110	–105	dBm
3rd Order Intermodulation Distortion	IMD3	See test conditions in Table 6		–110	–105	dBm
Triple Beat Ratio: 650 to 900 MHz 1710 to 2155 MHz	TBR	See test conditions in Table 7		 +85 +85		 dBc dBc
Turn–on time	t_{ON}	From application of V_{DD} and VIO			20	µs
Switching speed	t_S	Port to port		2	5	µs

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 5. IMD2 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker, Low (MHz)	Frequency Blocker, High (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	190	4090	–15	2140.0
2	1880.0		80	3840		1960.0
4	1732.0		400	3864		2132.0
5	836.5		45	1718		881.5
7	2535.0		120	5187		2655.0
8	897.0		45	1839		942.0

Table 6. IMD3 Test Conditions

Band	Transmit Frequency (MHz)	Transmit Power (dBm)	Frequency Blocker (MHz)	Power Blocker (dBm)	Receive Frequency (MHz)
1	1950.0	+20	1760.0	–15	2140.0
2	1880.0		1800.0		1960.0
4	1732.0		1332.0		2132.0
5	836.5		791.5		881.5
7	2535.0		2415.0		2655.0
8	897.0		852.0		942.0

Table 7. Triple Beat Ratio Test Conditions

Band	Transmit Frequency 1 (MHz)	Transmit Power 1 (dBm)	Transmit Frequency 2 (MHz)	Transmit Power 2 (dBm)	Frequency Blocker @ ANT (MHz)	Power Blocker (dBm)	TBR Product Frequency (MHz)
2	1880.0	+21.5	1881.0	+21.5	1960.0	–30	1960.0 ± 1
5	836.5		881.5		881.5		881.5 ± 1

Table 8. Isolation Matrix: "On" Arms to "Off" Arms (1 of 2)

"On" Arms	Freq (MHz)	Isolation (dB)															
		LTX	HTX	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10	TRX11	TRX12	TRX13	TRX14
LTX	915		–31	–52	–51	–46	–42	–45	–45	–41	–46	–49	–51	–51	–52	–55	–54
LTX	1910		–26	–51	–52	–43	–42	–47	–43	–37	–37	–41	–44	–45	–49	–53	–46
LTX	2690		–16	–47	–48	–42	–41	–42	–39	–34	–33	–37	–40	–41	–44	–48	–44
HTX	915	–33		–48	–46	–53	–53	–53	–51	–46	–37	–41	–44	–57	–53	–50	–52
HTX	1910	–23		–42	–38	–45	–45	–45	–43	–37	–32	–36	–38	–47	–53	–42	–43
HTX	2690	–17		–49	–40	–49	–49	–49	–48	–47	–33	–38	–41	–33	–39	–52	–47
TRX1	915	–35	–50		–29	–52	–54	–55	–53	–49	–54	–49	–46	–43	–34	–39	–50
TRX1	1910	–34	–33		–22	–42	–43	–43	–42	–38	–42	–41	–39	–36	–27	–31	–41
TRX1	2690	–28	–30		–19	–38	–39	–38	–38	–34	–37	–37	–35	–32	–24	–27	–37
TRX2	915	–35	–55	–37		–51	–53	–54	–53	–49	–55	–51	–49	–48	–40	–36	–48
TRX2	1910	–34	–34	–29		–41	–43	–42	–42	–37	–43	–42	–41	–39	–32	–28	–39
TRX2	2690	–28	–31	–26		–37	–38	–38	–37	–34	–37	–38	–37	–35	–28	–24	–36
TRX3	915	–33	–54	–55	–52		–29	–37	–42	–45	–57	–58	–59	–58	–57	–48	–36
TRX3	1910	–31	–35	–47	–44		–23	–31	–35	–34	–44	–46	–48	–46	–47	–39	–29
TRX3	2690	–27	–32	–42	–39		–20	–28	–32	–31	–38	–41	–43	–41	–41	–35	–25
TRX4	915	–32	–51	–55	–52	–34		–29	–38	–43	–57	–58	–59	–57	–56	–49	–39
TRX4	1910	–31	–35	–46	–43	–28		–23	–31	–33	–44	–46	–47	–45	–46	–40	–32
TRX4	2690	–27	–32	–41	–38	–25		–20	–28	–29	–38	–41	–43	–40	–41	–35	–28
TRX5	915	–33	–48	–54	–52	–41	–34		–29	–36	–56	–57	–57	–55	–55	–50	–46
TRX5	1910	–32	–35	–45	–42	–35	–27		–22	–28	–44	–46	–47	–45	–45	–40	–38
TRX5	2690	–28	–33	–41	–38	–32	–25		–19	–24	–38	–41	–42	–40	–41	–36	–35
TRX6	915	–34	–46	–53	–51	–45	–41	–33		–30	–55	–56	–55	–54	–54	–50	–48
TRX6	1910	–35	–35	–44	–42	–38	–34	–26		–23	–43	–45	–46	–43	–44	–40	–40
TRX6	2690	–30	–34	–40	–37	–34	–31	–23		–19	–37	–40	–41	–39	–40	–36	–36
TRX7	915	–35	–44	–52	–51	–47	–45	–39	–36		–53	–54	–54	–52	–52	–51	–49
TRX7	1910	–39	–36	–43	–41	–39	–37	–31	–29		–41	–44	–44	–42	–43	–40	–40
TRX7	2690	–31	–36	–39	–36	–35	–33	–27	–25		–36	–39	–40	–38	–39	–35	–36
TRX8	915	–34	–42	–46	–47	–54	–55	–56	–54	–49		–30	–35	–38	–43	–50	–52
TRX8	1910	–46	–35	–39	–39	–44	–44	–44	–43	–37		–23	–28	–31	–37	–40	–42
TRX8	2690	–32	–34	–36	–35	–39	–39	–40	–39	–34		–20	–25	–27	–34	–36	–38
TRX9	915	–34	–45	–44	–46	–54	–56	–56	–53	–49	–38		–28	–35	–41	–50	–52
TRX9	1910	–40	–37	–38	–38	–44	–44	–44	–43	–38	–30		–22	–28	–35	–40	–43
TRX9	2690	–32	–44	–34	–34	–39	–40	–40	–39	–34	–26		–19	–25	–32	–36	–38
TRX10	915	–34	–46	–42	–45	–54	–56	–55	–53	–49	–40	–33		–29	–37	–49	–52
TRX10	1910	–37	–35	–36	–37	–44	–44	–44	–43	–38	–32	–27		–23	–32	–40	–42
TRX10	2690	–31	–34	–33	–33	–39	–40	–39	–39	–34	–28	–24		–20	–29	–36	–38

Table 8. Isolation Matrix: "On" Arms to "Off" Arms (2 of 2)

"On" Arms	Freq (MHz)	Isolation (dB)															
		LTX	HTX	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10	TRX11	TRX12	TRX13	TRX14
TRX11	915	–34	–47	–38	–42	–54	–55	–55	–53	–49	–43	–39	–34		–30	–48	–52
TRX11	1910	–35	–33	–32	–35	–44	–44	–44	–43	–38	–34	–32	–28		–24	–39	–42
TRX11	2690	–30	–30	–29	–32	–39	–39	–39	–38	–34	–30	–28	–25		–21	–36	–38
TRX12	915	–34	–48	–29	–35	–53	–55	–55	–54	–49	–52	–46	–42	–36		–40	–51
TRX12	1910	–35	–33	–23	–27	–43	–44	–44	–43	–38	–41	–39	–36	–29		–31	–41
TRX12	2690	–29	–30	–19	–24	–39	–39	–39	–38	–34	–36	–35	–33	–26		–27	–38
TRX13	915	–48	–72	–58	–54	–31	–37	–44	–49	–53	–65	–65	–64	–63	–61		–46
TRX13	1910	–47	–63	–55	–51	–28	–33	–40	–46	–50	–63	–62	–61	–60	–58		–38
TRX13	2690	–45	–54	–55	–53	–27	–31	–38	–44	–48	–60	–60	–59	–59	–57		–34
TRX14	915	–61	–61	–33	–17	–53	–57	–60	–63	–65	–59	–56	–51	–44	–39	–46	
TRX14	1910	–56	–47	–29	–13	–51	–54	–58	–61	–64	–57	–53	–48	–41	–36	–39	
TRX14	2690	–52	–44	–27	–10	–48	–52	–56	–60	–63	–56	–52	–47	–39	–34	–34	

Table 9. Isolation Matrix: Antenna to "Off" Arms (1 of 2)

"On" Arms	Freq (MHz)	Isolation (dB)															
		LTX	HTX	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10	TRX11	TRX12	TRX13	TRX14
LTX	915		–33	–48	–48	–40	–38	–40	–39	–34	–42	–44	–46	–47	–48	–43	–47
LTX	1910		–45	–54	–54	–45	–41	–35	–35	–32	–44	–46	–49	–51	–53	–48	–51
LTX	2690		–38	–45	–42	–43	–39	–34	–34	–32	–43	–44	–45	–44	–44	–45	–42
HTX	915	–40		–50	–49	–46	–45	–43	–42	–38	–42	–47	–49	–43	–46	–48	–47
HTX	1910	–24		–42	–40	–39	–38	–36	–35	–32	–32	–37	–38	–36	–39	–40	–39
HTX	2690	–21		–39	–36	–36	–34	–33	–32	–31	–29	–34	–35	–36	–39	–38	–36
TRX1	915	–38	–35		–36	–48	–45	–44	–44	–39	–46	–51	–54	–51	–44	–50	–40
TRX1	1910	–34	–31		–30	–41	–39	–38	–37	–33	–39	–42	–43	–39	–32	–42	–30
TRX1	2690	–28	–32		–25	–38	–36	–36	–35	–30	–35	–38	–39	–35	–28	–39	–25
TRX2	915	–38	–34	–43		–48	–46	–45	–44	–39	–46	–50	–53	–50	–45	–52	–42
TRX2	1910	–34	–30	–32		–41	–39	–39	–38	–33	–39	–42	–43	–39	–35	–43	–31
TRX2	2690	–29	–34	–28		–38	–36	–36	–35	–29	–35	–38	–40	–35	–31	–39	–26
TRX3	915	–36	–36	–49	–49		–35	–43	–48	–41	–45	–47	–47	–47	–47	–44	–52
TRX3	1910	–32	–32	–41	–38		–29	–36	–37	–32	–38	–41	–41	–40	–40	–31	–40
TRX3	2690	–27	–36	–38	–35		–24	–31	–32	–28	–35	–38	–38	–36	–37	–27	–37
TRX4	915	–36	–37	–49	–49	–45		–33	–43	–41	–45	–47	–47	–47	–48	–46	–51
TRX4	1910	–31	–33	–41	–39	–33		–28	–35	–32	–38	–41	–41	–40	–41	–34	–40
TRX4	2690	–27	–37	–38	–36	–28		–24	–30	–28	–35	–38	–38	–36	–37	–30	–36
TRX5	915	–38	–37	–50	–49	–50	–42		–35	–40	–45	–47	–48	–48	–49	–52	–51
TRX5	1910	–32	–33	–42	–40	–39	–33		–29	–30	–38	–41	–41	–40	–41	–41	–40
TRX5	2690	–27	–40	–39	–36	–35	–29		–24	–26	–35	–37	–38	–37	–38	–36	–36

Table 9. Isolation Matrix: Antenna to "Off" Arms (2 of 2)

"On" Arms	Freq (MHz)	Isolation (dB)															
		LTX	HTX	TRX1	TRX2	TRX3	TRX4	TRX5	TRX6	TRX7	TRX8	TRX9	TRX10	TRX11	TRX12	TRX13	TRX14
TRX6	915	–40	–38	–50	–49	–52	–50	–44		–37	–46	–48	–48	–48	–50	–51	–51
TRX6	1910	–34	–34	–42	–40	–41	–39	–32		–28	–39	–41	–41	–41	–42	–41	–40
TRX6	2690	–28	–43	–39	–36	–37	–34	–28		–22	–35	–37	–38	–37	–38	–37	–36
TRX7	915	–43	–39	–51	–50	–51	–51	–45	–42		–47	–49	–49	–49	–50	–51	–50
TRX7	1910	–37	–34	–42	–40	–41	–39	–34	–31		–39	–41	–42	–41	–42	–41	–40
TRX7	2690	–29	–45	–38	–36	–36	–35	–30	–27		–34	–37	–38	–37	–38	–36	–35
TRX8	915	–40	–33	–57	–53	–47	–45	–43	–43	–39		–36	–45	–49	–54	–49	–50
TRX8	1910	–37	–28	–45	–42	–40	–38	–37	–36	–32		–31	–37	–37	–44	–41	–39
TRX8	2690	–28	–27	–40	–37	–36	–35	–34	–33	–30		–26	–31	–31	–39	–37	–35
TRX9	915	–39	–35	–55	–53	–47	–45	–43	–43	–39	–41		–34	–45	–49	–49	–50
TRX9	1910	–36	–32	–45	–42	–40	–38	–37	–36	–32	–31		–29	–36	–42	–41	–39
TRX9	2690	–29	–37	–39	–37	–37	–35	–34	–34	–30	–26		–24	–31	–37	–37	–35
TRX10	915	–39	–36	–50	–53	–47	–45	–43	–43	–39	–43	–45		–35	–43	–49	–50
TRX10	1910	–35	–32	–43	–42	–40	–38	–37	–36	–32	–33	–33		–30	–38	–41	–39
TRX10	2690	–29	–41	–38	–38	–37	–35	–34	–34	–30	–29	–29		–26	–34	–38	–34
TRX11	915	–38	–35	–43	–50	–47	–45	–43	–43	–39	–42	–47	–46		–34	–49	–49
TRX11	1910	–35	–32	–38	–42	–40	–38	–37	–37	–32	–33	–36	–35		–29	–41	–39
TRX11	2690	–29	–36	–34	–37	–37	–35	–34	–34	–30	–29	–32	–30		–25	–38	–34
TRX12	915	–38	–35	–35	–45	–47	–45	–44	–43	–39	–47	–53	–51	–44		–49	–41
TRX12	1910	–34	–32	–30	–34	–40	–38	–38	–37	–33	–39	–42	–42	–35		–42	–31
TRX12	2690	–28	–32	–25	–29	–37	–36	–35	–35	–30	–35	–38	–37	–31		–38	–26
TRX13	915	–37	–33	–46	–44	–50	–46	–45	–44	–39	–46	–49	–51	–49	–44		–49
TRX13	1910	–34	–29	–36	–33	–42	–39	–39	–38	–33	–39	–41	–42	–39	–35		–42
TRX13	2690	–29	–33	–31	–28	–38	–36	–35	–34	–29	–35	–38	–39	–35	–30		–38
TRX14	915	–37	–36	–49	–49	–35	–45	–49	–48	–40	–45	–47	–47	–46	–47	–41	
TRX14	1910	–33	–32	–40	–37	–29	–35	–39	–38	–32	–38	–41	–41	–39	–40	–31	
TRX14	2690	–28	–35	–37	–34	–24	–29	–34	–33	–28	–35	–38	–38	–36	–37	–26	

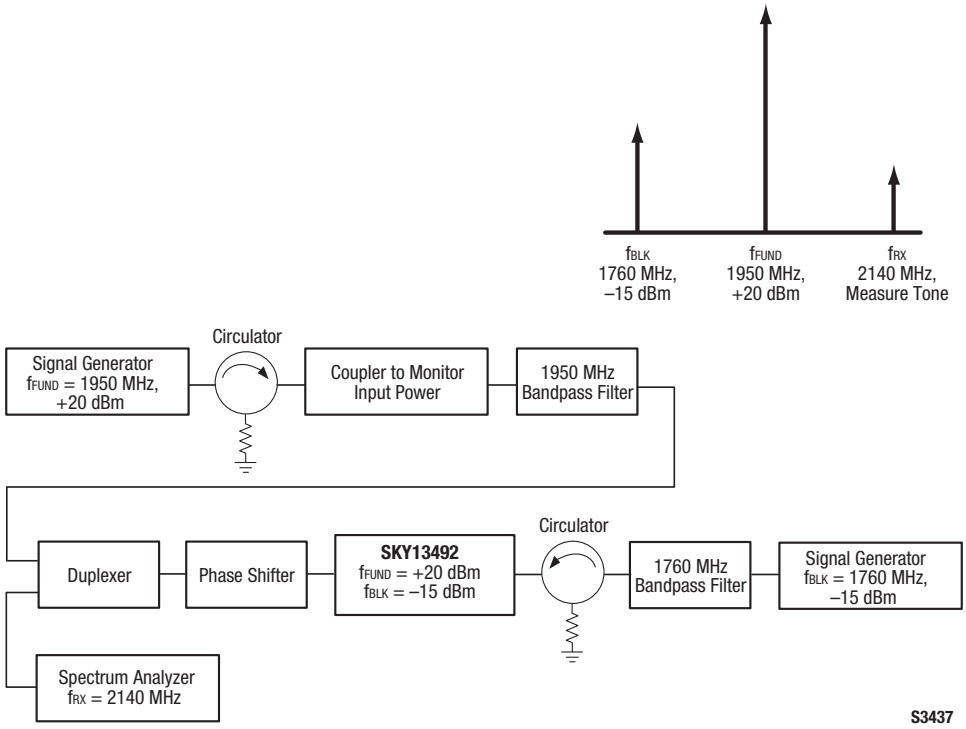


Figure 3. 3rd Order Intermodulation Test Setup

Table 10. Command Sequence Bit Definitions

Type	SSC	C11–C8	C7	C6–C5	C4	C3–C0	Parity Bits	BPC	Extended Operation					
									DA7(1)–DA0(1)	Parity Bits	BPC	DA7(n)–DA0(n)	Parity Bits	BPC
Reg0 Write	Y	SA[3:0]	1	Data[6:5]	Data[4]	Data{3:0]	Y	Y	–	–	–	–	–	–
Reg Write	Y	SA[3:0]	0	10	Addr[4]	Addr[3:0]	Y	–	Data[7:0]	–	–	–	Y	Y
Reg Read	Y	SA[3:0]	0	11	Addr[4]	Addr[3:0]	Y	Y	Data[7:0]	–	–	–	Y	Y

Legend:
SSC = Sequence start command
C = Command frame bits
DA = Data/address frame bits
BPC = Bus park cycle
BC = Byte count (# of consecutive addresses)

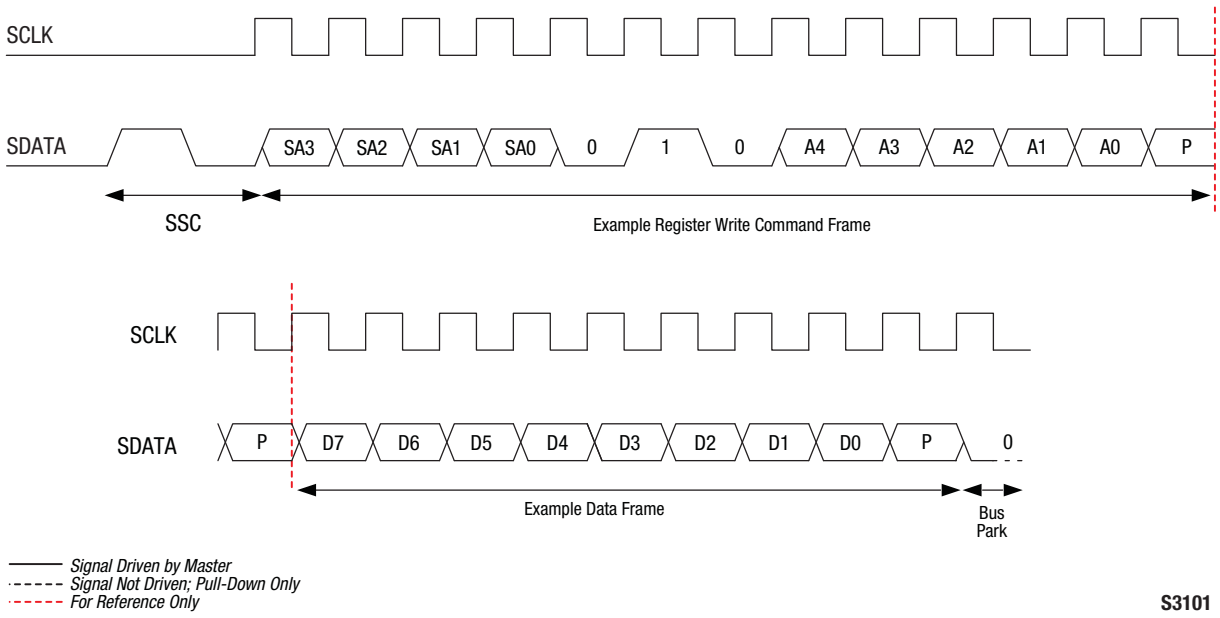


Figure 4. Register Write Command Timing Diagram

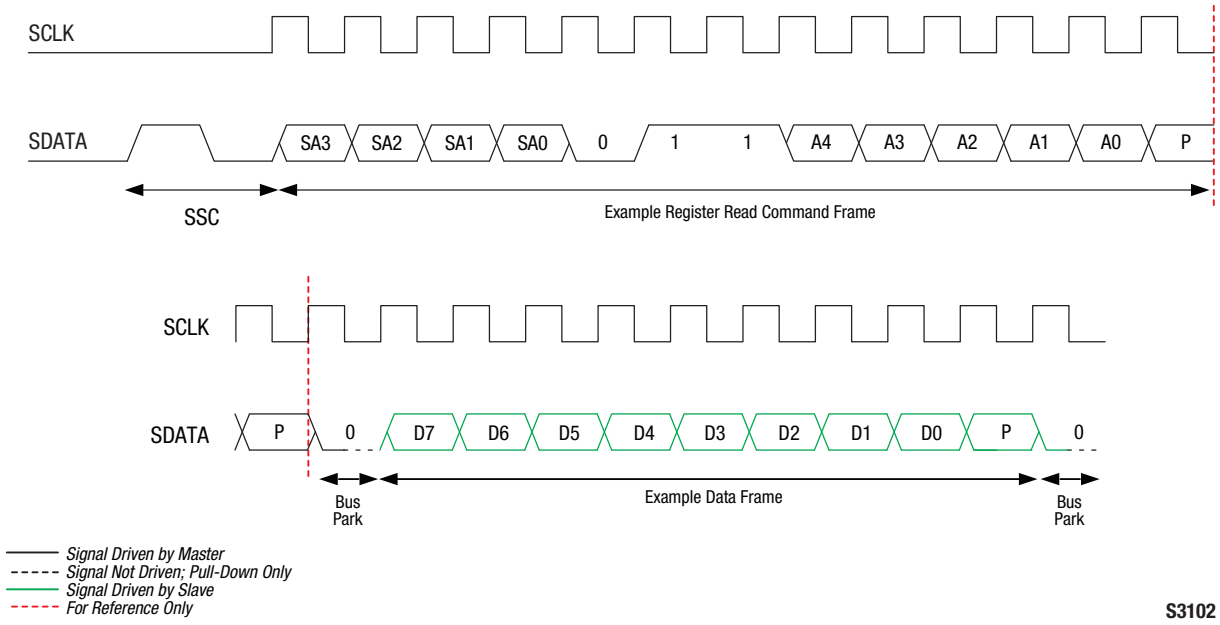


Figure 5. Register Read Command Timing Diagram

Table 11. Register_0 Truth Table

Antenna Path	Register_0 Bits							
	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
Sleep mode (standby)	X	0	0	0	0	0	0	0
2G transmit low band	X	0	0	0	1	0	1	0
2G transmit high band	X	0	0	0	1	0	0	0
TRX1	X	0	0	0	0	1	0	0
TRX2	X	0	0	0	0	1	0	1
TRX3	X	0	0	0	0	1	1	0
TRX4	X	0	0	0	0	1	1	1
TRX5	X	0	0	0	1	0	0	1
TRX6	X	0	0	0	1	0	1	1
TRX7	X	0	0	0	1	1	0	0
TRX8	X	0	0	0	0	0	0	1
TRX9	X	0	0	0	0	0	1	0
TRX10	X	0	0	0	0	0	1	1
TRX11	X	0	0	0	1	1	0	1
TRX12	X	0	0	0	1	1	1	0
TRX13	X	0	0	1	0	0	0	0
TRX14	X	0	0	1	0	0	0	1
Isolation mode (warm–up)	X	1	1	1	1	1	1	1

Table 12. Register Description and Programming (1 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
Register_0	0000	MODE_CTRL	Bits[7:0]: Switch control. See Table 8 for logic	–
RFFE_STATUS	001A	SOFTWARE RESET	Bit[7]: Resets all data to default values except for USID, GSID, or the contents of the PM_TRIG Register. 0 = Normal operation 1 = Software reset	0
		COMMAND_FRAME_PARITY_ERR	Bit[6]: Command sequence received with parity error – discard command.	0
		COMMAND_LENGTH_ERR	Bit[5]: Command length error.	0
		ADDRESS_FRAME_PARITY_ERR	Bit[4]: Address frame parity error = 1.	0
		DATA_FRAME_PARITY_ERR	Bit[3]: Data frame with parity error.	0
		READ_UNUSED_REG	Bit[2]: Read command to an invalid address.	0
		WRITE_UNUSED_REG	Bit[1]: Write command to an invalid address.	0
		BID_GID_ERR	Bit[0]: Read command with a BROADCAST_ID (refer to the *MIPI Alliance Specification*) or GSID.	0
GROUP_SID	001B	Reserved	Bits[7:4]: Reserved	0000
		GSID	Bits[3:0]: Group slave ID	0000

Table 12. Register Description and Programming (2 of 2)

Register		Parameter	Description	Default (Binary)
Name	Address (Hex)			
PM_TRIG (Note 1)	001C	PWR_MODE	Bits[7:6]: 00 = Normal operation (active) 01 = Default settings (startup) 10 = Low power (low power) 11 = Reserved	01
		Trigger_Mask_2	Bit[5]: If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	0
		Trigger_Mask_1	Bit[4]: If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	0
		Trigger_Mask_0	Bit[3]: If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	0
		Trigger_2	Bit[2]: If this bit is set, data is loaded into the trigger 2 registers.	0
		Trigger_1	Bit[1]: If this bit is set, data is loaded into the trigger 1 registers (unsupported).	0
		Trigger_0	Bit[0]: If this bit is set, data is loaded into the trigger 0 registers (unsupported).	0
PRODUCT_ID	001D	PRODUCT_ID	Bits[7:0]: This is a read–only register. However, during the programming of the Unique Slave Identifier (USID), a write command sequence is performed on this register but the value is not changed.	01011101
MANUFACTURER_ID	001E	MANUFACTURER_ID	Bits[7:0]: Read–only register	10100101
MAN_USID	001F	Reserved	Bits[7:6]: Reserved	00
		MANUFACTURER_ID	Bits[5:4]: Read–only register	01
		USID	Bits[3:0]: Programmable USID. A write to these bits programs the USID.	1011

Note 1: Unlike the complete independence between triggers 0, 1, and 2, and also between the associated trigger masks 0, 1, and 2, respectively (as described in the MIPI RFFE Specification), when pin 7 is grounded, this device uses additional interactions between the provided trigger functions.

The delayed application of updated data to all triggerable registers in this device may be accomplished using any of the three triggers (0, 1, or 2), provided that the particular trigger used is not currently masked off. If multiple triggers are enabled, any or all of those are sufficient to cause the data to be transferred from shadow registers to destination registers for all triggerable registers in the device.

It is also necessary to disable all three triggers (i.e., set all three trigger masks) to ensure that data written to any triggerable register will immediately be written to the destination register at the conclusion of the RFFE command sequence where the data is written.

Evaluation Board Description

The SKY13492 Evaluation Board is used to test the performance of the SKY13492 SP16T Switch. An Evaluation Board schematic diagram is provided in Figure 6. A recommended ESD protection circuit diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

Package Dimensions

The PCB layout footprint for the SKY13492 is provided in Figure 9. Typical case markings are shown in Figure 10. Package dimensions for the 24-pin MCM are shown in Figure 11, and tape and reel dimensions are provided in Figure 12.

Package and Handling Information

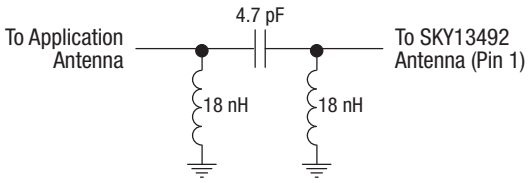
Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13492 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead–free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design and SMT Assembly/Rework Guidelines for MCM-L Packages*, document number 101752.

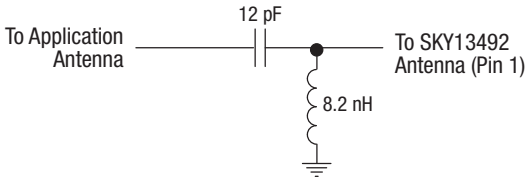
Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

***** TBD *****

Figure 6. SKY13492 Evaluation Board Schematic



ESD Circuit 1



ESD Circuit 2

S3436

Figure 7. SKY13492 Recommended ESD Protection Circuits

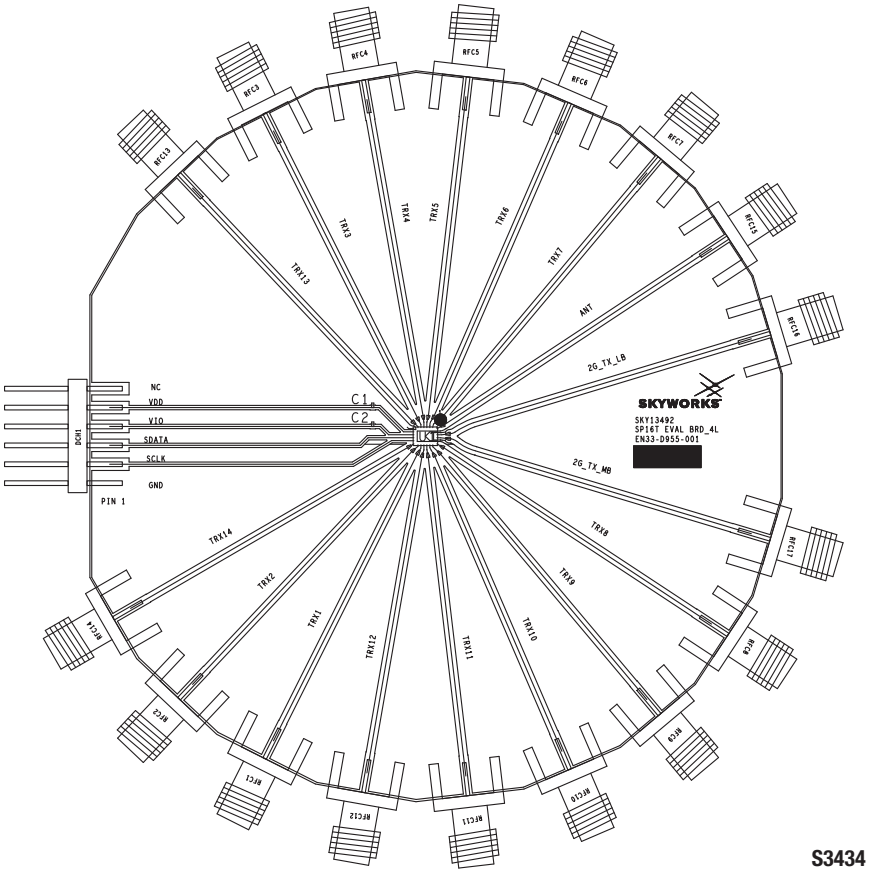


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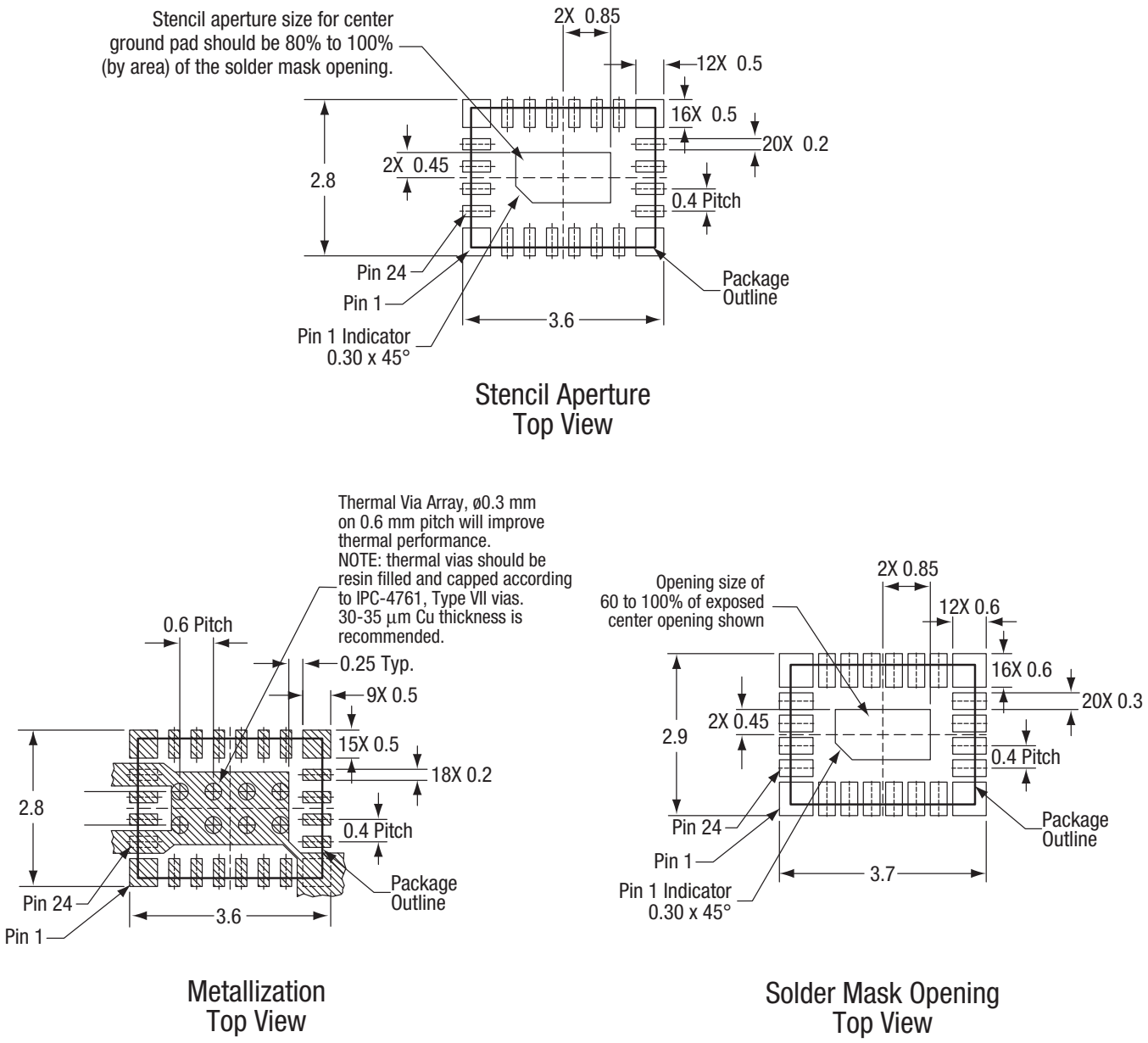
Figure 8. SKY13492 Evaluation Board Assembly Diagram

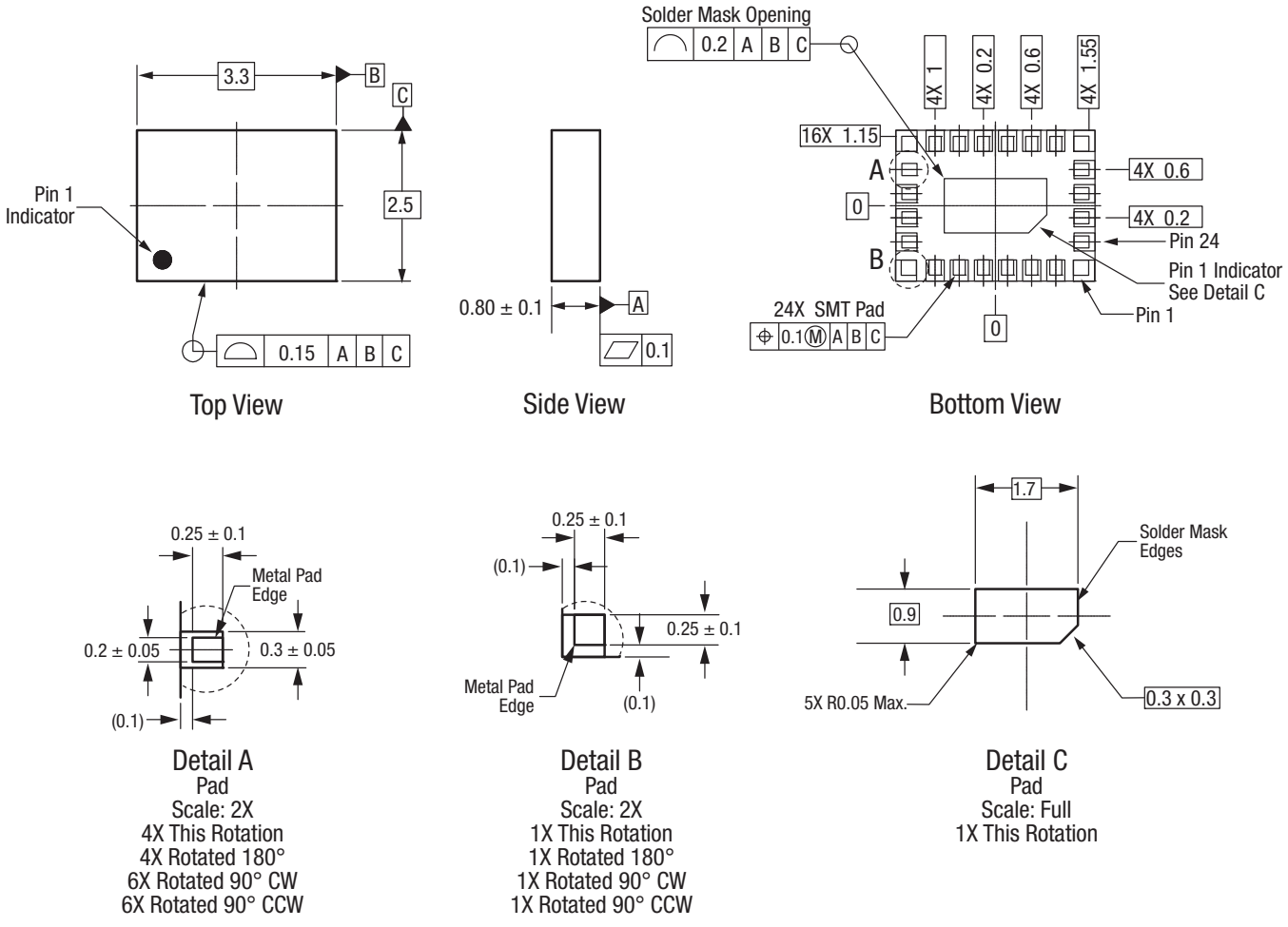


All dimensions are in millimeters **S3435**

Figure 9. SKY13492 PCB Layout Footprint (Top View)

***** TBD *****

Figure 10. Typical Part Markings (Top View)



All measurements are in millimeters
Dimensioning and tolerancing according to ASME Y14.5M-1994

S3421

Figure 11. SKY13492 24-Pin MCM Package Dimensions

*** TBD ***

Figure 12. SKY13492 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13492 0.4 to 3.8 GHz SP16T Antenna Switch with MIPI Interface	SKY13492	***** TBD *****