AWT6635

HELP3DC™ (Band 5)
LTE/WCDMA/CDMA Linear PA Module

PRELIMINARY DATASHEET - Rev 1.3

FEATURES

- CDMA/EVDO, WCDMA/HSPA and LTE compliant
- 3rd Generation HELP™ technology
- High Efficiency: (R99 waveform)
  - 40 % @ POUT = +28.5 dBm
  - 21.5 % @ POUT = +17 dBm
- Simpler Calibration with only 2 Bias modes
- Optimized for SMPS Supply
- Low Quiescent Current: 9 mA
- Low Leakage Current in Shutdown Mode: <5 μA
- Internal Voltage Regulator
- Integrated "daisy chainable" directional couplers with CPLIN and CPLOUT Ports
- Optimized for a 50 Ω System
- Low Profile Miniature Surface Mount Package
- Internal DC blocks on IN/OUT RF ports
- 1.8 V Control Logic
- RoHS Compliant Package, 260 °C MSL-3

10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module

APPLICATIONS

- Wireless Handsets and Data Devices for:
  - WCDMA/HSPA and LTE Cell-Band
  - CDMA/EVDO Band Class 0 & 10

PRODUCT DESCRIPTION

The AWT6635 PA is designed to provide highly linear output for WCDMA ,CDMA and LTE handsets and data devices with high efficiency at both high and low power modes. This HELP3DC™ PA can be used with an external switch mode power supply (SMPS) to improve its efficiency and reduce current consumption further at medium and low output powers. A "daisy chainable" directional coupler is integrated in the module thus eliminating the need of external couplers. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. There are two selectable bias modes that optimize efficiency for different output power levels, and a shutdown mode with low leakage current, which increases handset talk and standby time. The self-contained 3 mm x 3 mm x 1 mm surface mount package incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.

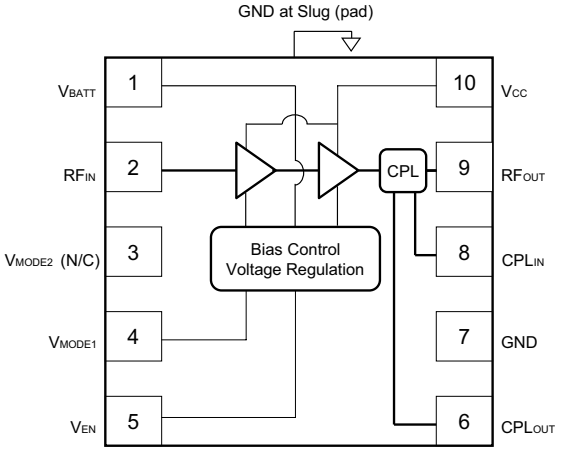


Figure 1: Block Diagram

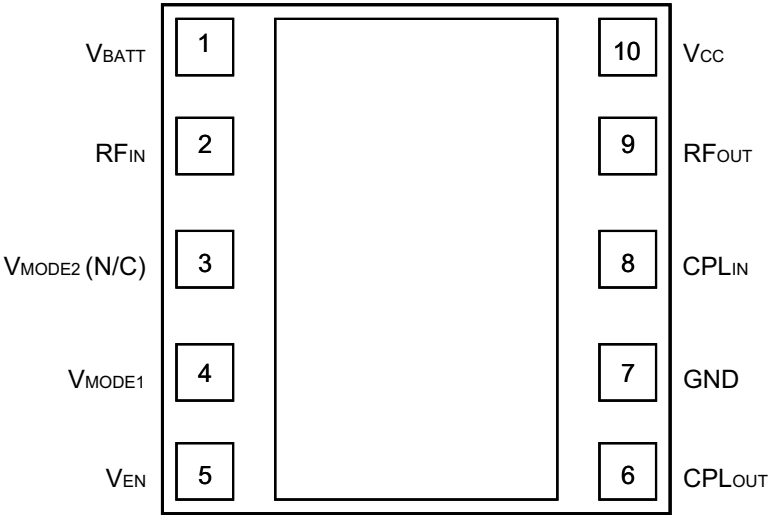


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION
1	V_{BATT}	Battery Voltage
2	RF_{IN}	RF Input
3	V_{MODE2} (N/C)	No Connection
4	V_{MODE1}	Mode Control Voltage 1
5	V_{EN}	PA Enable Voltage
6	CPL_{OUT}	Coupler Output
7	GND	Ground
8	CPL_{IN}	Coupler Input
9	RF_{OUT}	RF Output
10	V_{CC}	Supply Voltage

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{CC})	0	+5	V
Battery Voltage (V_{BATT})	0	+6	V
Control Voltages (V_{MODE1}, V_{ENABLE})	0	+3.5	V
RF Input Power (P_{IN})	-	+10	dBm
Storage Temperature (T_{STG})	-40	+150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (f)	814	-	849	MHz	
Supply Voltage (V_{CC})	+0.5	+3.4	+4.35	V	P_{OUT} ≤+28.5 dBm
Battery Voltage (V_{BATT})	+3.1	+3.4	+4.35	V	P_{OUT} ≤+28.5 dBm
Enable Voltage (V_{ENABLE})	+1.35 0	+1.8 0	+3.1 +0.5	V	PA "on" PA "shut down"
Mode Control Voltage (V_{MODE1})	+1.35 0	+1.8 0	+3.1 +0.5	V	Low Bias Mode High Bias Mode
RF Output Power (P_{OUT}) R99 WCDMA, HPM HSPA (MPR=0), HPM LTE, HPM R99 WCDMA, LPM HSPA (MPR=0), LPM LTE, LPM	 27.7(1) 26.7(1) 26.7(1) 16.2(1) 15.2(1) 15.2(1)	 28.5 27.5 27.5 17 16 16	 28.5 27.5 27.5 17 16 16	dBm	 3GPP TS 34.121-1, Rel 8 Table C.11.1.3 for WCDMA SUBTEST 1 TS 36.101 Rel 8 for LTE
CDMA Output Power HPM LPM	 26.7(1) 15.2(1)	 27.5 16.0	 27.5 16.0	dBm	CDMA2000, RC1
Case Temperature (T_C)	-30	-	+90	°C	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Notes:

(1) For operation at V_{CC} = +3.1 V, P_{OUT} is derated by 0.8 dB.

Table 4: Electrical Specifications - WCDMA Operation (R99 waveform)
(T_C = +25 °C, V_{CC} = +3.4 V, V_{BATT} = +3.4 V, V_{ENABLE} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
					P_{OUT}	V_{MODE1}
Gain	25.5 13	28.5 16	31 18	dB	+28.5 dBm +17 dBm	0 V 1.8 V
ACLR1 at 5 MHz offset (1)	- -	-41 -41	-38 -38	dBc	+28.5 dBm +17 dBm	0 V 1.8 V
ACLR2 at 10 MHz offset (1)	- -	-56 -56	-48 -48	dBc	+28.5 dBm +17 dBm	0 V 1.8 V
Power-Added Efficiency (1)	- -	40 21.5	- -	%	+28.5 dBm +17 dBm	0 V 1.8 V
Quiescent Current (Icq) Low Bias Mode	-	9	11	mA	V_{MODE1} = +1.8 V	
Mode Control Current	-	0.06	0.15	mA	through V_{MODE} pin, V_{MODE1} = +1.8 V	
Enable Current	-	0.4	0.6	mA	through V_{ENABLE} pin	
BATT Current	-	3.0	5	mA	through V_{BATT} pin, V_{MODE1} = +1.8 V	
Leakage Current	-	4	-	µA	V_{BATT} = +4.2 V, V_{CC} = +4.2 V, V_{ENABLE} = 0 V, V_{MODE1} = 0 V	
Noise in Receive Band(2)	-	-133	-131	dBm/Hz	$P_{OUT} \leq$ +28.5 dBm, V_{MODE1} = 0V	
	-	-137	-135	dBm/Hz	$P_{OUT} \leq$ 17 dBm, V_{MODE1} = +1.8 V	
Harmonics 2fo 3fo, 4fo	- -	-40 -60	-35 -45	dBc	$P_{OUT} \leq$ +28.5 dBm	
Input Impedance	-	-	2:1	VSWR		
Coupling Factor	-	20	-	dB		
Directivity	-	20	-	dB		
Coupler In-Out Daisy Chain Insertion Loss	-	<0.25	-	dB	698 MHz to 2620 MHz Pin 8 to 6 Shutdown Mode	
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	$P_{OUT} \leq$ +28.5 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions	
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range	
Phase Delta (HPM-LPM)	-	10	-	Deg		

Notes:
(1) ACLR and Efficiency measured at 836.5 MHz.
(2) 869 MHz to 894 MHz.

Table 5: Electrical Specifications - LTE Operation (RB = 12, START = 0, QPSK)
(T_C = +25 °C, V_{CC} = V_{BATT} = +3.4 V, V_{ENABLE} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
					P_{OUT}	V_{MODE1}
Gain	25.5 13	28.5 16	31 18	dB	+27.5 dBm +16 dBm	0 V 1.8 V
ACLR E-UTRA at ± 10 MHz offset	- -	-39 -38	- -	dBc	+27.5 dBm +16 dBm	0 V 1.8 V
ACLR1 UTRA (1) at ± 7.5 MHz offset	- -	-40 -39	- -	dBc	+27.5 dBm +16 dBm	0 V 1.8 V
ACLR2 UTRA at ± 12.5 MHz offset	- -	-60 -60	- -	dBc	+27.5 dBm +16 dBm	0 V 1.8 V
Power-Added Efficiency (1)	- -	36 19	- -	%	+27.5 dBm +16 dBm	0 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	<-70	dBc	P_{OUT} ≤ +27.5 dBm In-band load VSWR < 5:1 Out-of-band load VSWR < 10:1 Applies over all operating conditions	
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over full operating range	

Notes:
(1) ACLR and Efficiency measured at 836.5 MHz.

Table 6: Electrical Specifications - CDMA2000 Operation (RC-1 waveform)
(T_C = +25 °C, V_{CC} = +3.4 V, V_{BATT} = +3.4 V, V_{ENABLE} = +1.8 V, 50 Ω system)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS	
					P_{OUT}	V_{MODE1}
Gain	25.5 13	28.5 16	31 18	dB	P_{OUT} = +27.5 dBm P_{OUT} = +16 dBm	0 V 1.8 V
Adjacent Channel Power at ±885 kHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	- -	-51 -50	- -	dBc	P_{OUT} = +27.5 dBm P_{OUT} = +16 dBm	0 V 1.8 V
Adjacent Channel Power at ±1.98 MHz offset (1) Primary Channel BW = 1.23 MHZ Adjacent Channel BW = 30 kHz	- -	-61 -59	- -	dBc	P_{OUT} = +27.5 dBm P_{OUT} = +16 dBm	0 V 1.8 V
Power-Added Efficiency (1)	- -	36 19	- -	%	P_{OUT} = +27.5 dBm P_{OUT} = +16 dBm	0 V 1.8 V
Spurious Output Level (all spurious outputs)	-	-	-70	dBc	$P_{OUT} \leq$ +27.5 dBm In-band Load VSWR < 5:1 Out-of-band Load VSWR < 10:1 Applies over all operating conditions	
Load mismatch stress with no permanent degradation or failure	8:1	-	-	VSWR	Applies over all operating conditions	

PERFORMANCE DATA PLOTS:
(WCDMA Operation at 836.5 MHz and 50 Ω system)

Figure 3: WCDMA Gain (dB) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

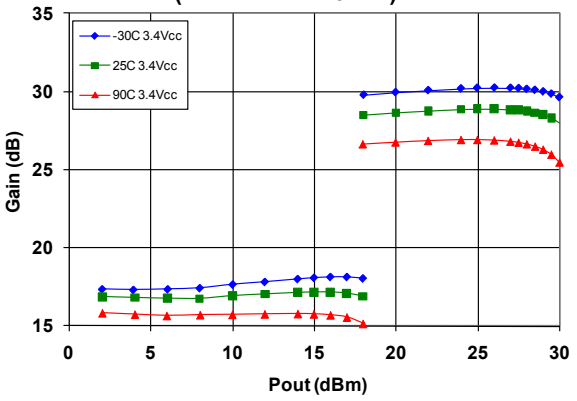


Figure 4: WCDMA Gain (dB) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

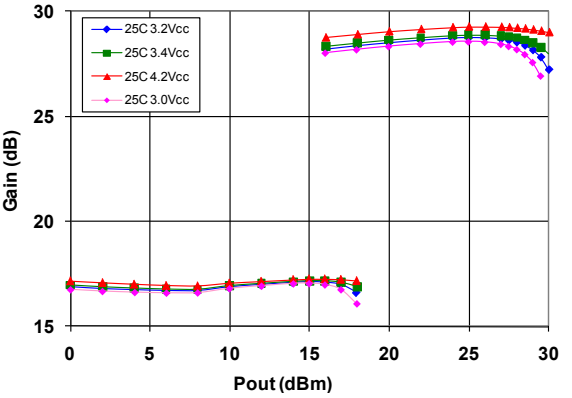


Figure 5: WCDMA PAE (%) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

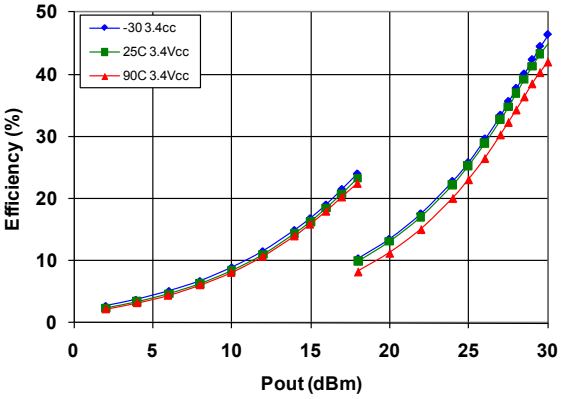


Figure 6: WCDMA PAE (%) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

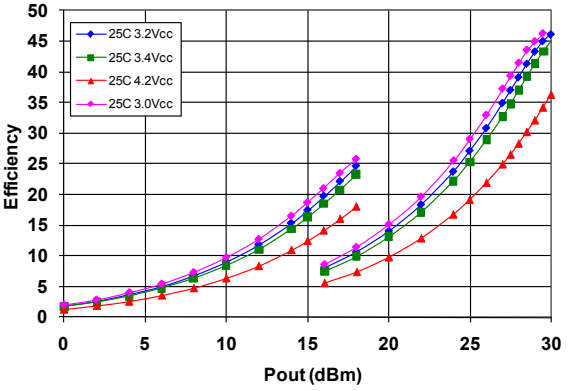


Figure 7: WCDMA ACLR1 (dBc) over Temperature (V_{BATT} = V_{CC} = 3.4 V)

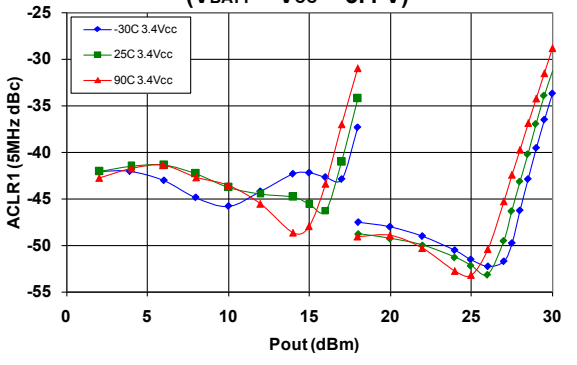
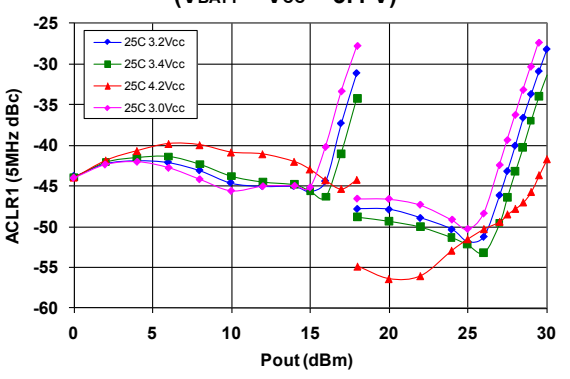


Figure 8: WCDMA ACLR1 (dBc) over Temperature (V_{BATT} = V_{CC} = 3.4 V)



APPLICATION INFORMATION

To ensure proper performance, refer to all related Application Notes on the ANADIGICS web site: http://www.anadigics.com

Shutdown Mode

The power amplifier may be placed in a shutdown mode by applying logic low levels (see Operating Ranges table) to the V_{ENABLE} and V_{MODE1} voltages.

Bias Modes

The power amplifier may be placed in either a Low Bias mode or a High Bias mode by applying the appropriate logic level (see Operating Ranges table) to V_{MODE1}. The Bias Control table lists the recommended modes of operation for various applications. V_{MODE2} is not necessary for this PA.

Two operating modes are available to optimize current consumption. High Bias/High Power operating mode is for P_{OUT} levels $\geq$ 16 dBm. At around 17 dBm output power, the PA can be "Mode Switched" to Low power mode for lowest quiescent current consumption.

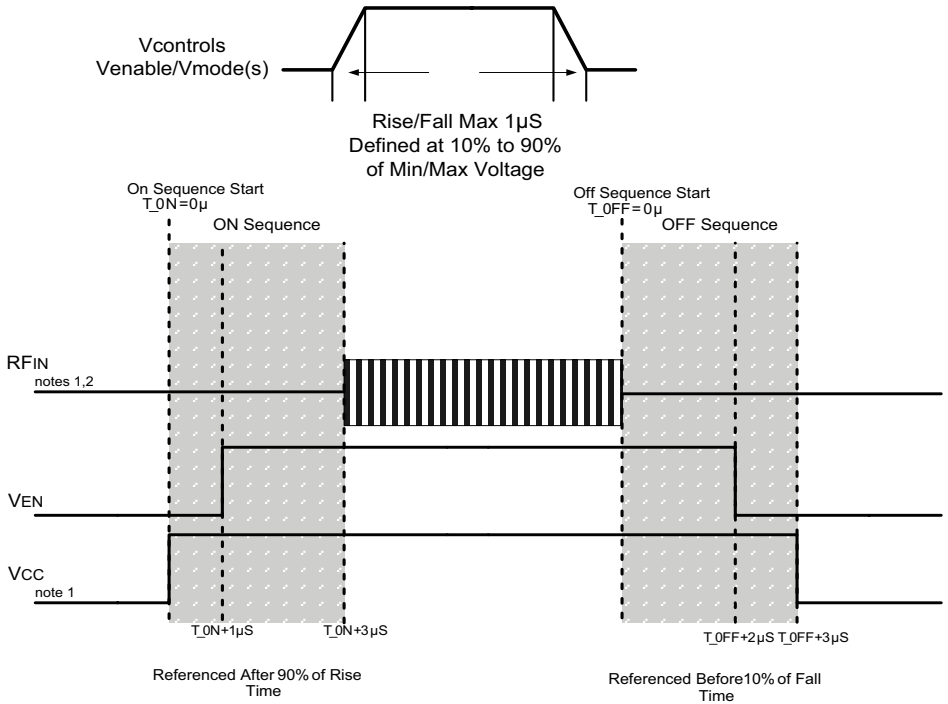


Figure 9: Recommended ON/OFF Timing Sequence

Notes:
(1) Level might be changed after RF is ON.
(2) RF OFF defined as $P_{IN} \leq$ -30 dBm.
(3) Switching simultaneously between V_{MODE} and V_{EN} is not recommended.

Table 7: Bias Control

APPLICATION	P_{OUT} LEVELS	BIAS MODE	V_{ENABLE}	V_{MODE1}	V_{CC}	V_{BATT}
High power (High Bias Mode)	> +16 dBm	High	+1.8 V	0 V	1.5 - 4.35 V	> 3.1 V
Med/low power (Low Bias Mode)	≤ +17 dBm	Low	+1.8 V	+1.8 V	0.5 - 4.35 V	> 3.1 V
Shutdown	-	Shutdown	0 V	0 V	0.5 - 4.35 V	> 3.1 V

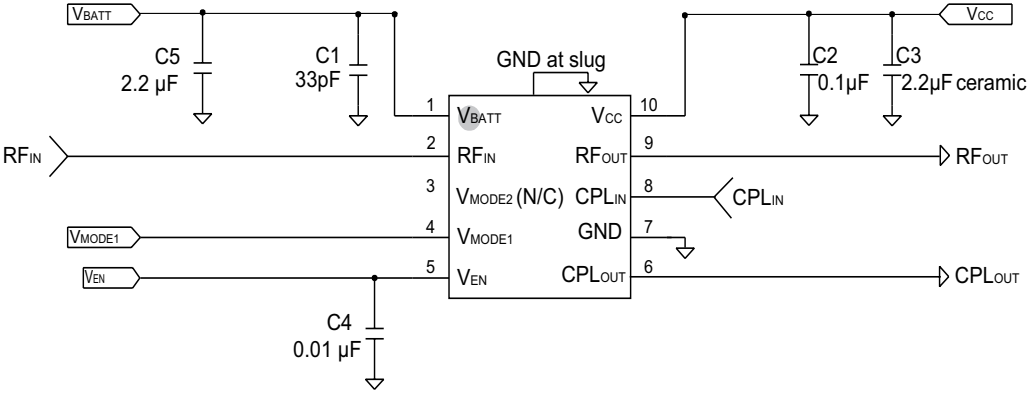


Figure 10: Evaluation Circuit Schematic

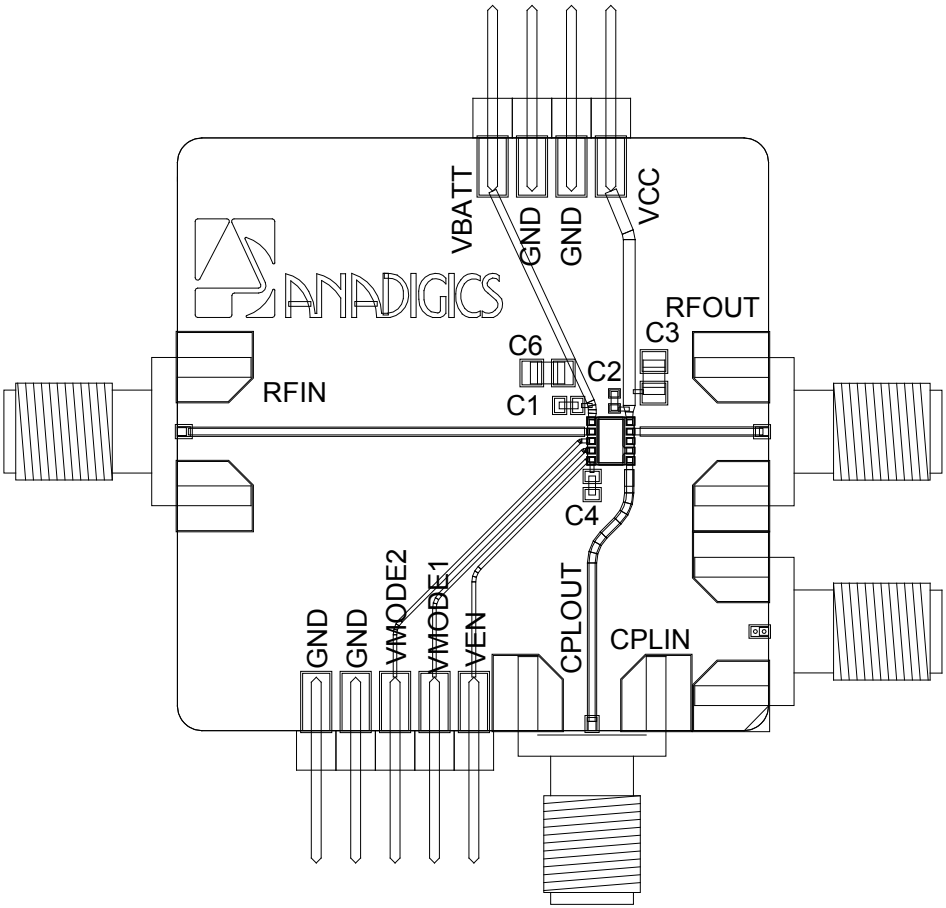


Figure 11: Evaluation Board Layout

HELP3DC™

The AWT6635 power amplifier module is based on ANADIGICS proprietary HELP3DC™ technology. The PA is designed to operate up to 17 dBm in the low power mode, thus eliminating the need for three gain state, while still maintaining low quiescent current and high efficiency in low and medium power levels. Average weighted efficiency can be increased by using an external switch mode power supply (SMPS) or DC/DC converter to reduce V_{CC}.

The directional “daisy chainable” coupler is integrated within the PA module, therefore there is no need for external couplers.

The AWT6635 has an integrated voltage regulator, which eliminates the need for an external constant voltage source. The PA is turn on/off is controlled by V_{EN} pin. A single V_{MODE} control logic (V_{MODE1}) is needed to operate this device.

AWT6635 requires only two calibration sweeps for system calibration, thus saving calibration time.

Figure 11 shows one application example on mobile board. C1 and C2 are RF bypass caps and should be placed nearby pin 1 and pin 10. Bypass caps C4 and C5 may not be needed. Also a “T” matching topology is recommended at PA RF_{IN} and RF_{OUT} ports to provide matching between input TX Filter and Duplexer / Isolator.

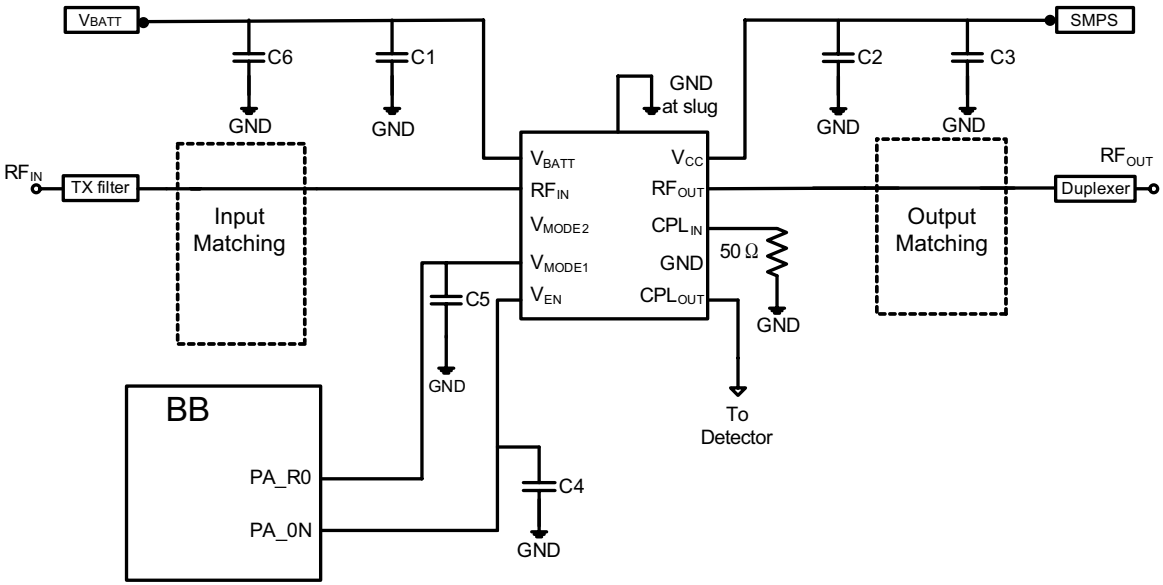
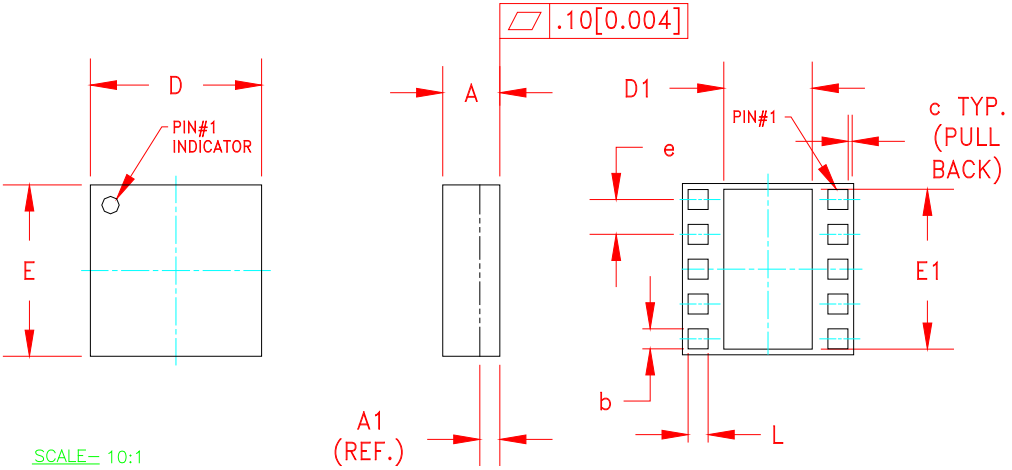


Figure 12: Typical Application Circuit

PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.91	1.03	1.13	0.035	0.041	0.044	–
A1	PLEASE REFER TO LAMINATE CONTROL DRAWING						–
b	0.32	0.35	0.40	0.013	0.014	0.016	3
c	–	0.10	–	–	0.004	–	–
D	2.88	3.00	3.12	0.113	0.118	0.123	–
D1	1.45	1.50	1.57	0.057	0.059	0.062	3
E	2.88	3.00	3.12	0.113	0.118	0.123	–
E1	2.70	2.75	2.85	0.106	0.108	0.112	3
e		0.60			0.024		3
L	0.32	0.35	0.40	0.013	0.014	0.016	3

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.
4. UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
5. LAMINATE CONTROL DRAWING SPECIFIED BY PART NUMBER.

Figure 13: Package Outline - 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module

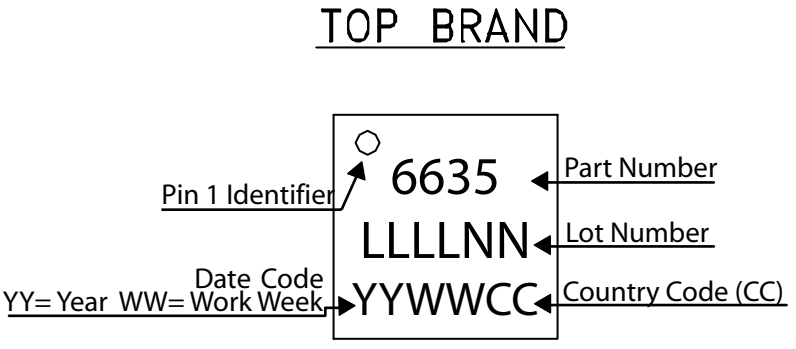
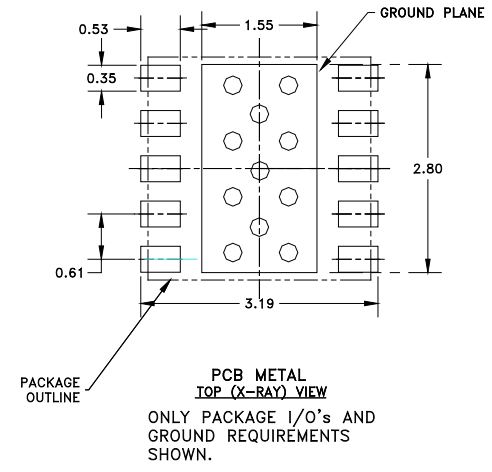


Figure 14: Branding Specification Package

PCB AND STENCIL DESIGN GUIDELINE



NOTES:

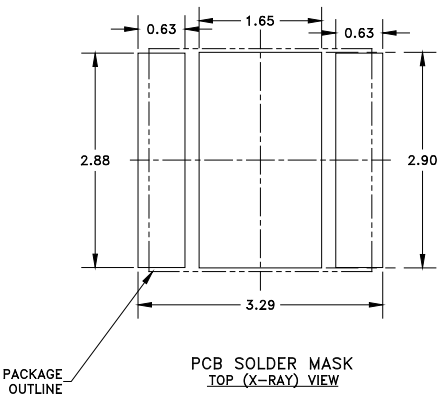
(1) OUTLINE DRAWING REFERENCE: P8002478_E

(2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.

(3) DIMENSIONS IN MILLIMETERS.

(4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.

(5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)



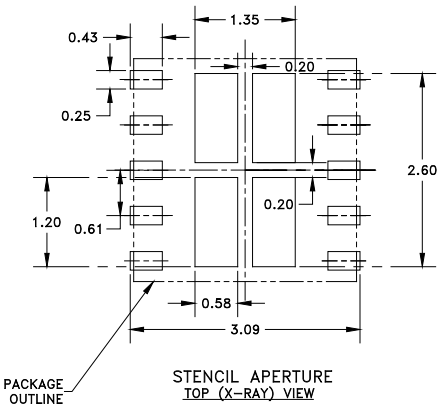
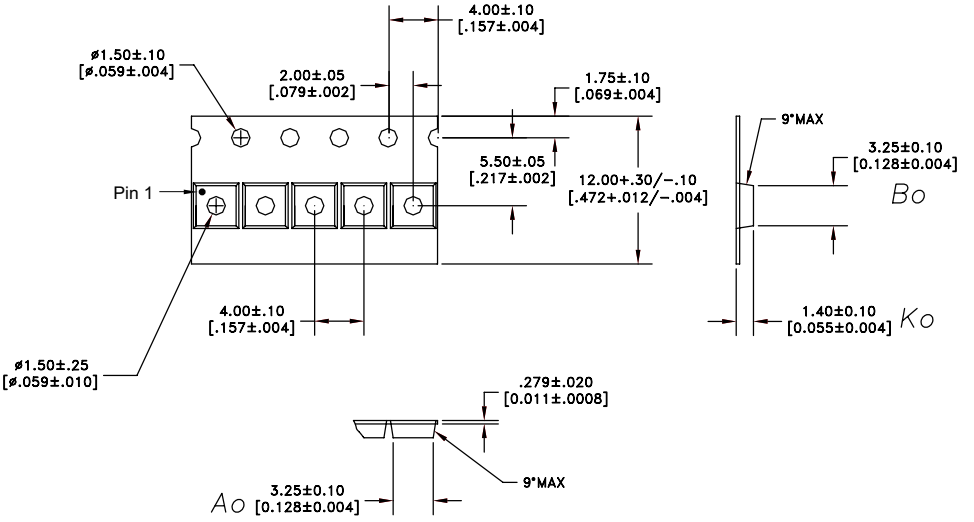


Figure 15: Recommended PCB Layout Information

COMPONENT PACKAGING



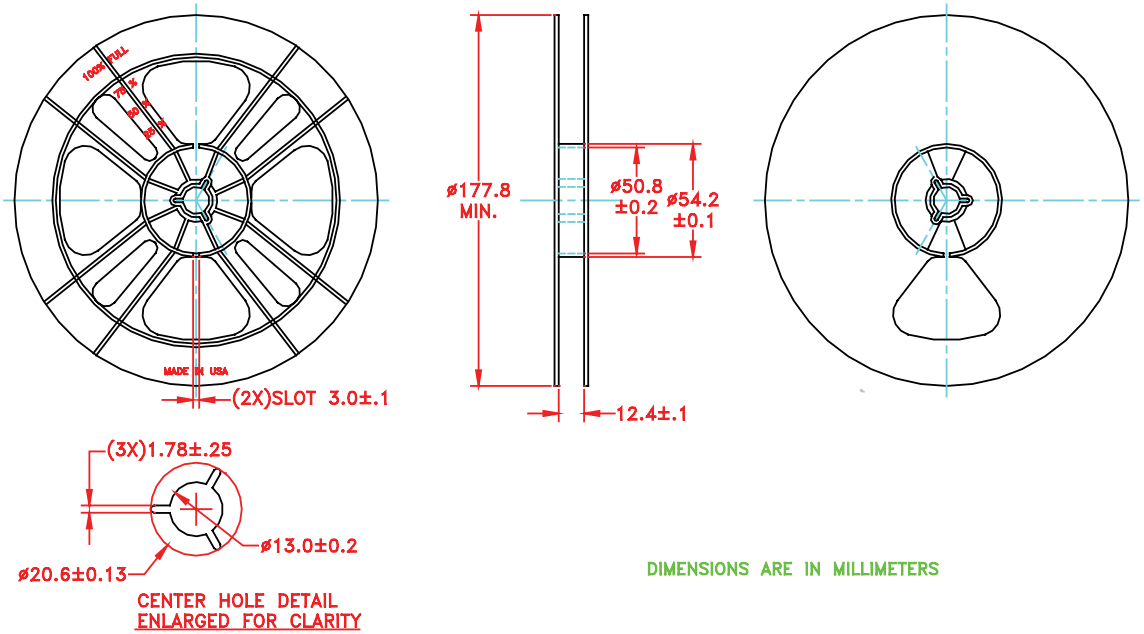
NOTES:

1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 16: Carrier Tape



DIMENSIONS ARE IN MILLIMETERS

NOTES:

1. MATERIAL: BLACK CARBON POLYSTYRENE
SURFACE RESISTIVITY: $1X10^4$ TO $1X10^5$ ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

Figure 17: Reel

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6635Q7	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Tape and Reel, 2500 pieces per Reel
AWT6635P9	-30 °C to +90 °C	RoHS Compliant 10 Pin 3 mm x 3 mm x 1 mm Surface Mount Module	Partial Tape and Reel

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