MASW-00x102 Series

HMIC™ Silicon PIN Diode Switches with Integrated Bias Network

Rev. V5

Features

- Broad Bandwidth Specified 2 - 18 GHz
- Usable up to 26 GHz
- Integrated Bias Network
- Lower Insertion Loss / Higher Isolation
- Fully Monolithic, Glass Encapsulated Chip
- Up to +33 dBm CW Power Handling @ +25°C
- RoHS* Compliant

Description

The MASW-002100 (SP2T) and MASW-3102 (SP3T) broadband switches with an integrated bias networks utilizing MACOM's HMIC™ (Heterolithic Microwave Integrated Circuit) process, US Patent 5,268,310. This process allows the incorporation of silicon pedestals that form series and shunt diodes or vias by imbedding them in low loss, low dispersion glass. By using small spacing between circuit elements, this combination of silicon and glass gives HMIC devices low loss and high isolation performance with exceptional repeatability through low millimeter frequencies.

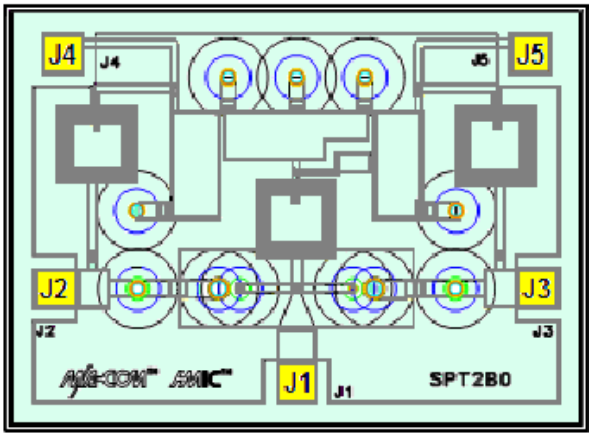
The top side of the chip is protected by a polymer coating for manual or automatic handling and large gold bond pads help facilitate connection of low inductance ribbons. The gold metallization on the backside of the chip allows for attachment via 80/20 (gold/tin) solder or conductive silver epoxy.

Ordering Information

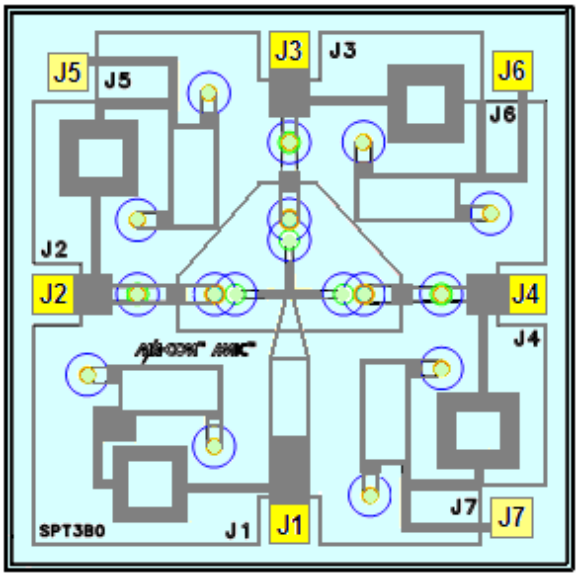
Part Number	Package xx = 0G	Package xx = 0W
MASW-002102-1358(xx)	Gel Pack	Waffle Pack
MASW-003102-1359(xx)	Gel Pack	Waffle Pack

Functional Diagrams[1]

MASW-002102 (SP2T)



MASW-003102 (SP3T)



1. Yellow areas indicate ribbon/wire bonding pads

*Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Electrical Specifications: T_A = 25°C, 20 mA

MA4SW210B-1 (SPDT)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	2 GHz 6 GHz 12 GHz 18 GHz	dB	—	1.5 0.7 0.9 1.2	1.8 1.0 1.2 1.8
Isolation	2 GHz 6 GHz 12 GHz 18 GHz	dB	55 47 40 36	60 50 45 40	—
Input Return Loss	2 GHz 6 GHz 12 GHz 18 GHz	dB	—	14 15 15 13	—
Switching Speed[2]	—	ns	—	50	—

MA4SW310B-1 (SP3T)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Insertion Loss	2 GHz 6 GHz 12 GHz 18 GHz	dB	—	1.6 0.8 1.0 1.3	2.0 1.1 1.3 1.9
Isolation	2 GHz 6 GHz 12 GHz 18 GHz	dB	54 47 40 36	59 50 45 40	—
Input Return Loss	2 GHz 6 GHz 12 GHz 18 GHz	dB	—	14 15 16 14	—
Switching Speed[2]	—	ns	—	50	—

1. Typical switching speed is measured from (10% to 90% and 90% to 10% of detected RF voltage), driven by TTL compatible drivers. In the modulating state, (the switching port is modulating, all other ports are in steady state isolation.) The switching speed is measured using an RC network using the following values: R = 50 - 200 Ω, C = 390 - 1000 pF. Driver spike current, I_C = C dv/dt, ratio of spike current to steady state current, is typically 10:1.

Absolute Maximum Ratings[3,4,5]

Parameter	Absolute Maximum
RF CW Incident Power	+33 dBm
Reverse Voltage	-50 V
Bias Current per Port	±50 mA @ +25°C
Operating Temperature	-65°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+175°C

3. Exceeding any one or combination of these limits may cause permanent damage to this device.
4. MACOM does not recommend sustained operation near these survivability limits.
5. Maximum operating conditions for a combination of RF power, DC bias and temperature: +33 dBm CW @ 15 mA (per diode) @ +85°C.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 0 (HBM) and Class C1 (CDM).devices.

Cleanliness

The chips should be handled in a clean environment free of dust and organic contamination.

Wire / Ribbon Bonding

Thermo compression wedge bonding using 0.003" x 0.00025" ribbon or 0.001" diameter gold wire is recommended. A work stage temperature of 150°C - 200°C, tool tip temperature of 120°C - 150° and a downward force of 18 to 22 grams should be used. If ultrasonic energy is necessary, it should be adjusted to the minimum level required to achieve a good bond. Excessive power or force will fracture the silicon beneath the bond pad causing it to lift. RF bond wires and ribbons should be kept as short as possible for optimum RF performance.

Chip Mounting

HMIC switches have Ti-Pt-Au backside metallization and can be mounted using a gold-tin eutectic solder or conductive epoxy. Mounting surface must be free of contamination and flat.

Eutectic Die Attachment

An 80/20, gold-tin, eutectic solder is recommended. Adjust the work surface temperature to 255°C and the tool tip temperature to 265°C. After placing the chip onto the circuit board re-flow the solder by applying hot forming gas (95/5 Ni/H) to the top surface of the chip. Temperature should be approximately 290°C and not exceed 320°C for more than 20 seconds. Typically no more than three seconds is necessary for attachment. Solders rich in tin should be avoided

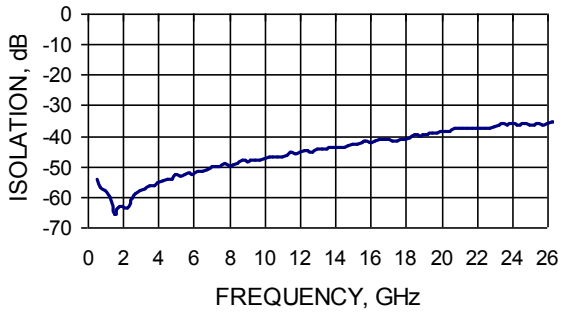
Epoxy Die Attachment

A minimum amount of epoxy, 1 - 2 mils thick, should be used to attach chip. A thin epoxy fillet should be visible around the outer perimeter of the chip after placement. Epoxy cure time is typically 1 hour at 150°C.

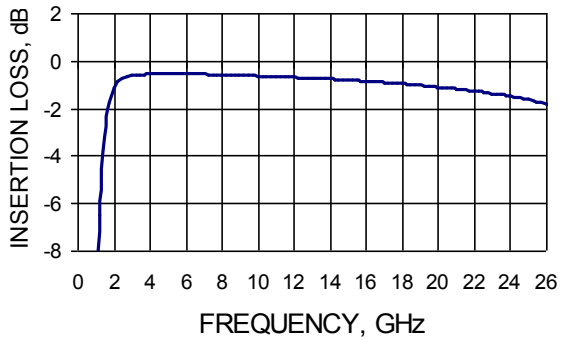
Typical RF Performance at T_{AMB} = +25°C, 20 mA Bias Current

MASW-002102

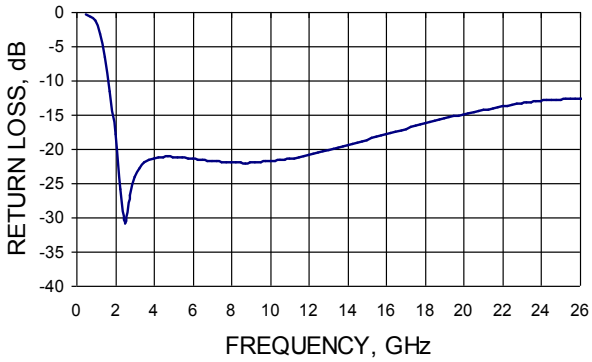
Isolation



Insertion Loss

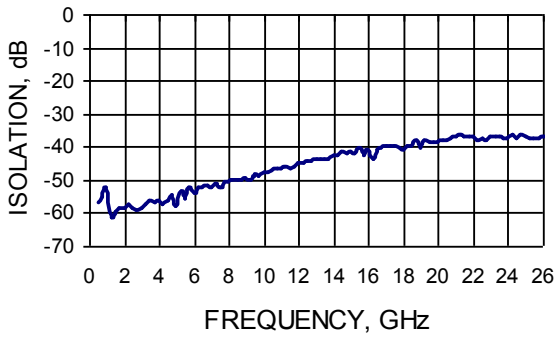


Return Loss

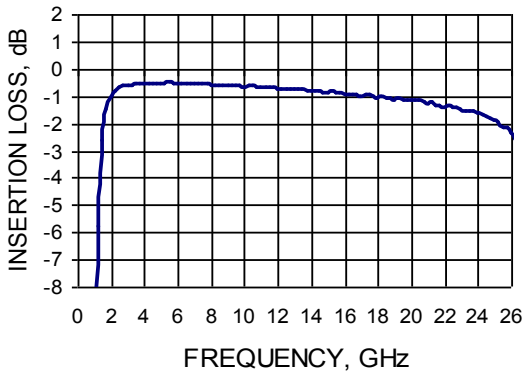


MASW-003102

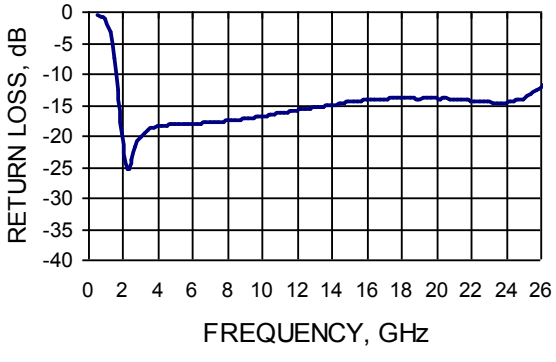
Isolation

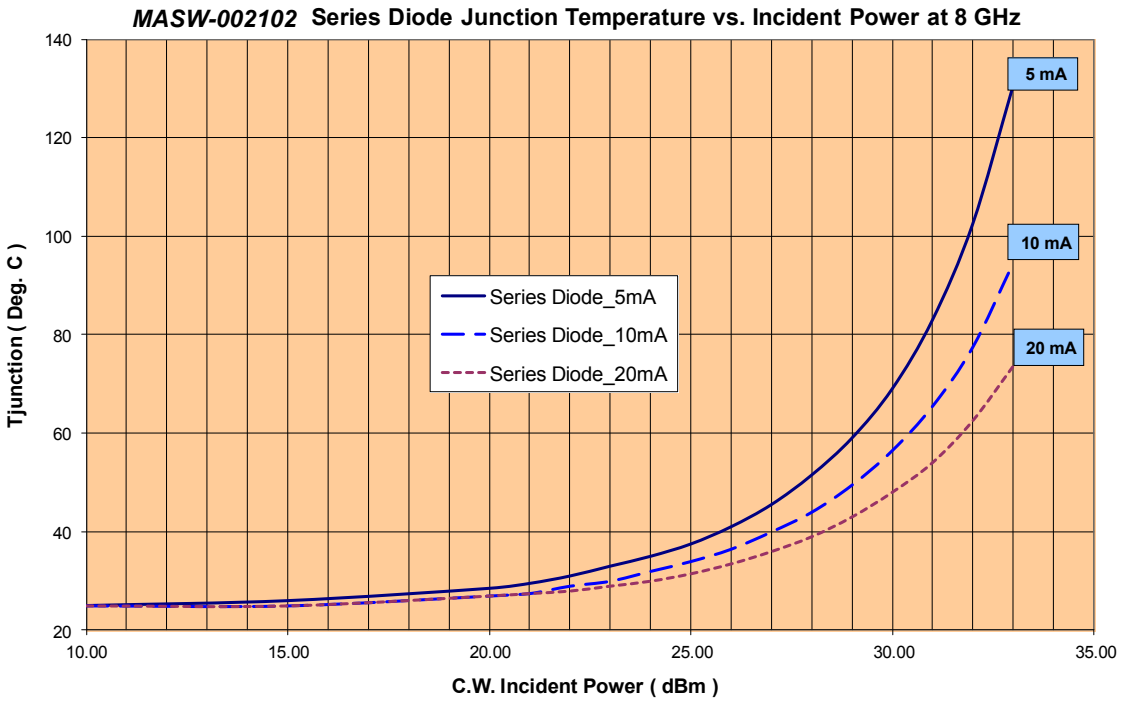


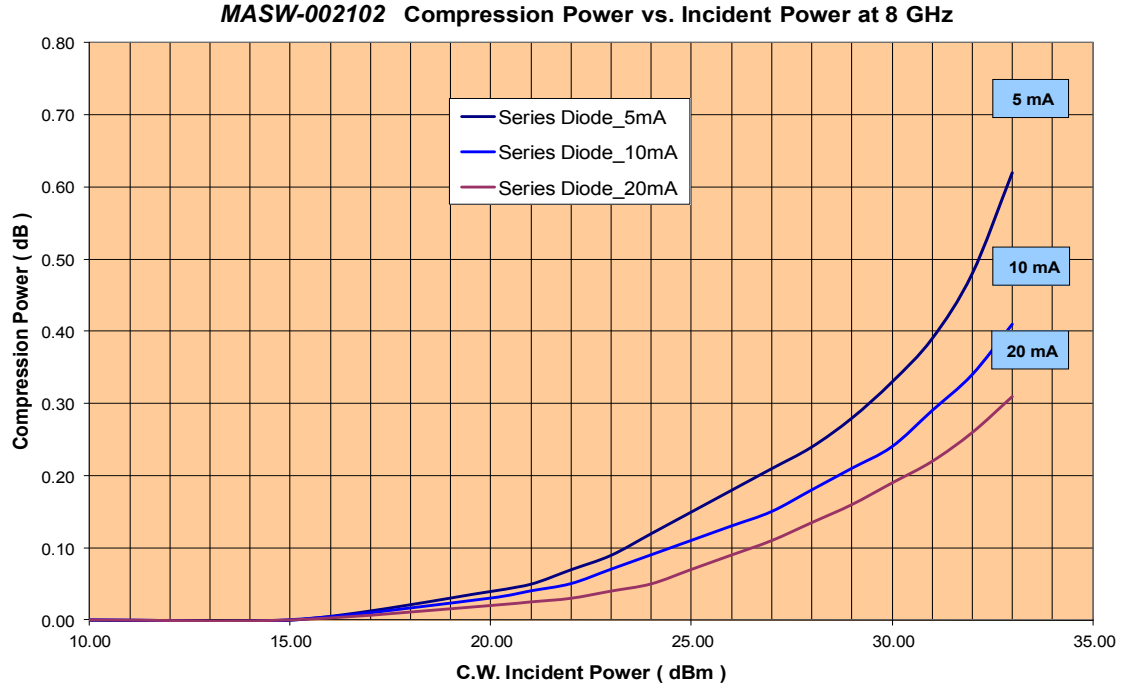
Insertion Loss



Return Loss







6. The MASW-003100 contains the same PIN diodes and will have similar performance.

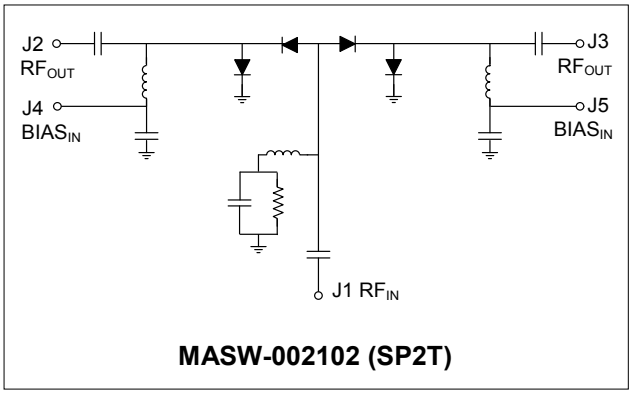
Operation of MASW-00x102 Series

Operation of the MASW-00x102 series PIN diode switches is achieved by simultaneous application of DC currents to the bias pads. The required levels for the different states are shown in the tables below. The control currents should be supplied by constant current sources. The nominal 40 - 60 Ω pull-up resistor voltage @ J4 and J5 is usually -1 V for -20 mA and +20 mA for +1 V.

Driver / Bias Connections

MASW-002102 (SP2T)

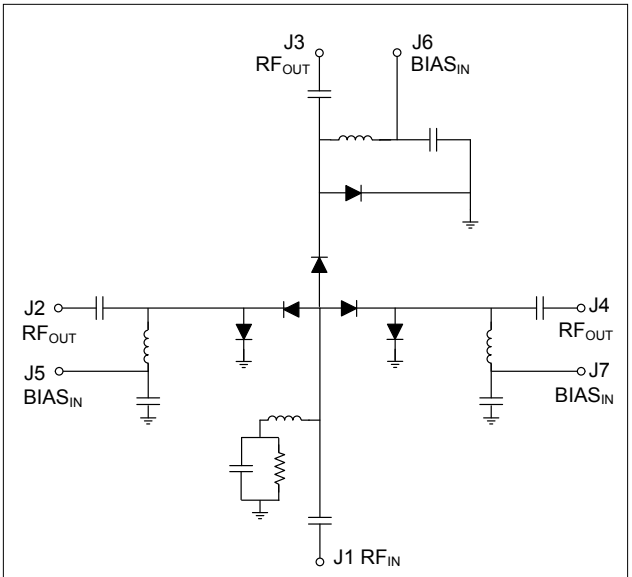
DC Control Current (mA)		RF Output States	
J4	**J5**	**J1-J2**	**J1-J3**
-20	+20	low loss	Isolation
+20	-20	Isolation	low loss



MASW-002102 (SP2T)

MASW-003102 (SP3T)

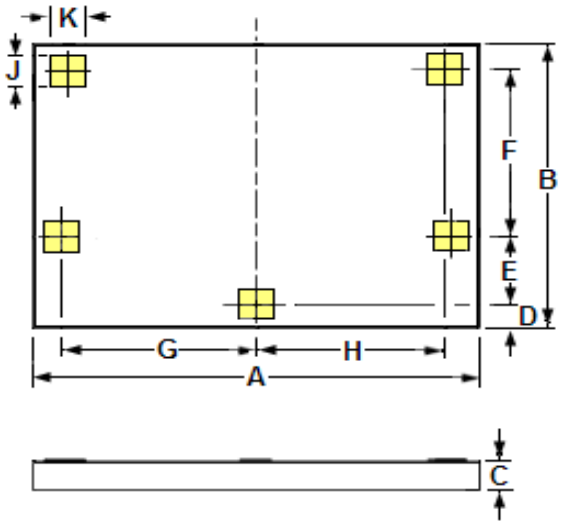
DC Control Current (mA)			RF Output States		
J5	**J6**	**J7**	**J1-J2**	**J1-J3**	**J1-J4**
-20	+20	+20	low loss	Isolation	Isolation
+20	-20	+20	Isolation	low loss	Isolation
+20	+20	-20	Isolation	Isolation	low loss



MASW-003102 (SP3T)

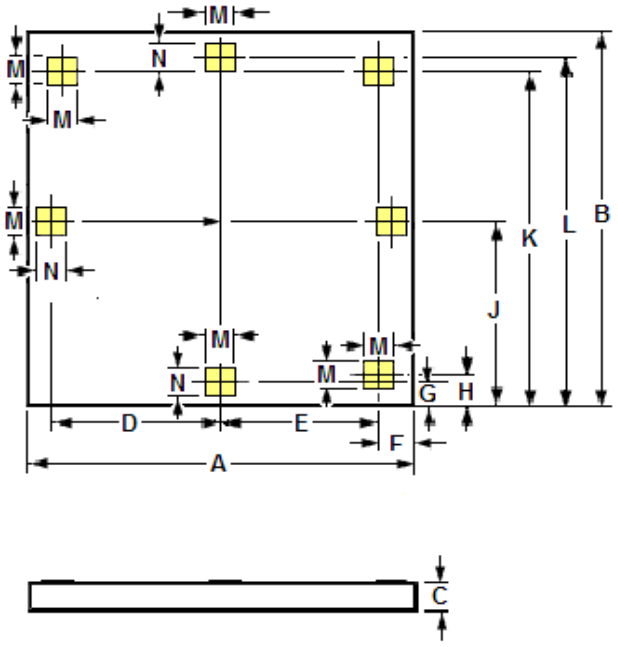
Chip Outline Drawings[7,8]

MASW-002102 (SP2T)



DIM	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.066	0.070	1.680	1.780
B	0.048	0.052	1.230	1.330
C	0.004	0.006	0.100	0.150
D	0.004	0.006	0.090	0.140
E	0.012	0.013	0.292	0.317
F	0.029	0.030	0.735	0.760
G	0.030	0.031	0.766	0.791
H	0.029	0.030	0.732	0.757
J	0.005	REF.	0.129	REF.
K	0.005	REF.	0.129	REF.

MASW-003102 (SP3T



DIM	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.071	0.072	1.807	1.833
B	0.071	0.072	1.797	1.823
C	0.0045	0.0055	0.100	0.150
D	0.031	0.032	0.781	0.807
E	0.029	0.030	0.732	0.758
F	0.006	0.007	0.152	0.178
G	0.004	0.005	0.099	0.125
H	0.005	0.006	0.125	0.151
J	0.034	0.035	0.871	0.897
K	0.064	0.065	1.617	1.643
L	0.066	0.067	1.683	1.709
M	0.005	REF.	0.1250	REF.
N	0.0046	REF.	0.1180	REF.

7. Topside and backside metallization is gold, 2.5 µm thick typical.
8. Yellow areas indicate ribbon/wire bonding pads