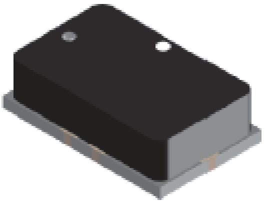
MSW203x-203

SP2T Limiter PIN Diode Switch

Rev. V1

Features

- Wide Frequency Range: 50 MHz to 6 GHz, in 3 bands
- Surface Mount SP2T Switch in Compact Outline:
  - 8 mm L x 5 mm W x 2.5 mm H
- Higher Average Power Handling than Plastic Packaged
  - MMIC Switches: 100 W CW
- High RF Peak Power: 500 W
- Low Insertion Loss: 0.25 dB
- High IIP3: 65 dBm
- Operates From Positive Voltage Only: 5 V & 28 V to 125 V
- RoHS Compliant


Case Style CS203

Applications

- High Power Transmit/Receive (TR) Switching
- Active Receiver Protection

Description

The MSW2030-203, MSW2031-203, and MSW2032-203 series of surface mount silicon PIN diode SP2T switches comprises three switches which can be used for high power transmit/receive (TR) switching or active receiver protection from 50 MHz to 1 GHz, 400 MHz to 4 GHz and 2 to 6 GHz respectively. These switches are manufactured using Aeroflex/Metelics proven hybrid manufacturing process incorporating high voltage PIN diodes and passive devices integrated on a ceramic substrate. These low profile, compact, surface mount components (8 mm L x 5 mm W x 2.5 mm H) offer superior small and large signal performance compared to that of MMIC devices in QFN packages. The SP2T switches are designed in a symmetrical topology to enable either switched RF port to be used as the high-input-power-handling port, to minimize insertion loss and to maximize isolation performance. The very low thermal resistance (< 25 ºC/W) of the PIN diodes in these devices enables them to reliably handle RF incident power levels of 50 dBm CW and RF peak incident power levels of 57 dBm in cold switching applications at T_A = 85 ºC. The thick I layers of the PIN diodes (> 100 µm), coupled with their long minority carrier lifetime (> 2 µs), produces input third order intercept point (IIP3) greater than 65 dBm.

These MSW2030-203, MSW2031-203, and MSW2032-203 series SP2T switches are designed to be used in high average and peak power switch applications, operating from 50 MHz to 6 GHz in three bands, which utilize high volume, surface mount, solder re-flow manufacturing. These products are durable and capable of reliably operating in military, commercial, and industrial environments. The devices are RoHS compliant.

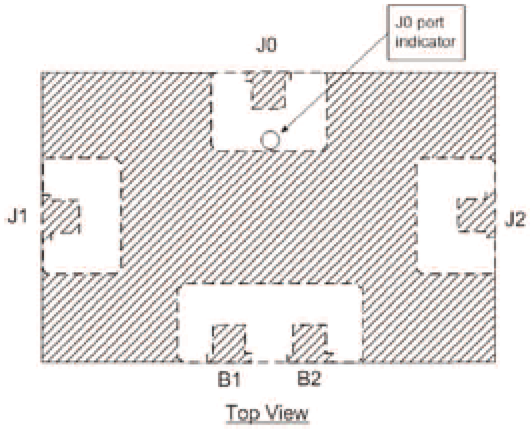
Environmental Capabilities

The MSW2030-203, MSW2031-203, and MSW2032-203 series SP2T switches are capable of meeting the environmental requirements of MIL-STD-202 and MIL-STD-750.

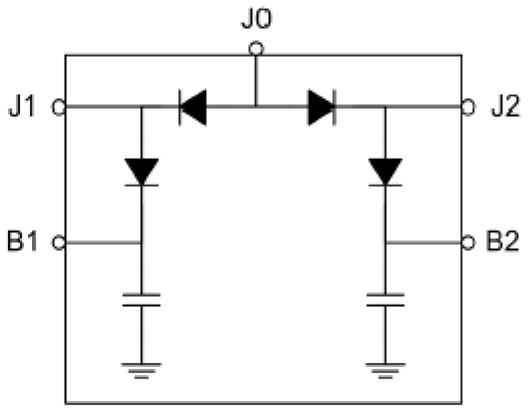
ESD and Moisture Sensitivity Level Rating

PIN Diode Switches are susceptible to ESD conditions as with all semiconductors. The ESD rating for this device is Class 0, HBM. The moisture sensitivity level rating is MSL 1.

Pin Out



Schematic



Truth Table for Control of Symmetrical SP2T Switch

MSW203x-203 Series

+V_{CC1} = 5 V and +V_{CC2} = 28 V (Unless otherwise noted)

Port J0 – J1	Port J0 – J2	Bias:J1 (Notes 1,2)	Bias:J2 (Notes 1,2)	B1 (Notes 1,2)	B2 (Notes 1,2)
Low Loss	Isolation	V = 0 V, I = -100 mA	V = V_{HIGH} I = 25 mA	V = V_{HIGH} I = 0 mA	V = 0 V, I = -25 mA
Isolation	Low Loss	V = V_{HIGH} I = 25 mA	V = 0 V, I = -100 mA	V = 0 V, I = -25 mA	V = V_{HIGH} I = 0 mA

Notes:

1 28 V ≤ V_{HIGH} ≤ 125 V.

2 PIN diode minimum reverse DC voltage (V_{HIGH}) to maintain high resistance in the OFF PIN diode is determined by RF frequency, incident power, duty cycle, characteristic impedance and VSWR as well as by the characteristics of the diode. The recommended minimum reverse bias voltage (V_{HIGH}) values are provided in the Minimum Reverse Bias Voltage table of this datasheet.

MSW2030-203Electrical Specifications

Z_0 = 50 Ω, T_A= 25 ºC (Unless Otherwise Defined)

Parameter	Symbol	Test Conditions	Min. Value	Typ. Value	Max. Value	Units
Frequency	F		50	-	1000	MHz
Insertion Loss	IL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2	-	0.3	0.4	dB
Return Loss	RL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2	20	22	-	dB
Isolation	Isol	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2	50	52	-	dB
CW Incident Power (Note 2)	P_{inc}(CW)	source & load VSWR = 1.5:1	-	50	51	dBm
Peak Incident Power (Note 2)	P_{Inc}(Pk)	source & load VSWR = 1.5:1, pulse width = 10 µs, duty cycle = 1%	-	57	-	dBm
Switching Time (Note 1)	t_{sw}	10% -90% RF voltage, TTL rep rate = 100	-	2	3	µs
Input 3rd Order Intercept Point	IIP3	F_1 = 500 MHz, F_2 = 510 MHz, P_1 = P_2 = 10 dBm, measured on path biased to low loss state	60	65	-	dBm

MSW2031-203 Electrical Specifications

Z_0 = 50 Ω, T_A= 25 ºC (Unless Otherwise Defined)

Parameter	Symbol	Test Conditions	Min. Value	Typ. Value	Max. Value	Units
Frequency	F		400	-	4000	MHz
Insertion Loss	IL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2	-	0.5	0.6	dB
Return Loss	RL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2	14	16	-	dB
Isolation	Isol	Bias state 1: port J0 to J2 Bias state 2: port J0 to J1	32	35	-	dB
CW Incident Power (Note 2)	P_{inc}(CW)	source & load VSWR = 1.5:1	-	50	51	dBm
Peak Incident Power (Note 2)	P_{Inc}(Pk)	source & load VSWR = 1.5:1, pulse width = 10 µs, duty cycle = 1%	-	57	-	dBm
Switching Time (Note 1)	t_{sw}	10% -90% RF voltage, TTL rep rate = 100	-	1	2	µs
Input 3rd Order Intercept Point	IIP3	F_1 = 1000 MHz, F_2 = 1010 MHz, P_1 = P_2 = 10 dBm, measured on path biased to low loss state	60	65	-	dBm

(continued next page)

MSW2032-203 Electrical Specifications

Z_0 = 50 Ω, T_A = 25 °C (Unless Otherwise Defined)

Parameter	Symbol	Test Conditions	Min. Value	Typ. Value	Max. Value	Units
Frequency	F		2	-	6	GHz
Insertion Loss	IL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2	-	0.6	0.8	dB
Return Loss	RL	Bias state 1: port J0 to J1 Bias state 2: port J0 to J2	11	13	-	dB
Isolation	Isol	Bias state 1: port J0 to J2 Bias state 2: port J0 to J1	32	35	-	dB
CW Incident Power (Note 2)	P_{inc}(CW)	source & load VSWR = 1.5:1	-	50	51	dBm
Peak Incident Power (Note 2)	P_{inc}(Pk)	source & load VSWR = 1.5:1, pulse width = 10 µs, duty cycle = 1%	-	57	-	dBm
Switching Time (Note 1)	t_{SW}	10% -90% RF voltage, TTL rep rate = 100	-	1	2	µs
Input 3rd Order Intercept Point	IIP3	F_1 = 2000 MHz, F_2 = 2010 MHz, P_1 = P_2 = 10 dBm, measured on path biased to low loss state	60	65	-	dBm

Conditions:

1 State 1 (J0 – J1 in low insertion loss state, J0 - J2 in isolation state):

a. B1: V_{HIGH} (note 2), 0 mA

b. B2: -25 mA, 0 V

c. J1: -100 mA, 0 V

d. J2: 25 mA, V_{HIGH} (note 2)

e. J0: 100 mA, ≈0.9 V

2 State 2 (J0 – J2 in low insertion loss state, J0 - J1 in isolation state):

a. B1: -25 mA, 0 V

b. B2: V_{HIGH} (note 2), 0 mA

c. J1: 25 mA, V_{HIGH} (note 2)

d. J2: -100 mA, 0 V

e. J0: 100 mA, ≈0.9 V

Notes:

1 Switching time (50% TTL – 10/90% RF Voltage) is a function of the PIN diode driver performance as well as the characteristics of the diode. An RC "current spiking network" is used on the driver output to provide a transient current to rapidly remove stored charge from the PIN diode. Typical component values are: R = 50 to 220 Ω and C = 470 to 1,000 pF. MACOM's MPD2T28125-700 is the recommended PIN diode driver to interface with the MSW2030-203, MSW2031-203, and MSW2032-203 SP2T switches. Its data sheet is available

2 PIN diode minimum reverse DC voltage (V_{HIGH}) to maintain high resistance in the OFF PIN diode is determined by RF frequency, incident power, duty cycle, characteristic impedance and VSWR as well as by the characteristics of the diode. The recommended minimum reverse bias voltage (V_{HIGH}) values are provided in the Minimum Reverse Bias Voltage table (page 5)of this datasheet.

RF Bias Network Component Values

P/N	F (MHz)	DC Blocking Capacitors	Inductors	RF Bypass Capacitors	Secondary Bypass
MSW2030-203	50 – 1,000	470 pF	Ferrite Bead 600 Ω, 1A	470 pF	470 pF
MSW2031-203	400 – 4,000	47 pF	43 nH	220 pF	1000 pF
MSW2032-203	2,000 - 6,000	22 pF	33 nH	33 pF	1000 pF

Minimum Reverse Bias Voltage at TX, RX, DC Ports vs. Signal Frequency

P_{INC} = 100 W CW, Z_0 = 50Ω with 1.5:1 VSWR

Part Number	F = 20 MHz	F = 100 MHz	F = 200 MHz	F = 400 MHz	F = 1 GHz	F = 4 GHz
MSW2030-203	120 V	110 V	85 V	55 V	28 V	NA
MSW2031-203	NA	NA	110 V	85 V	55 V	28 V
MSW2032-203	(F = 1 GHz) 55 V	(F = 2 GHz) 28 V	(F = 3 GHz) 28 V	(F = 4 GHz) 28 V	(F = 5 GHz) 28 V	(F = 6 GHz) 28 V

Note: "NA" denotes the switch is not recommended for use in that frequency band.

Absolute Maximum Ratings

Z_0 = 50 Ω, T_A= +25 ºC (Unless Otherwise Defined)

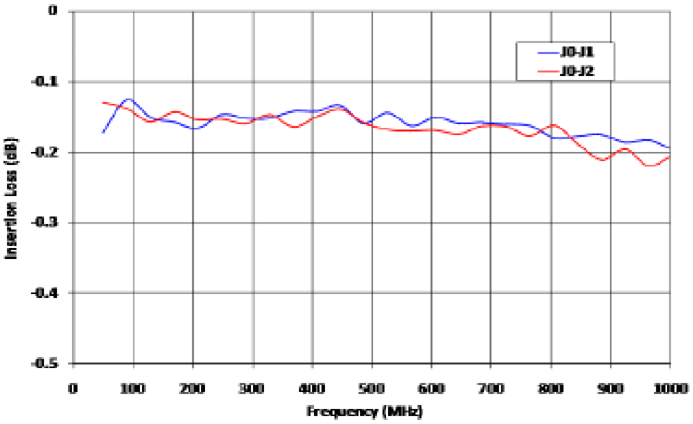
Parameter	Conditions	Absolute Maximum Value
Forward Current - J0, J1, J2 Port		250 mA
Forward Current - B1 and B2 Port		150 mA
Reverse Voltage - J0, J1, J2, B1, B2 Port		125 V
Forward Diode Voltage	I_F = 250 mA	1.2 V
Operating Temperature		-65 ºC to 125 ºC
Storage Temperature		-65 ºC to 150 ºC
Junction Temperature		175 ºC
Assembly Temperature	t = 10 s	260 ºC for 10 s
CW Incident Power Handling – J0, J1, J2 Port (Note 1)	Source & load VSWR = 1.5 :1, T_{CASE} = 85 ºC, cold switching	50 dBm
Peak Incident Power Handling – J0, J1, J2 Port (Note 1)	Source & load VSWR = 1.5 :1, T_{CASE} = 85 ºC, cold switching, pulse width = 10 µs, duty cycle = 1%	57 dBm
Total Dissipated RF & DC Power (Note 1)	T_{CASE} = 85 ºC, cold switching	8 W

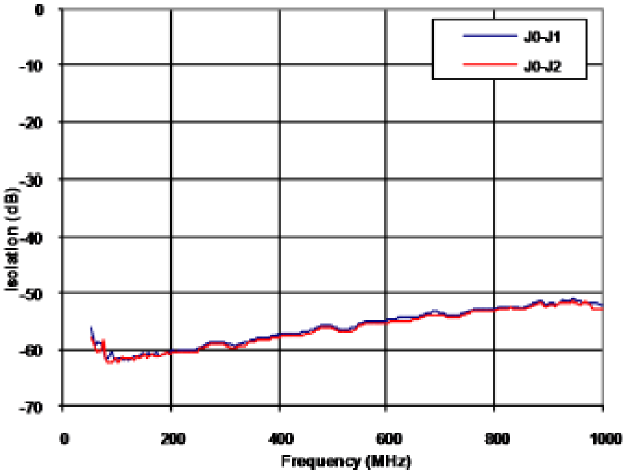
Notes:

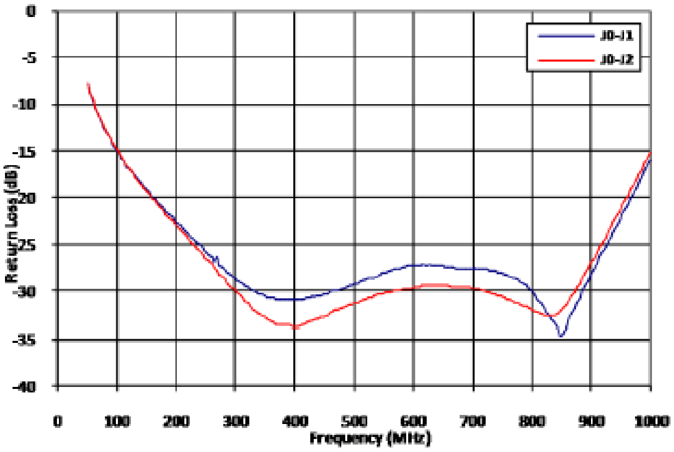
1 Backside RF and DC grounding area of device must be completely solder-attached to RF circuit board vias for proper electrical and thermal circuit grounding.

MSW2030-203 Small Signal Typical Performance

Z_0 = 50 Ω, T_A = +25 ºC (Unless Otherwise Defined)

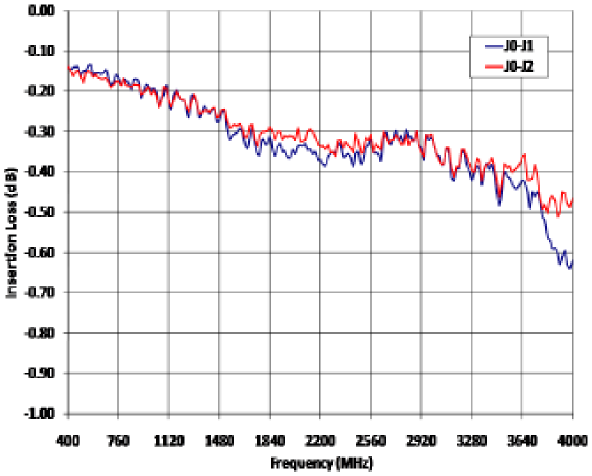


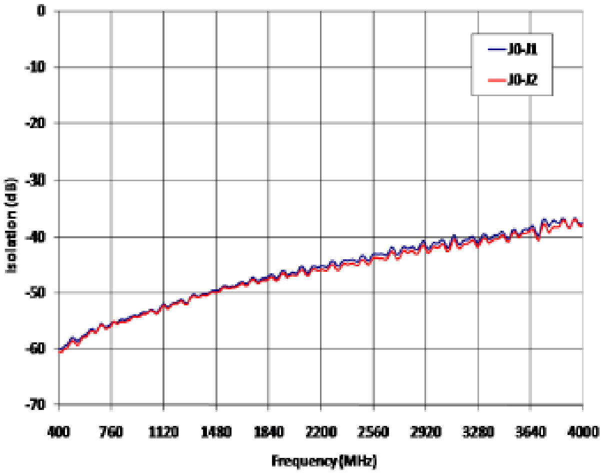


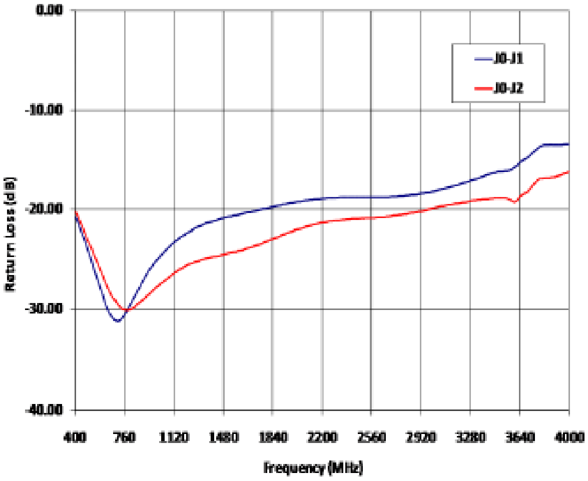


MSW2031-203 Small Signal Typical Performance

Z_0 = 50 Ω, T_A = +25 ºC (Unless Otherwise Defined)







MSW2032-203 Small Signal Typical Performance

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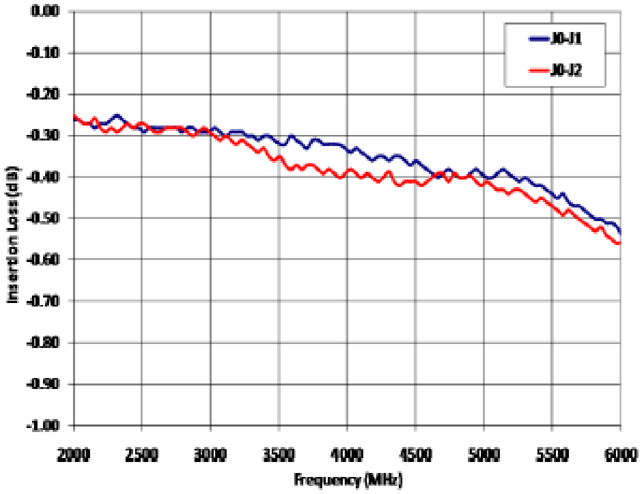
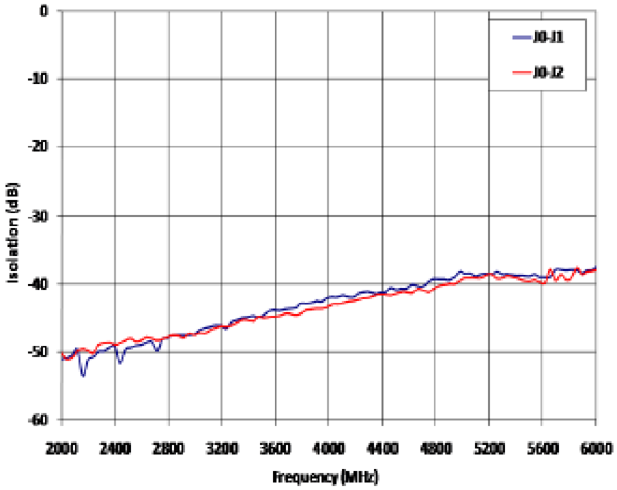
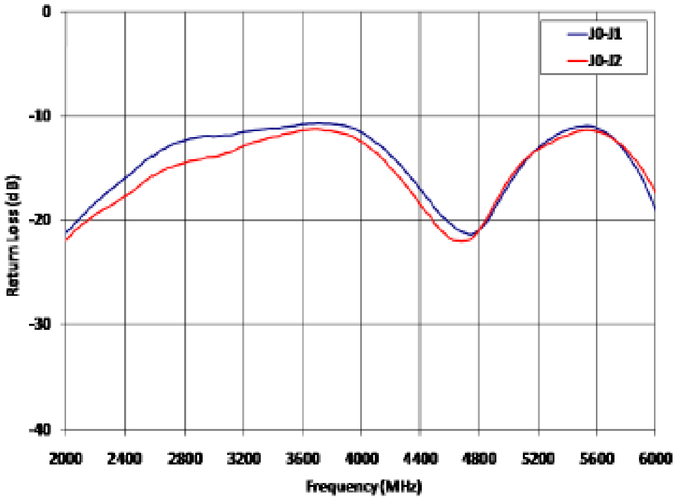
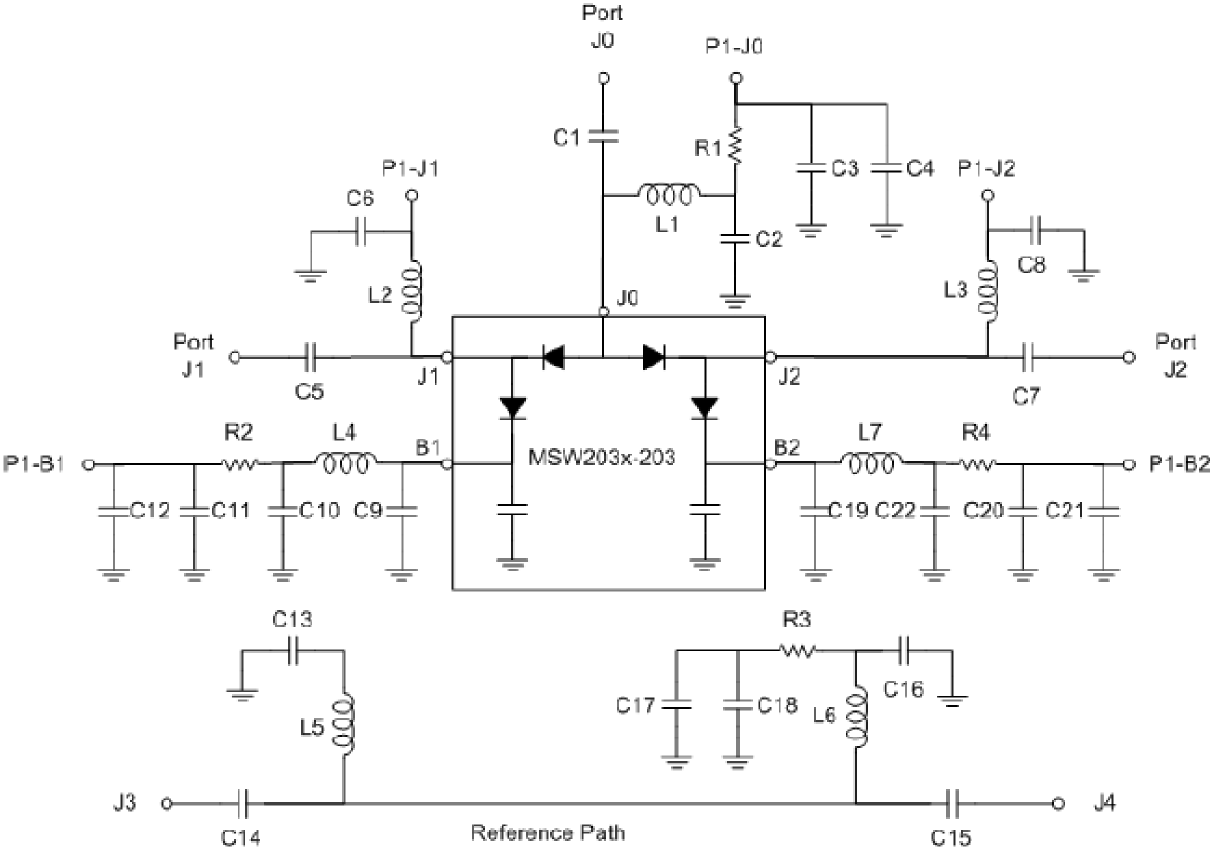






SP2T Switch Evaluation Board Schematic



Evaluation Board Description

The evaluation boards for the MSW2030 family of surface mount silicon PIN diode SP2T T-R switches allow the full exercise of each switch for small signal performance analysis, as well as for large signal operation with maximum input signal power of 45 dBm (CW or peak power). Each evaluation board includes the appropriate MSW203x-203 switch, DC blocking capacitors at each RF port and bias decoupling networks at each RF port which allow DC or low frequency control signals to be applied to the switch.

Four complementary control signals are required for proper operation. Bias voltages are applied to the B1 and B2 bias ports, as well as to the J0, J1 and J2 RF ports to control the state of the switch. A fixed bias voltage must be applied to the J0 port (connect 5 V to pin 3 of multi-pin connector P1) whenever the switch is in operation.

Caution: the evaluation board, as supplied from the factory, is not capable of handling RF input signals larger than 45 dBm. If performance of the switch under larger input signals is to be evaluated several of the passive components on the board must be changed in order to safely handle the dissipated power as well as the high bias voltage necessary for proper performance. The evaluation board must be connected to an adequate heat sink for large signal operation. Contact the factory for recommended components.

For the purposes of description, State 1 is defined to be the condition in which the evaluation board is biased to produce the low insertion condition between ports J0 and J1 while producing high isolation between ports J0 and J2. State 2 is the converse of State 1.

State 1

In State 1, the series PIN diode between the J0 and J1 ports is forward biased by applying 0 V to the J1 bias input port (pin 1 of multi-pin connector P1). The magnitude of the resultant bias current through the diode is primarily determined by the voltage applied to the J0 bias port (pin 3 of P1), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA. At the same time, the PIN diode connected between J2 and B2 ports is also forward biased by applying a high bias voltage, nominally 28 V, to the J2 bias port (pin 7 of P1) and 0 V to the B2 bias port (pin 5 of P1). Under this condition, the PIN diode connected between the J0 and J2 ports is reverse biased and the PIN diode connected between the J2 and B2 ports is forward biased. The magnitude of the bias current through this diode is primarily determined by the voltage applied to the J2 bias port, the magnitude of the forward voltage across the PIN diode and the resistance of R4. This current is nominally 25 mA.

The series PIN diode which is connected between the J0 and J2 ports must be reverse biased during State 1. The reverse bias voltage must be sufficiently large to maintain the diode in its non-conducting, high impedance state when large RF signal voltage may be present in the J0-to-J1 path. The reverse voltage across this diode is the arithmetic difference of the bias voltage applied to the J2 bias port and the DC forward voltage of the forward-biased J0-to-J1 series PIN diode.

The minimum voltage required to maintain the series diode between J0 and J2 out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the series diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors. Minimum control voltages for several signal frequencies are shown in the table "Minimum Reverse Bias Voltage", assuming the input power to the J0 or J1 port to be 100 W CW and the VSWR on the J0-J1 path to be 1.5:1.

State 2

In the State 2, the series PIN diode between the J0 and J2 ports is forward biased by applying 0 V to the J2 bias input port (pin 7 of multi-pin connector P1). The magnitude of the resultant bias current through the diode is primarily determined by the voltage applied to the J0 bias port (pin 3 of P1), the magnitude of the forward voltage across the PIN diode and the resistance of R1. This current is nominally 100 mA. At the same time, the PIN diode connected between J2 and B2 ports is reverse biased by applying a high bias voltage, nominally 28 V, to the B2 bias port (pin 5 of P1). A high voltage, nominally 28 V, is also applied to the J1 bias port (pin 1 of P1). Under this condition, the PIN diode connected between the J0 and J1 ports is reverse biased thus isolating the J1 RF port from the RF signal path between J0 and J2. The reverse voltage across this diode is the arithmetic difference of the bias voltage applied to the J1 bias port and the DC forward voltage of the forward-biased J0-to-J2 series PIN diode. The minimum voltage required to maintain the series diode on the J0-to-J1 side of the switch out of conduction is a function of the magnitude of the RF voltage present, the standing wave present at the diode's anode, the frequency of the RF signal and the characteristics of the series diode, among other factors.

The values of the reactive components which comprise the bias decoupling networks as well as the signal path DC blocking are shown in the table RF Bias Network Recommended Component Values.

Reference Path

A reference path is provided on the evaluation board, complete with bias decoupling networks, so that the magnitude of the insertion loss of the microstrip transmission lines connected to the switch and the associated bias decoupling components can be measured and removed from the measured performance of the switch.

Minimum Reverse Bias Voltage

The minimum reverse bias voltage required to maintain a PIN diode out of conduction in the presence of a large RF signal is given by:

$$|V_{DC}| = \frac{|V_{RF}|}{\sqrt{1+\left[\left(\frac{0.0142\times f_{MHz}\times W_{mils}^{2}}{V_{RF}\times\sqrt{D}}\right)\times\left(1+\sqrt{1+\left(\frac{0.056\times V_{RF}\times\sqrt{D}}{W_{mils}}\right)^{2}}\right)\right]^{2}}}$$

where

$|V_{DC}|$ = magnitude of the minimum DC reverse bias voltage

$|V_{RF}|$ = magnitude of the peak RF voltage (including the effects of VSWR)

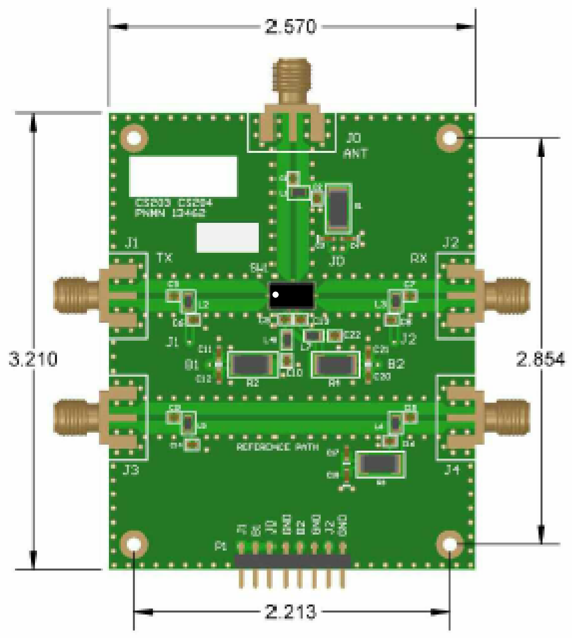
f_{MHz} = lowest RF signal frequency expressed in MHz

D = duty factor of the RF signal

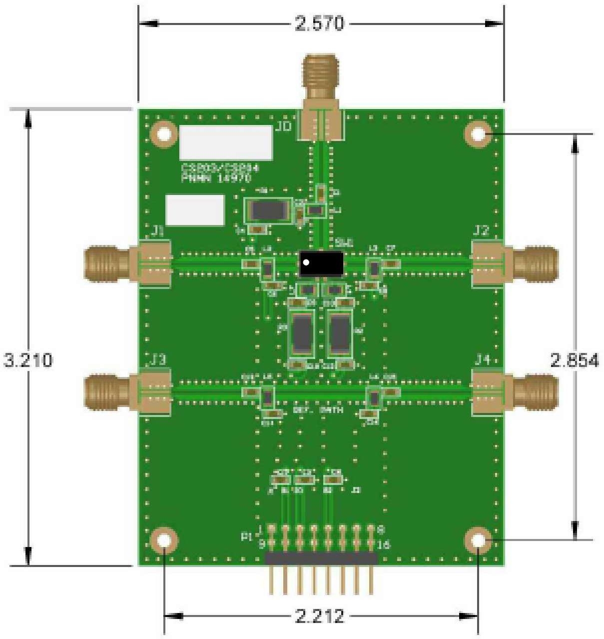
W_{mils} = thickness of the diode I layer, expressed in mils (thousandths of an inch)

(Caverly, R. H. & Hiller, G., "Establishing the Minimum Reverse Bias for a p-i-n Diode in a High-Power Switch", IEEE Transactions on Microwave Theory and Techniques, Vol. 38, No. 12, December 1990)

SP2T Switch Evaluation Board Layout



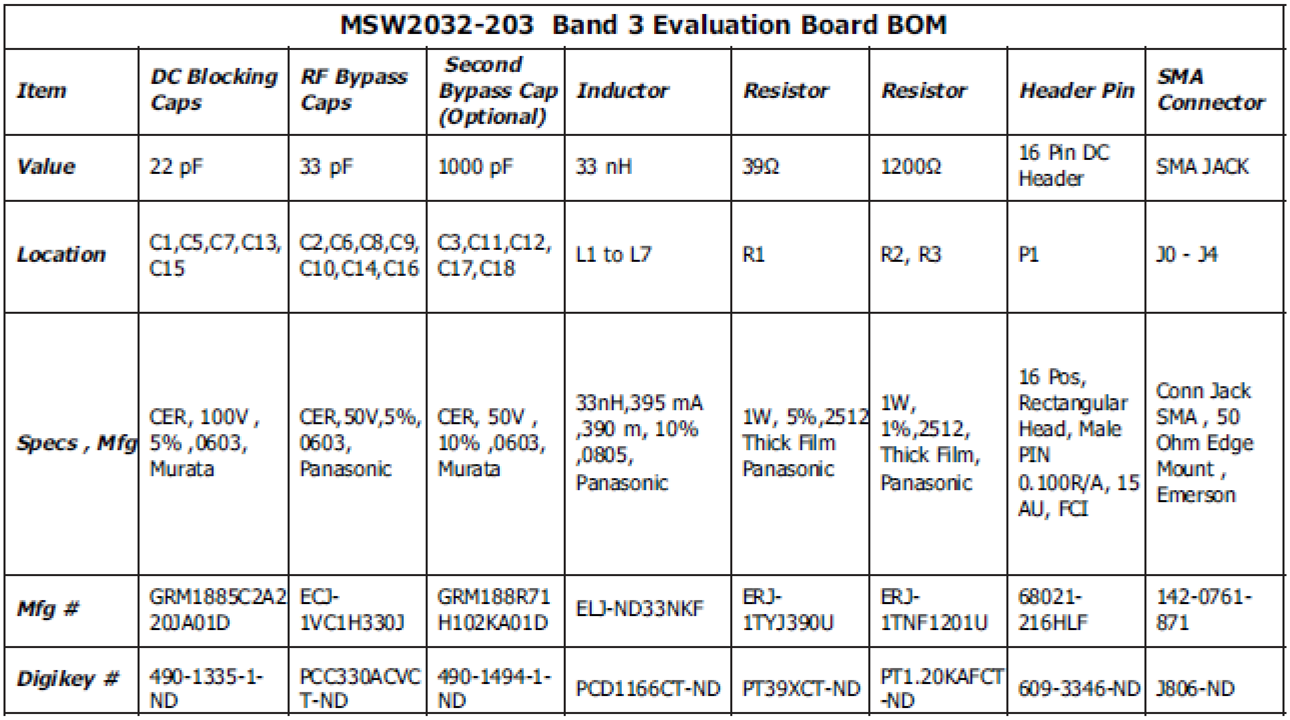
APPLIES TO THE FOLLOWING EVAL BOARDS:
CS203/CS204 - BAND 1/ BAND 2



APPLIES TO THE FOLLOWING EVAL BOARDS:
CS203/CS204 - BAND 3

MSW2030-203 Band 1 Evaluation Board BOM								
Item	***DC Blocking Caps***	***RF Bypass Caps***	***Second Bypass Cap (Optional)***	***Inductor***	***Resistor***	***Resistor***	***Header Pin***	***SMA Connector***
Value	470 pF	470 pF	470 pF	600 Ohm	39Ω	1200Ω	16 Pin DC Header	SMA JACK
Location	C1,C5,C7,C13, C15	C2,C6,C8, C9, C10, C14,C16,C19	C3,C4,C11, C12, C17, C18,C20,C21	L1 to L7	R1, R3	R2, R4	P1	J0 - J4
Specs , Mfg	CAP CER,470 pF,50 V , 5% ,NP0 ,0603, Johanson Dielectric Inc	CAP CER,470 pF,50 V , 5% ,NP0 ,0603, Johanson Dielectric Inc	CAP CER,470 pF,50 V , 5% ,NP0 ,0603, Johanson Dielectric Inc	Ferrite Bead, 600 Ohm, 1.0A, 0603, Wirth Electronics Inc	1W, 5%,2512 Thick Film Panasonic	1W, 1%,2512 , Thick Film, Panasonic	16 Pos, Rectangular Head , Male PIN 0.100R/A , 15 AU, FCI	Conn Jack SMA , 50 Ohm Edge Mount , Emerson
Mfg #	500R14N471JV4T	500R14N471JV4T	500R14N471JV4T	742792651	ERJ-1TYJ390U	ERJ-1TNF1201U	68016-208HLF	901-10309
Digikey #	709-1150-1-ND	709-1150-1-ND	709-1150-1-ND	732-1593-1-ND	PT39XTR-ND	PT1.20KAFTR-ND	609-3321-ND	ARF1744-ND

MSW2031-203 Band 2 Evaluation Board BOM								
Item	***DC Blocking Caps***	***RF Bypass Caps***	***Second Bypass Cap (Optional)***	***Inductor***	***Resistor***	***Resistor***	***Header Pin***	***SMA Connector***
Value	47 pF	220 pF	1000 pF	43 nH	39Ω	1200Ω	8 Pin DC Header	SMA JACK
Location	C1,C5,C7,C13, C15	C2,C6,C8,C9, C10, C14,C16, C19,C22	C3,C4,C11, C12,C17, C18,C20, C21	L1 to L7	R1, R3	R2, R4	P1	J0 - J4
Specs , Mfg	CAP CER,47 pF,50 V , 5% ,NP0 ,0603, Johanson Dielectric Inc	CAP CER,220 pF,50 V , 5% ,NP0 ,0603, Johanson Dielectric Inc	CAP CER,470 pF,50 V , 10% ,NP0 ,0603, X7R , Murata Electronics	RF Chip Inductor , 5%, 0603, Q min = 38, SRF min = 2 GHz, DCR Max (ohms)= 0.280, Irms(mA)= 600mA, CoilCraft.	1W, 5%,2512 Thick Film Panasonic	1W, 1%,2512 , Thick Film, Panasonic	8 Pos, Rectangular Head , Male PIN 0.100R/A , 15 AU, FCI	Conn Jack SMA , 50 Ohm Edge Mount , Amphenol –RF Division
Mfg #	500R14N4701JV4T	500R14N221JV4T	GRM188R71H102KA01D	0603CS-43NXJLU	ERJ-1TYJ390U	ERJ-1TNF1201U	68016-208HLF	ARF1744-ND
Digikey #	709-1145-1-ND	709-1148-1-ND	490-1494-1-ND	N/A	PT39XTR-ND	PT1.20KAFTR-ND	609-3321-ND	ARF1744-ND



MSW2032-203 Band 3 Evaluation Board BOM								
Item	***DC Blocking Caps***	***RF Bypass Caps***	***Second Bypass Cap (Optional)***	***Inductor***	***Resistor***	***Resistor***	***Header Pin***	***SMA Connector***
Value	22 pF	33 pF	1000 pF	33 nH	39Ω	1200Ω	16 Pin DC Header	SMA JACK
Location	C1,C5,C7,C13, C15	C2,C6,C8,C9, C10,C14,C16	C3,C11,C12, C17,C18	L1 to L7	R1	R2, R3	P1	J0 - J4
Specs , Mfg	CER, 100V , 5% ,0603, Murata	CER, 50V,5%, 0603, Panasonic	CER, 50V , 10% ,0603, Murata	33nH,395 mA ,390 m, 10% ,0805, Panasonic	1W, 5%,2512 Thick Film Panasonic	1W, 1%,2512, Thick Film, Panasonic	16 Pos, Rectangular Head, Male PIN 0.100R/A, 15 AU, FCI	Conn Jack SMA , 50 Ohm Edge Mount , Emerson
Mfg #	GRM1885C2A220JA01D	ECJ-1VC1H330J	GRM188R71H102KA01D	ELJ-ND33NKF	ERJ-1TYJ390U	ERJ-1TNF1201U	68021-216HLF	142-0761-871
Digikey #	490-1335-1-ND	PCC330ACVCT-ND	490-1494-1-ND	PCD1166CT-ND	PT39XCT-ND	PT1.20KAFCT-ND	609-3346-ND	J806-ND

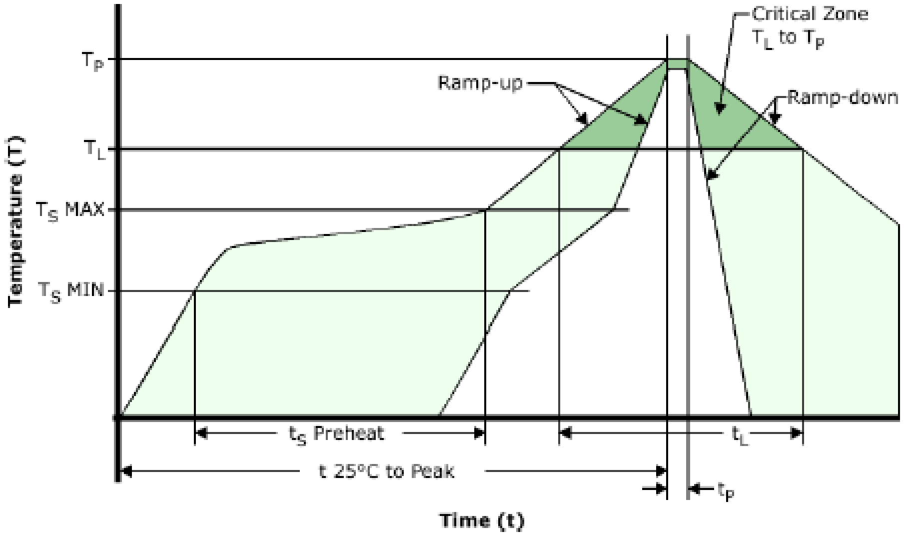
Assembly Instructions

SP2T PIN Diodes may be placed onto circuit boards with pick and place manufacturing equipment from tape-reel. The devices are attached to the circuit using conventional solder re-flow or wave soldering procedures with RoHS type or Sn 60 / Pb 40 type solders.

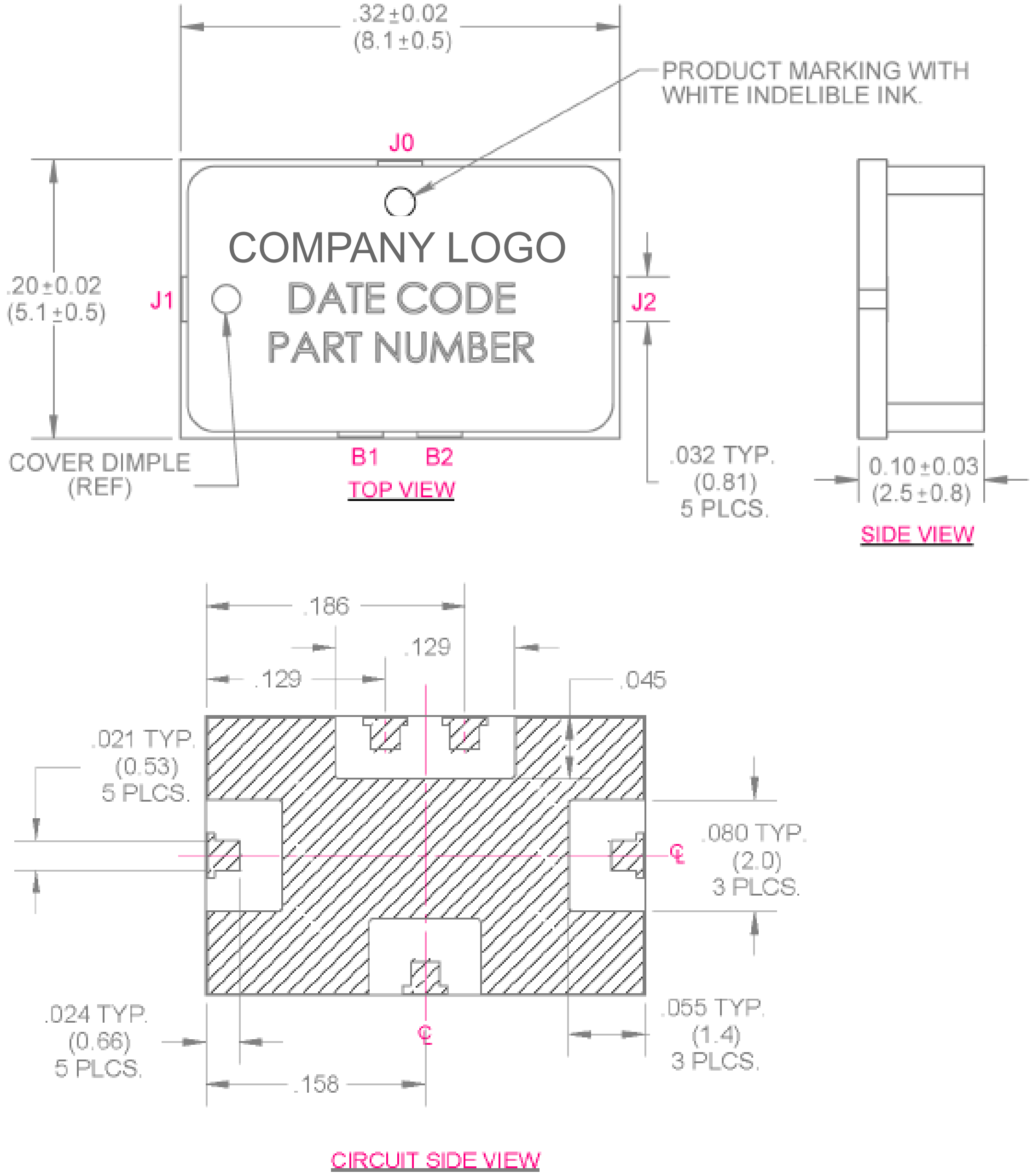
Table 1. Time-Temperature Profile for Sn60/Pb40 or RoHS Type Solders

Profile Feature	SnPb Solder Assembly	Pb-Free Solder Assembly
Average Ramp-Up Rate (T_L to T_P)	3 °C /second maximum	3 °C /second maximum
Preheat: - Temperature Min (T_{SMIN}) - Temperature Max (T_{SMAX}) - Time (min to max)(t_s)	100 °C 150 °C 60-120 s	150 °C 200 °C 60-180 s
T_{SMAX} to T_L - Ramp-Up Rate		3 °C/s maximum
Time Maintained Above: - Temperature (T_L) - Time (t_L)	183 °C 60-150 s	217 °C 60-150 s
Peak temperature (T_P)	225 +0/-5 °C	260 +0/-5 °C
Time Within 5 °C of Actual Peak Temperature (t_P)	10 – 30 s	20 – 40 s
Ramp-Down Rate	6 °C /s maximum	6 °C /s maximum
Time 25 °C to Peak Temperature	6 minutes maximum	8 minutes maximum

Figure 1. Solder Re-Flow Time-Temperature Profile



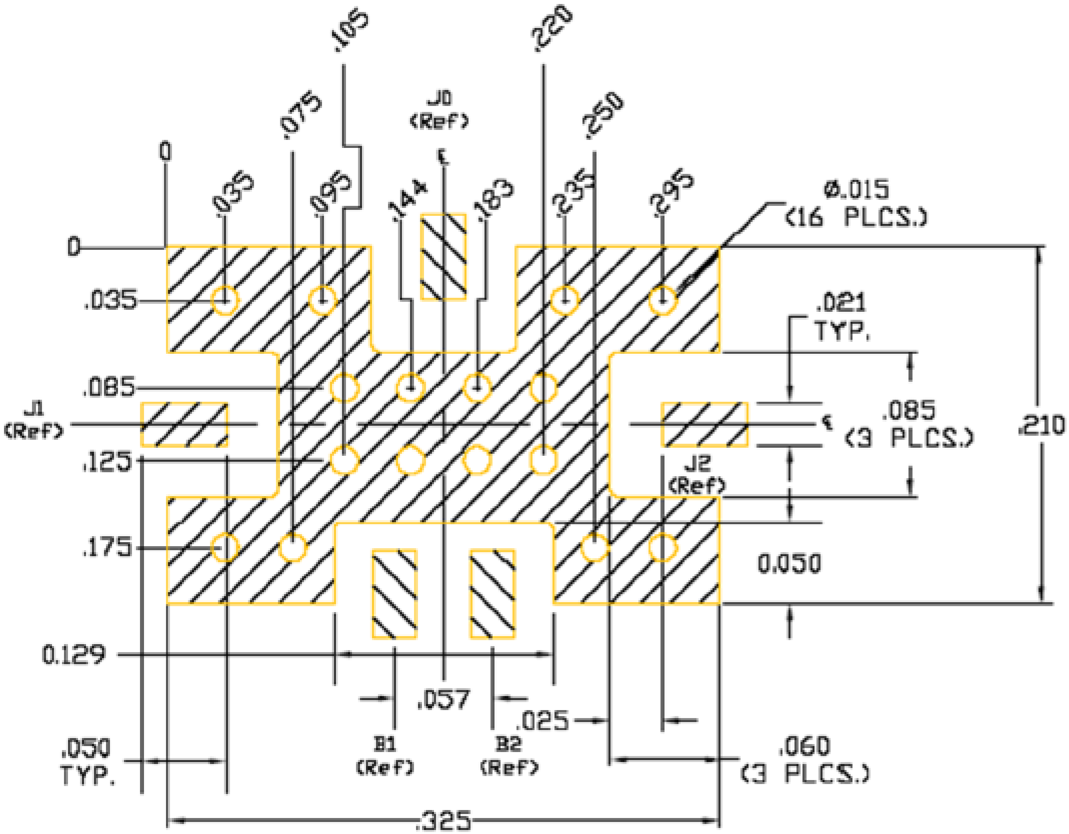
MSW2030-203, MSW2031-203, and MSW2032-203
SP2T Switch Outline (CS203)



Notes:

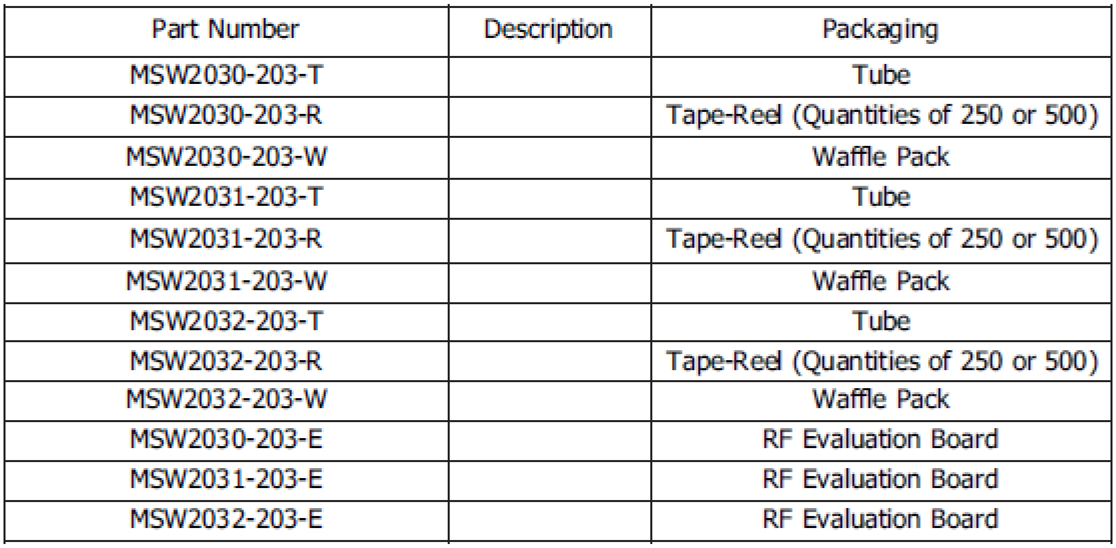
1. Hatched metal area on circuit side of device is RF, DC and thermal ground.

RF Circuit Solder Footprint for Case Style 203 (CS203)



Hatched area is RF, DC, and thermal Ground. Vias should be solid copper fill and gold plated for optimum heat transfer from backside of switch module through Circuit Vias to metal thermal ground.

Part Number Ordering Information



Part Number	Description	Packaging
MSW2030-203-T		Tube
MSW2030-203-R		Tape-Reel (Quantities of 250 or 500)
MSW2030-203-W		Waffle Pack
MSW2031-203-T		Tube
MSW2031-203-R		Tape-Reel (Quantities of 250 or 500)
MSW2031-203-W		Waffle Pack
MSW2032-203-T		Tube
MSW2032-203-R		Tape-Reel (Quantities of 250 or 500)
MSW2032-203-W		Waffle Pack
MSW2030-203-E		RF Evaluation Board
MSW2031-203-E		RF Evaluation Board
MSW2032-203-E		RF Evaluation Board

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