NVD4C05N

Product Preview

Power MOSFET

30 V, 4.1 mΩ, 90 A, Single N−Channel

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	T_C = 25°C	I_D	90	A
		T_C = 100°C		64	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	57	W
		T_C = 100°C		28	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25°C	I_D	22	A
		T_A = 100°C		16	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.5	W
		T_A = 100°C		1.7	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	270	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	75	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 5.6 A, L = 10 mH)			E_{AS}	157	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Note 1)	$R_{\theta JC}$	2.65	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	43	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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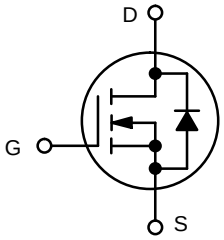
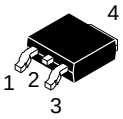
$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
30 V	4.1 mΩ @ 10 V	90 A
	6.0 mΩ @ 4.5 V	

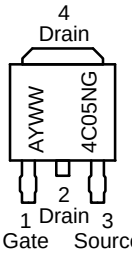


N−CHANNEL MOSFET



DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



A	= Assembly Location
Y	= Year
WW	= Work Week
4C05N	= Device Code
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				14.9		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.3		2.2	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4.7		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 45 A			3.4	4.1	mΩ
		V_{GS} = 4.5 V, I_D = 45 A			4.5	6.0	
CHARGES, CAPACITANCES AND GATE RESISTANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			1970		pF
Output Capacitance	C_{oss}				725		
Reverse Transfer Capacitance	C_{rss}				30		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 24 V, I_D = 45 A			31		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 24 V, I_D = 45 A			14		nC
Threshold Gate Charge	$Q_{G(TH)}$				3.3		
Gate−to−Source Charge	Q_{GS}				6.2		
Gate−to−Drain Charge	Q_{GD}				3.2		
Plateau Voltage	V_{GP}				3.1		V
Gate Resistance	R_G				1.0		Ω
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 24 V, I_D = 45 A, R_G = 0 Ω			11		ns
Rise Time	t_r				107		
Turn−Off Delay Time	$t_{d(off)}$				17		
Fall Time	t_f				6.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 45 A	T_J = 25°C		0.9	1.2	V
			T_J = 125°C		0.8		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 45 A			41		ns
Charge Time	ta				21		
Discharge Time	tb				20		
Reverse Recovery Charge	Q_{RR}				26		nC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

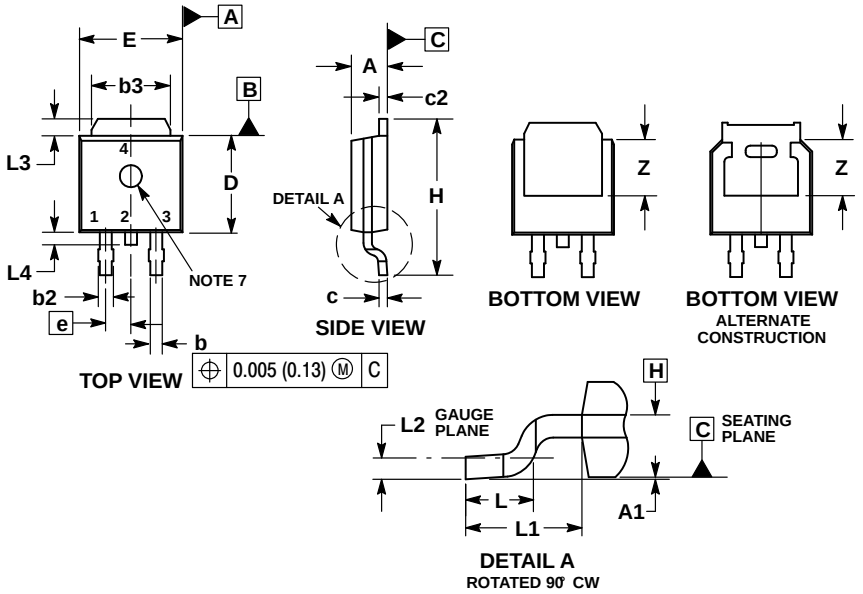
ORDERING INFORMATION

Order Number	Package	Shipping†
NVD4C05NT4G	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE E

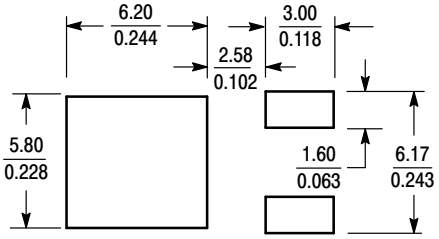


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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