GRF4003

Preliminary

Broadband LNA/Linear Driver 100 MHz to 3800 MHz

Package: 6-Pin DFN

Features

- Broadband: 100 MHz to 3800 MHz
- 0.72 dB Noise Figure at 2600 MHz
- 13.5 dB Gain at 2600 MHz
- Exceptional Low Voltage Linearity
- +40.5 dBm OIP3 at 3.3 V; 2600 MHz
- +21.8 dBm OP1dB at 3.3 V; 2600 MHz
- Flexible Drain Voltage: 1.8 V to 4.0 V
- Adjustable Bias Current
- RF Ports Internally Matched to 50 Ω

Applications

- First Stage LNA
- Linear Driver Amp for High PAR waveforms such as LTE and WCDMA
- Small Cells and Cellular Repeaters
- Microwave Backhaul
- Fast Switching TDD Systems
- Low Voltage Radio

Product Description

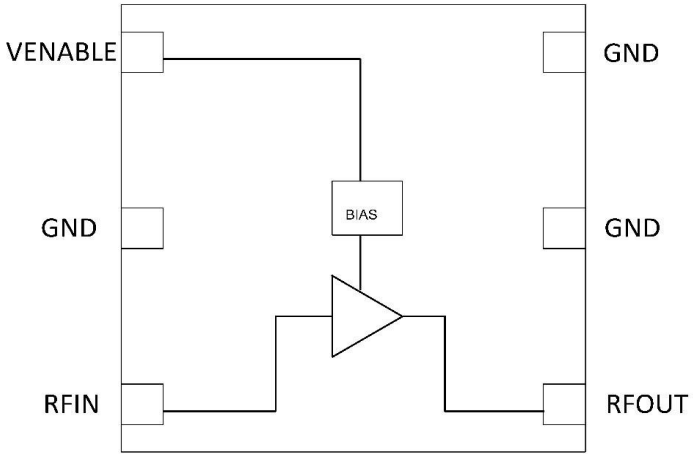
The GRF4003 is a broadband low noise gain block designed for small cell, wireless infrastructure and other high performance RF applications. It exhibits outstanding broadband NF, linearity and return losses over 100 to 3800 MHz with a single match.

Configured as a first stage LNA, linear driver or cascaded gain block, GRF4003 offers high levels of reuse both within a design and across platforms. The device is operated from a drain voltage (Vd) of 1.8 V to 4.0 V with a selectable Iddq range of 30 to 100 mA for optimal efficiency and linearity. Supply voltages (Vdd) higher than 4.0 V should use a small series resistor (M4) to lower the Vd to <= 4.0 volts under quiescent conditions.

GRF4003 is housed in a 1.5 mm x 1.5 mm x 0.5 mm 6-pin plastic DFN package and is internally matched to 50 Ω at the input and output ports, needing only external DC blocks and a bias choke on the output.

Functional Block Diagram

1.5mm X 1.5mm 6-Pin DFN Package



Absolute Ratings

Parameter	Symbol	Min.	Max.	Unit
Drain Voltage	V_D	0	5.0	V
RF Input Power: (Load VSWR < 2:1; V_D: 4.0 volts)	$P_{IN\ MAX}$		+18	dBm
Operating Temperature (Package Heat Sink)	T_{AMB}	-40	+105	°C
Storage Temperature	T_{STG}	-40	+150	°C
Maximum Channel Temperature (MTTF > 10^6 Hours)	Tmax		+160	°C
Maximum Quiescent Current	$I_{DDQ\ MAX}$		150	mA
Maximum Disspated Power (Note: De-rate 10 mW/°C for T_{AMB} > +85C.	$P_{DISS\ MAX}$		600	mW
Electrostatic Discharge:				
Charged Device Model: (TBD)	CDM	Class 4: 1000		V
Human Body Model: (TBD)	HBM	Class 1B: 500		V
Machine Model: (TBD)	MM	Class A: 50		V

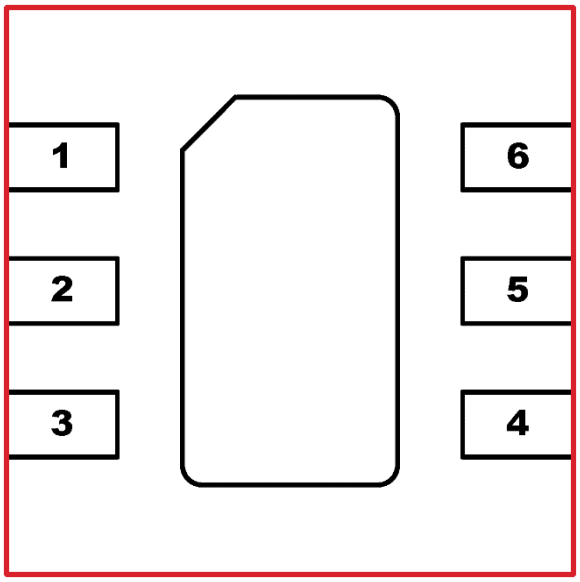
Caution! ESD Sensitive Device

Exceeding Absolute Maximum Rating conditions may cause permanent damage to the device.

Nominal Operating Parameters

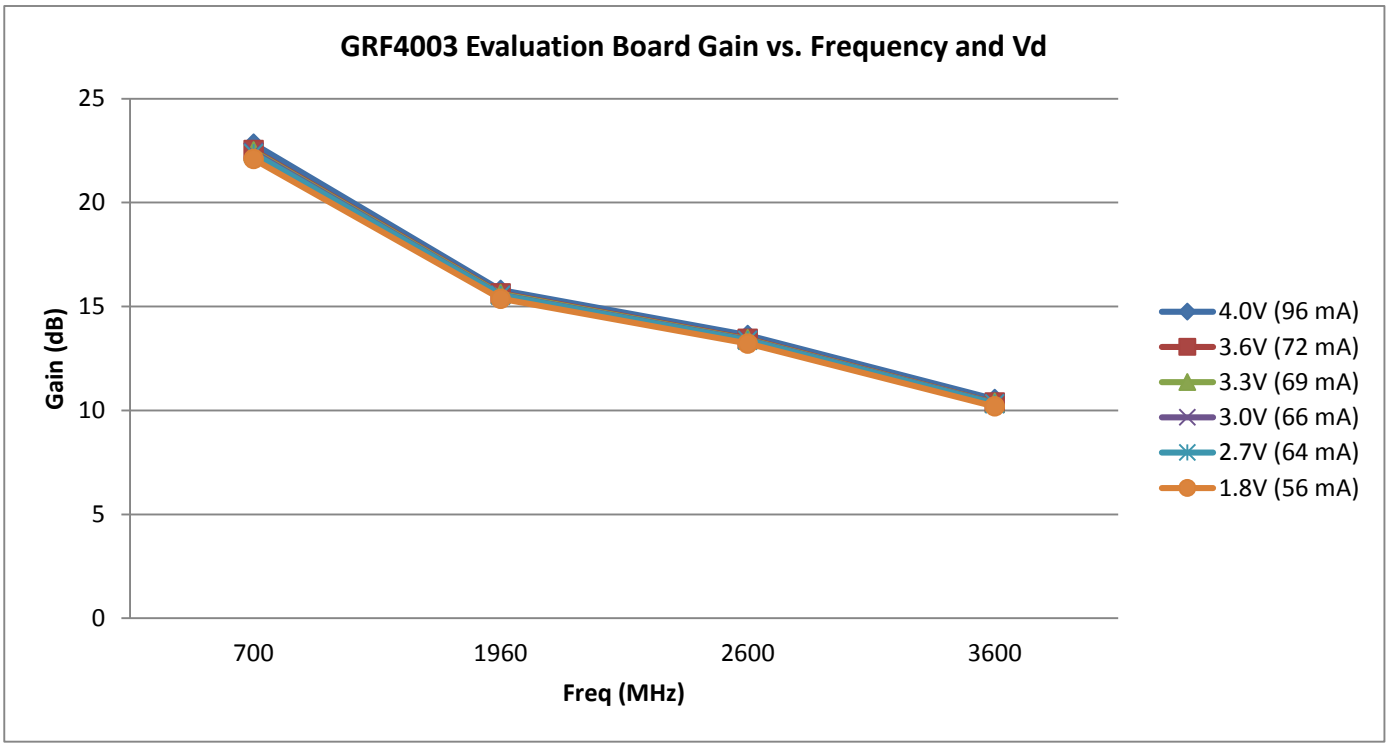
Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Gain Mode (Venable high)						Vd = 3.3 V, T_A = 25°C
Test Frequency	F_{TEST}		2600		MHz	
Gain	S21		13.5		dB	
Input Return Loss	S11		-12		dB	
Output Return Loss	S22		-17		dB	
Noise Figure	NF		0.72		dB	Input trace losses de-embedded
Output 3rd Order Intercept	OIP3		+40.5		dBm	+2 dBm P_{OUT} per tone at 2 MHz Spacing (2599 and 2601 MHz)
Output 1dB Compression Power	OP1dB		+21.8		dBm	
Switching Rise Time	T_{RISE}		300		ns	
Switching Fall Time	T_{FALL}		300		ns	
Supply Current	Idd		70		mA	Adjustable for optimal IP3
Enable Current	Ienable		2		mA	
Thermal Data						
Thermal Resistance (measured via IR scan)	Θjc		118		°C/W	On standard evaluation board
Channel Temperature @ +85 C Reference (Package Heat Sink)	Tchannel		+112		°C	Vd: 3.3 V; Iddq: 70 mA; No RF; Pdiss: 198 mW

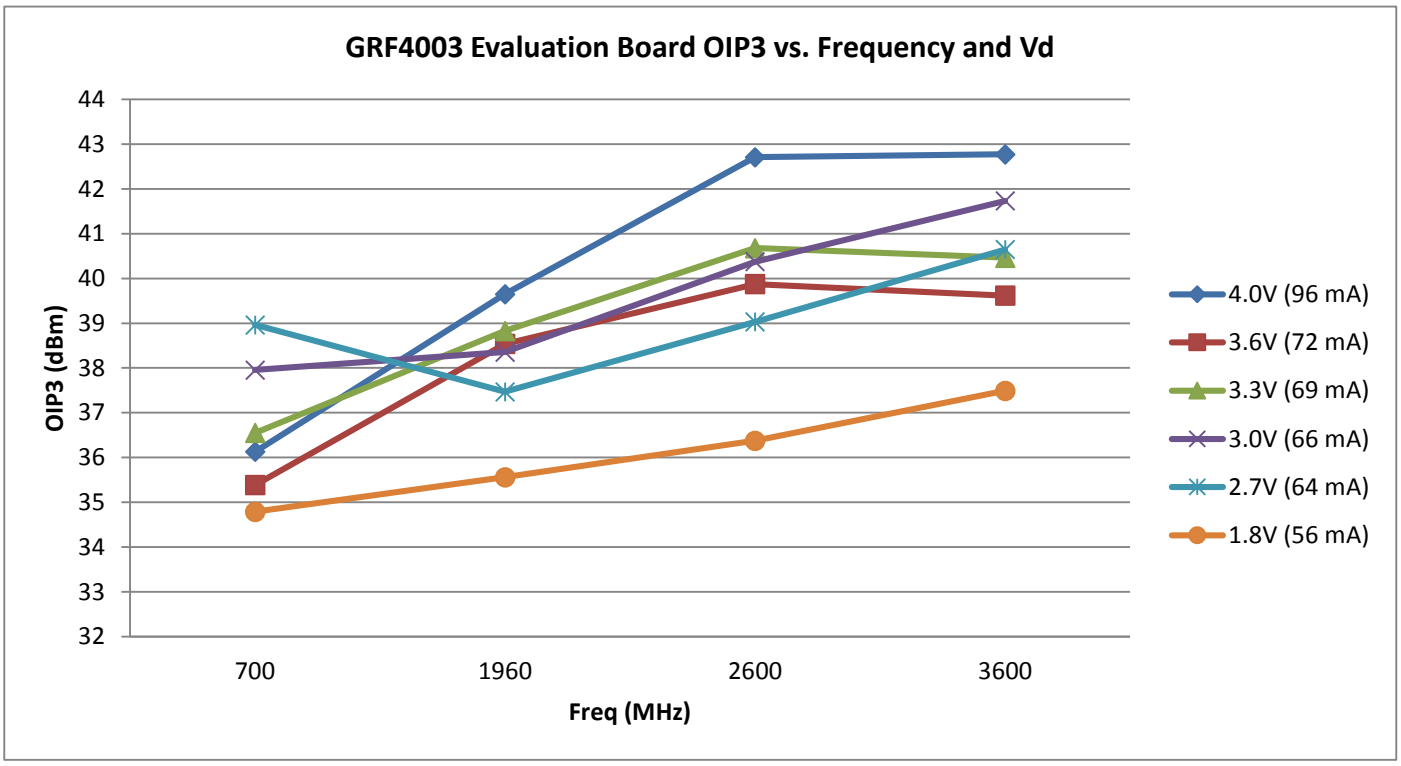
Pin Out

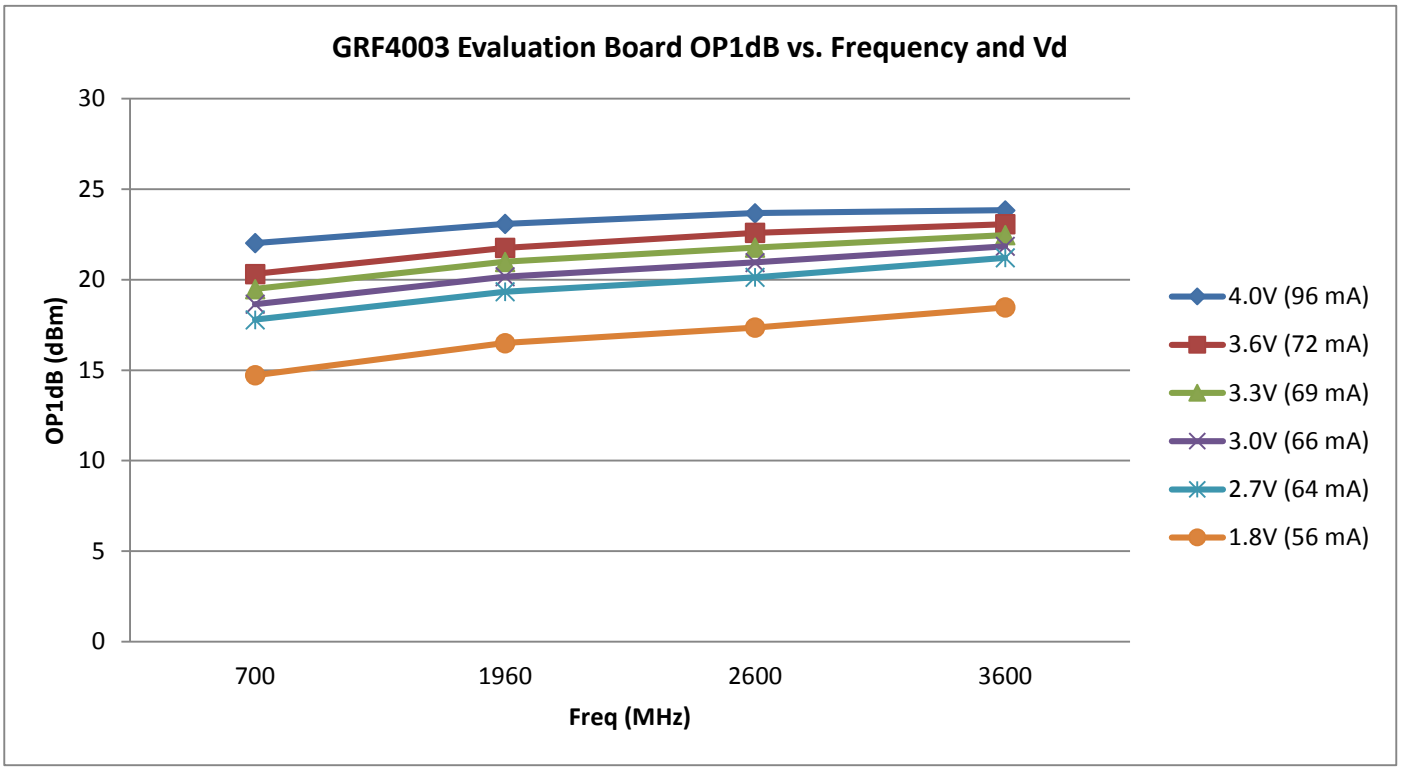


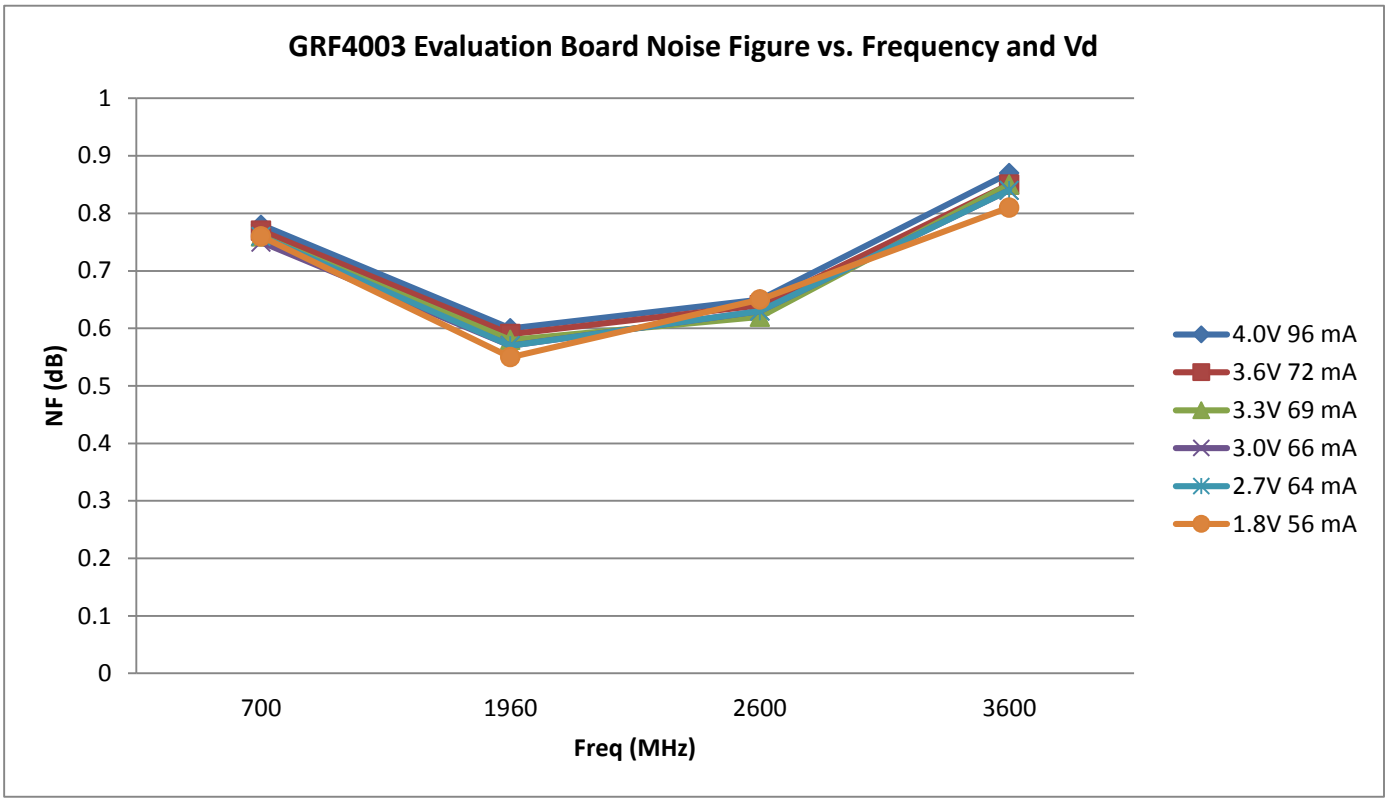
Pin Chart

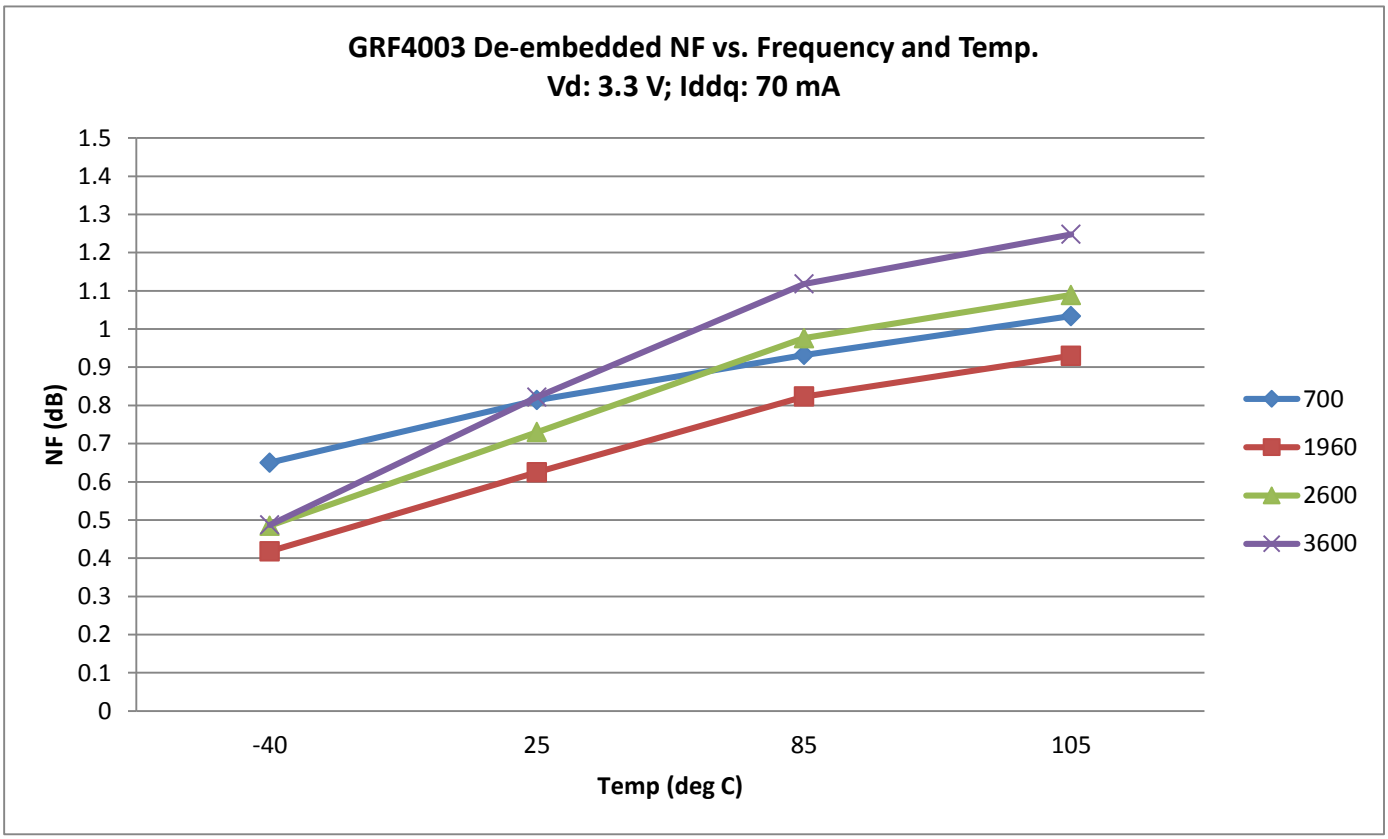
Pin	Name	Description	Note
1	V_{ENABLE}	LNA RF input	Ienable is approximately 5% of Iddq. Venable < 0.2 volts turns the device off. Venable and series resistor M3 control the device Iddq.
2	GND	Ground	Connect to ground for maximum RF performance.
3	RF_{IN}	LNA RF input	Internally matched 50 Ω.
4	RF_{OUT}	LNA RF output	Internally matched 50 Ω. V_{DD} must be applied through a choke to this pin.
5	GND	Ground	Connect to ground for maximum RF performance.
6	GND	Ground	Connect to ground for maximum RF performance.
PKG BASE	GND	Ground	Provides DC and RF ground for LNA, as well as thermal heat sink. Use multiple ground vias beneath the package for optimal RF and thermal performance.

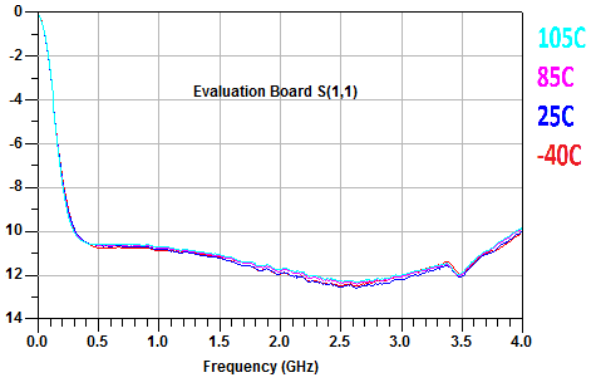

GRF4003 Evaluation Board Gain vs. Frequency and Vd
25
20
15
10
5
0
Gain (dB)
700
1960
2600
3600
Freq (MHz)
4.0V (96 mA)
3.6V (72 mA)
3.3V (69 mA)
3.0V (66 mA)
2.7V (64 mA)
1.8V (56 mA)

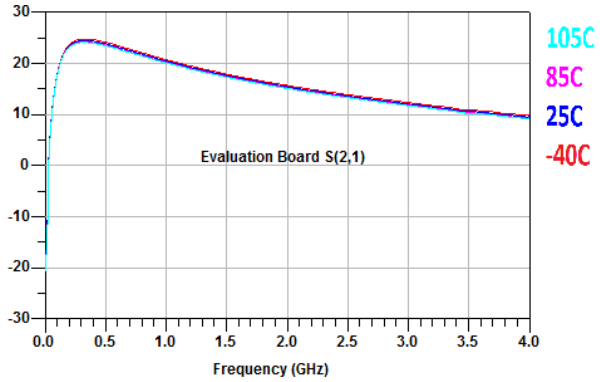

GRF4003 Evaluation Board OIP3 vs. Frequency and Vd
OIP3 (dBm)
44
43
42
41
40
39
38
37
36
35
34
33
32
700
1960
2600
3600
Freq (MHz)
4.0V (96 mA)
3.6V (72 mA)
3.3V (69 mA)
3.0V (66 mA)
2.7V (64 mA)
1.8V (56 mA)

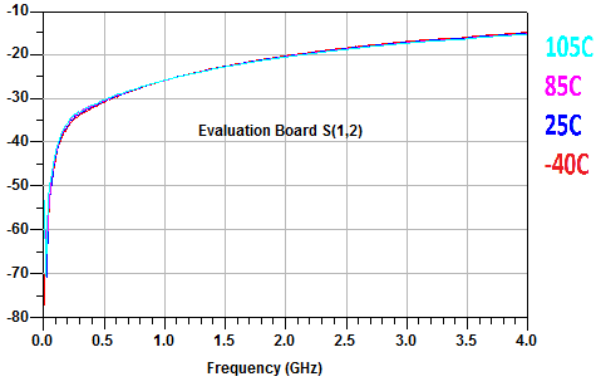

GRF4003 Evaluation Board OP1dB vs. Frequency and Vd
OP1dB (dBm)
30
25
20
15
10
5
0
700
1960
2600
3600
Freq (MHz)
4.0V (96 mA)
3.6V (72 mA)
3.3V (69 mA)
3.0V (66 mA)
2.7V (64 mA)
1.8V (56 mA)

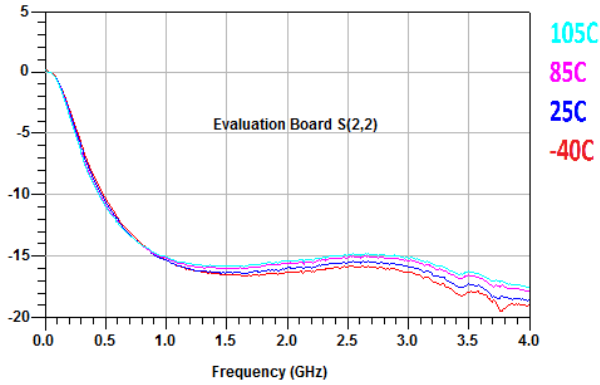

GRF4003 Evaluation Board Noise Figure vs. Frequency and Vd
NF (dB)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
700
1960
2600
3600
Freq (MHz)
4.0V 96 mA
3.6V 72 mA
3.3V 69 mA
3.0V 66 mA
2.7V 64 mA
1.8V 56 mA

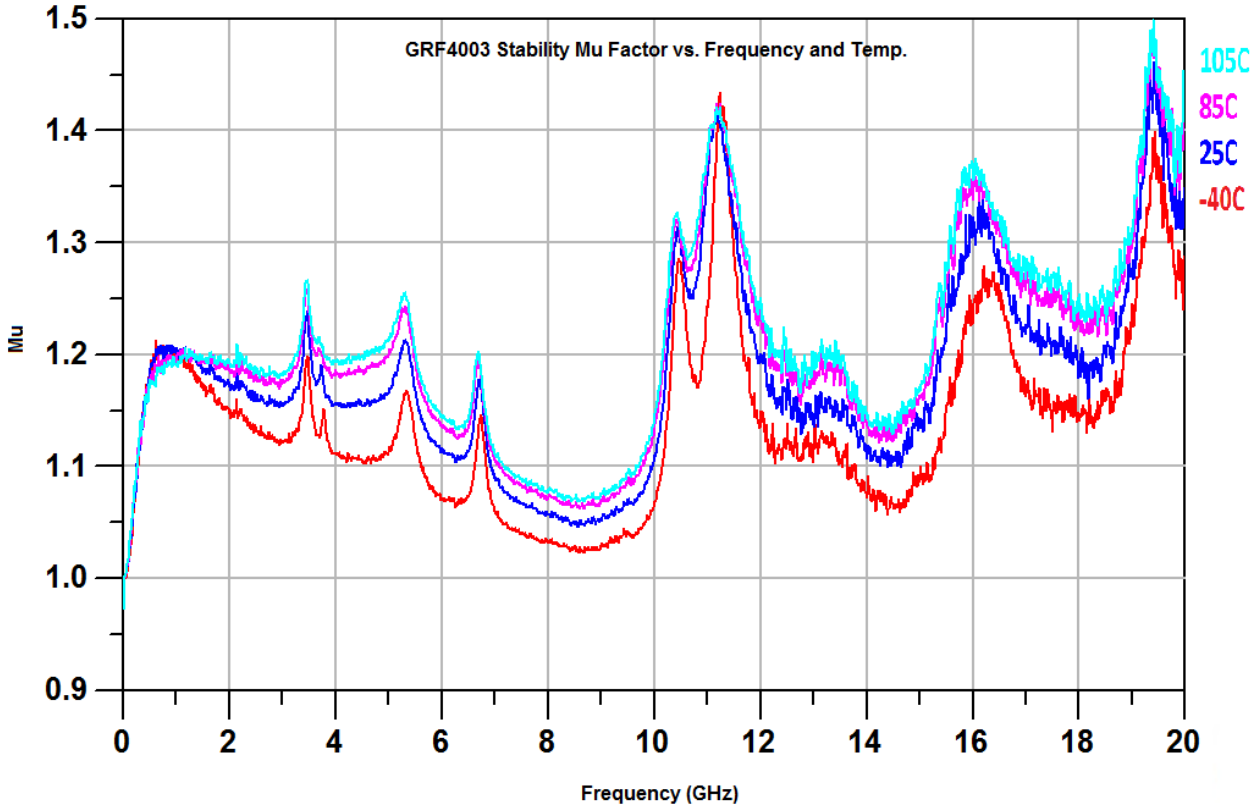

GRF4003 De-embedded NF vs. Frequency and Temp.
Vd: 3.3 V; Iddq: 70 mA
NF (dB)
1.5
1.4
1.3
1.2
1.1
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-40
25
85
105
Temp (deg C)
700
1960
2600
3600


Evaluation Board S(1,1)
105C
85C
25C
-40C
Frequency (GHz)

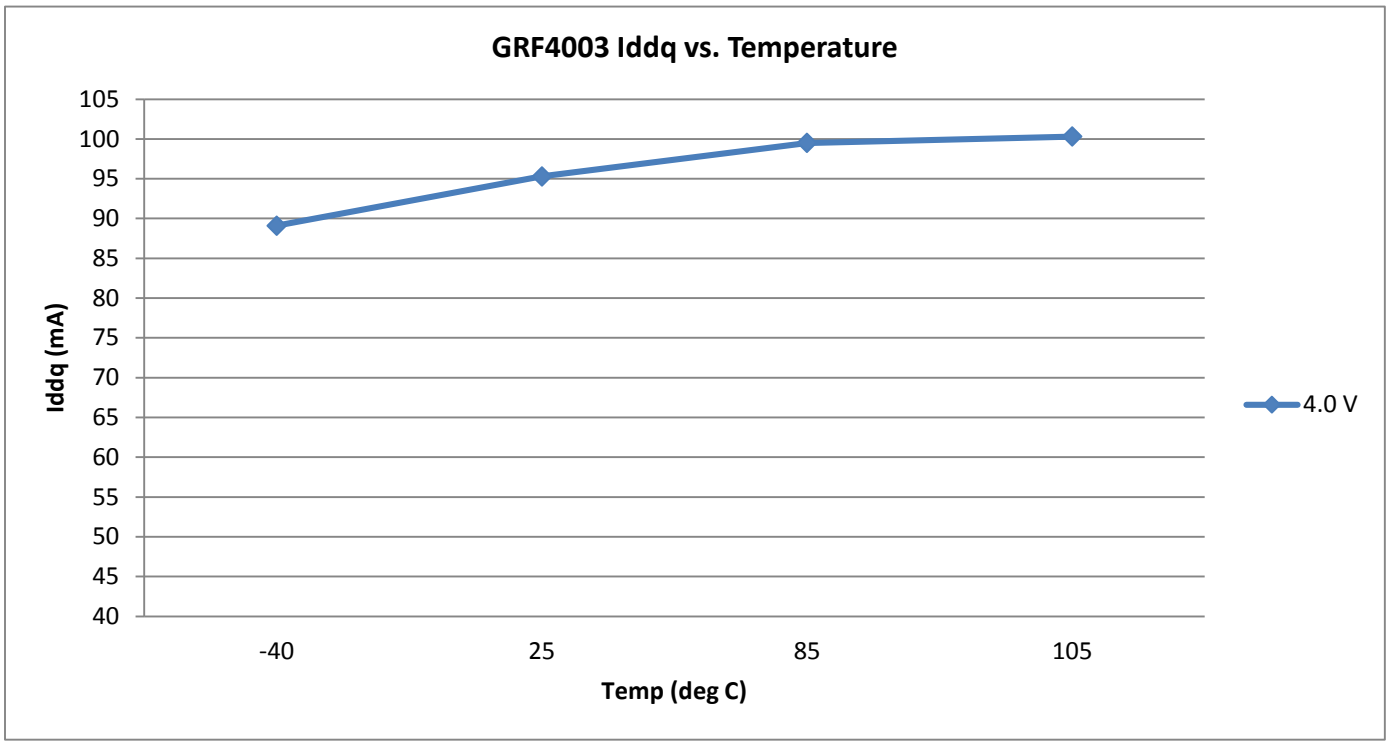

Evaluation Board S(2,1)
105C
85C
25C
-40C
Frequency (GHz)

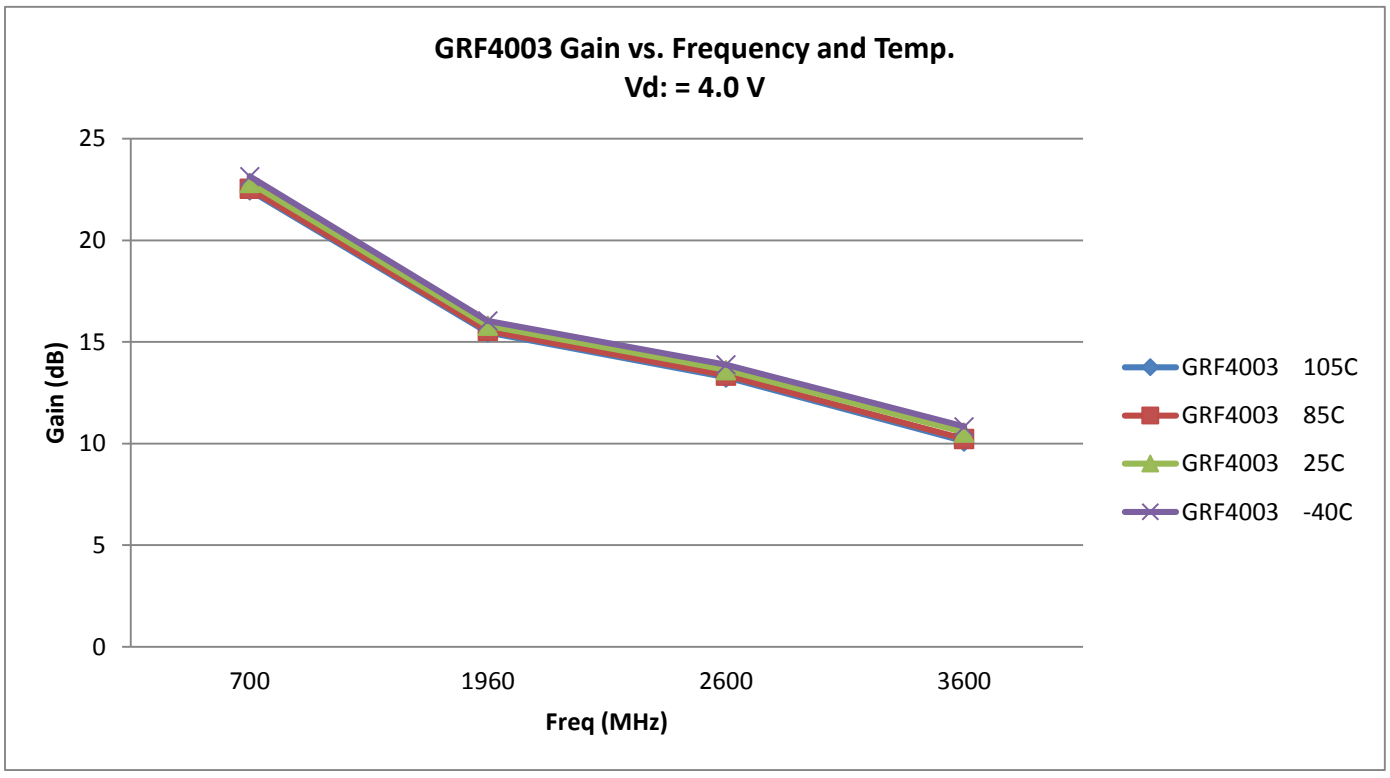

Evaluation Board S(1,2)
105C
85C
25C
-40C
Frequency (GHz)

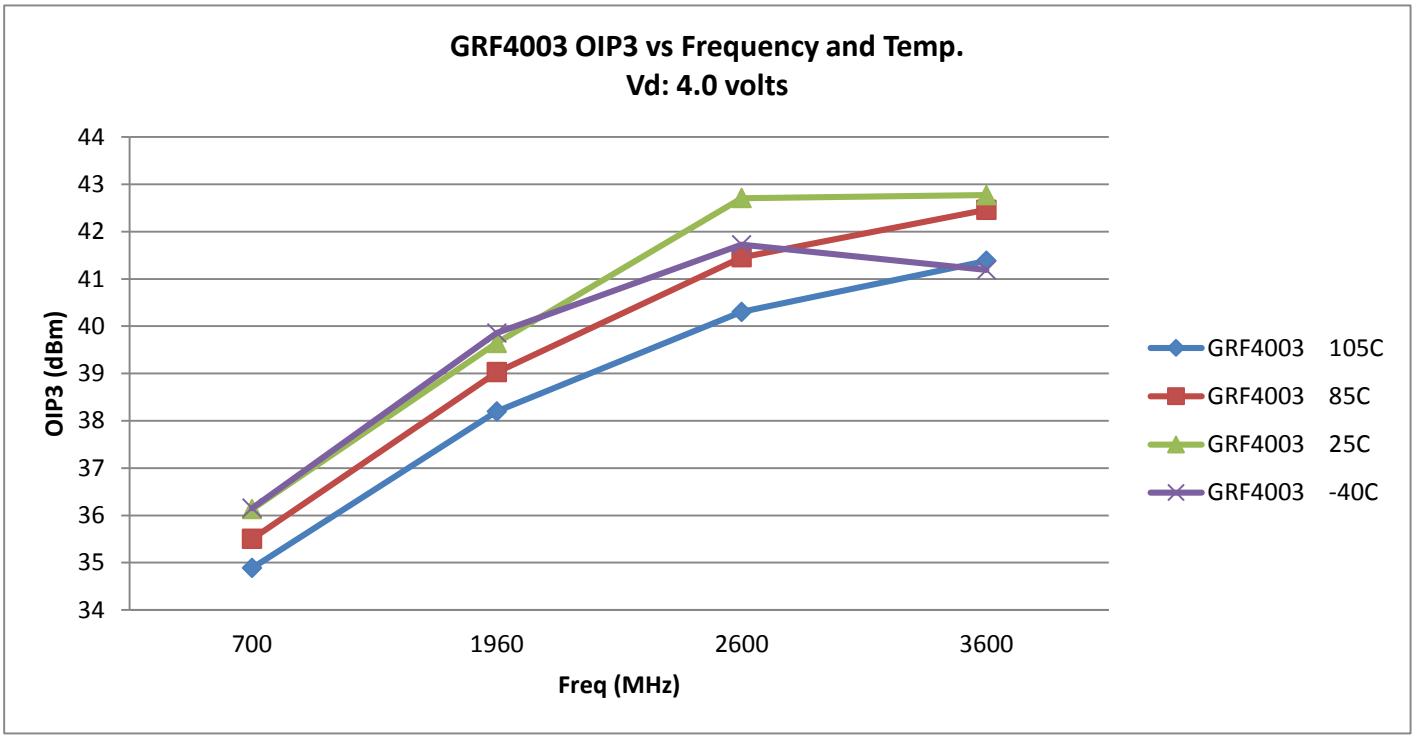

Evaluation Board S(2,2)
105C
85C
25C
-40C
Frequency (GHz)

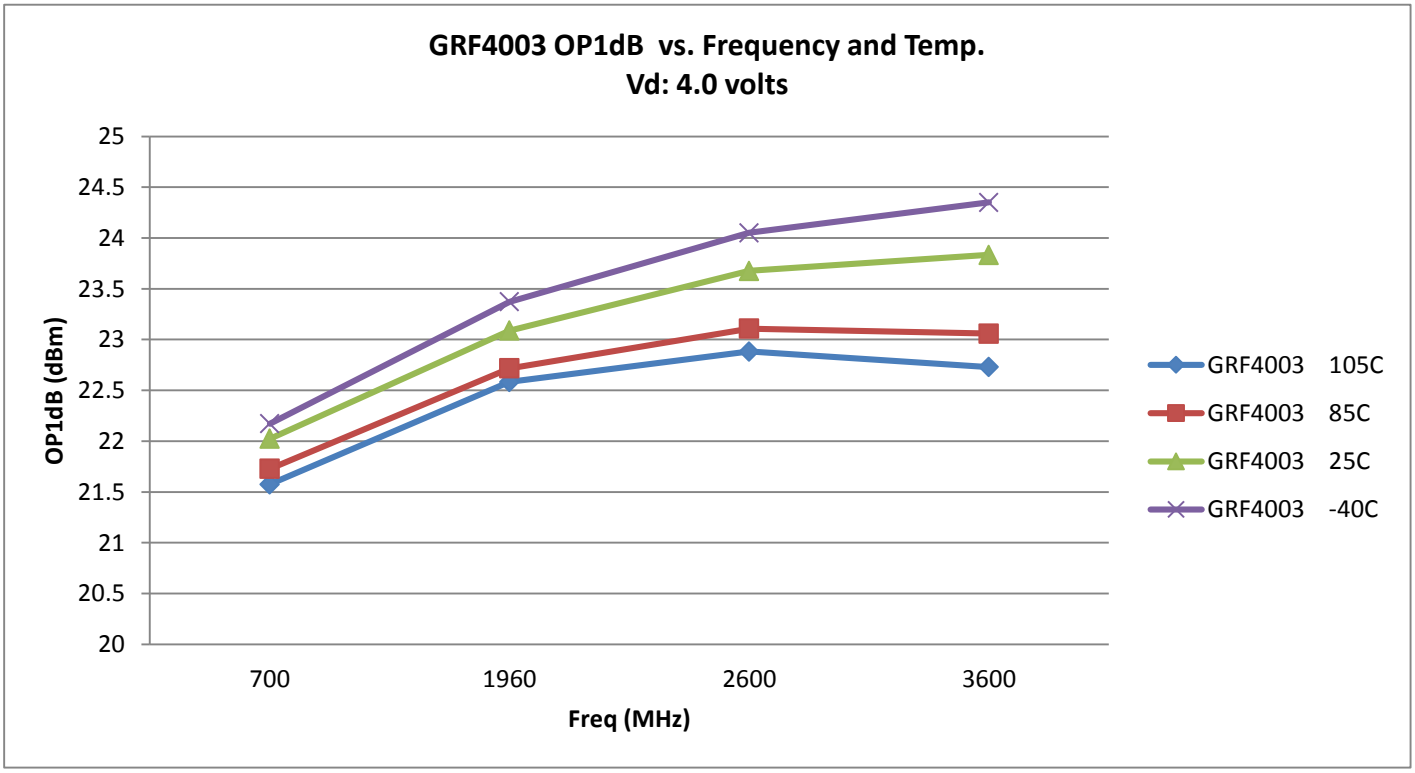

GRF4003 Stability Mu Factor vs. Frequency and Temp.
105C
85C
25C
-40C
Mu
Frequency (GHz)

4.0 Volt Evaluation Board Performance:

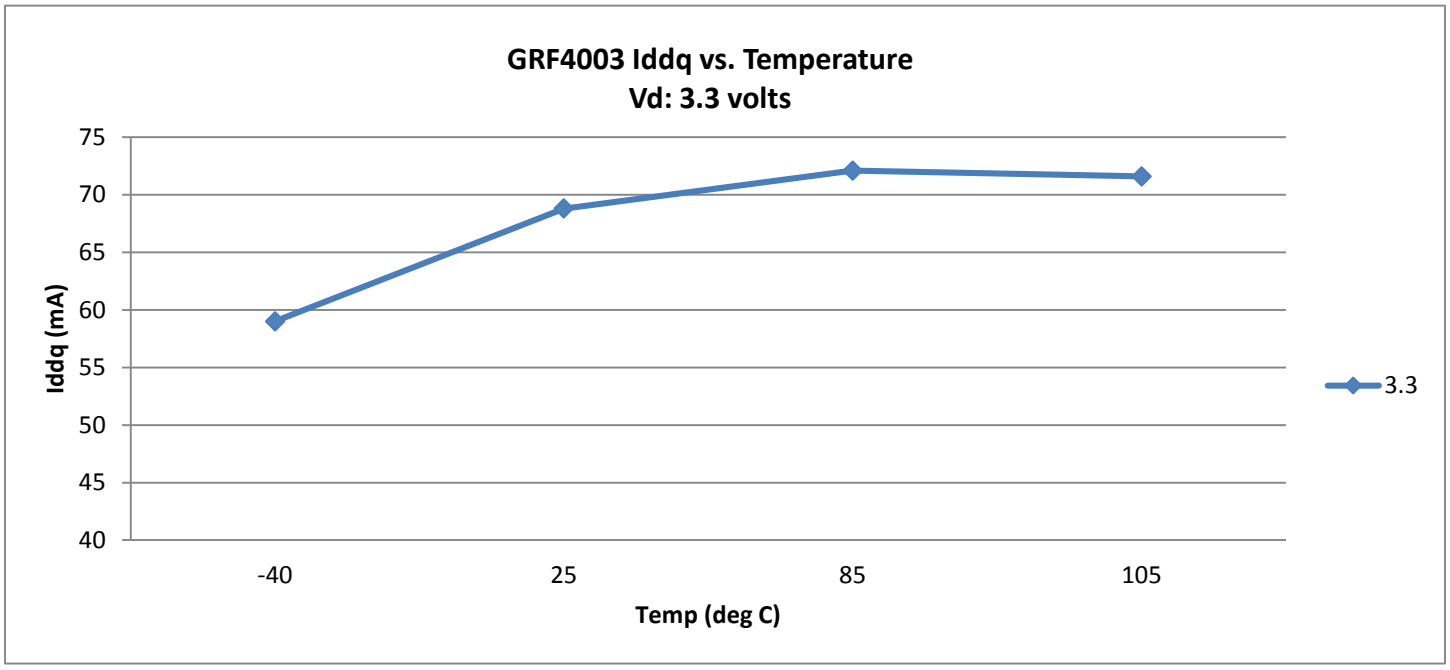


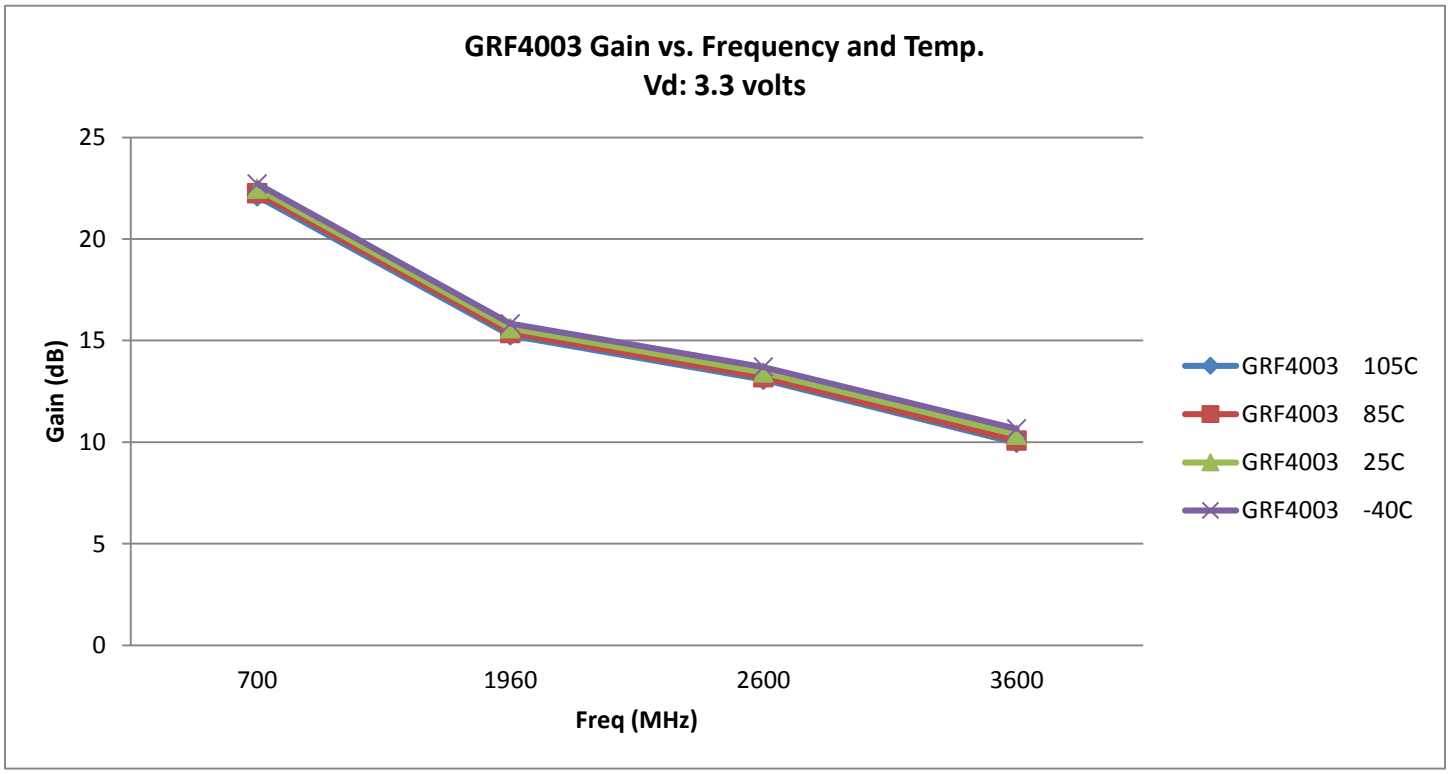


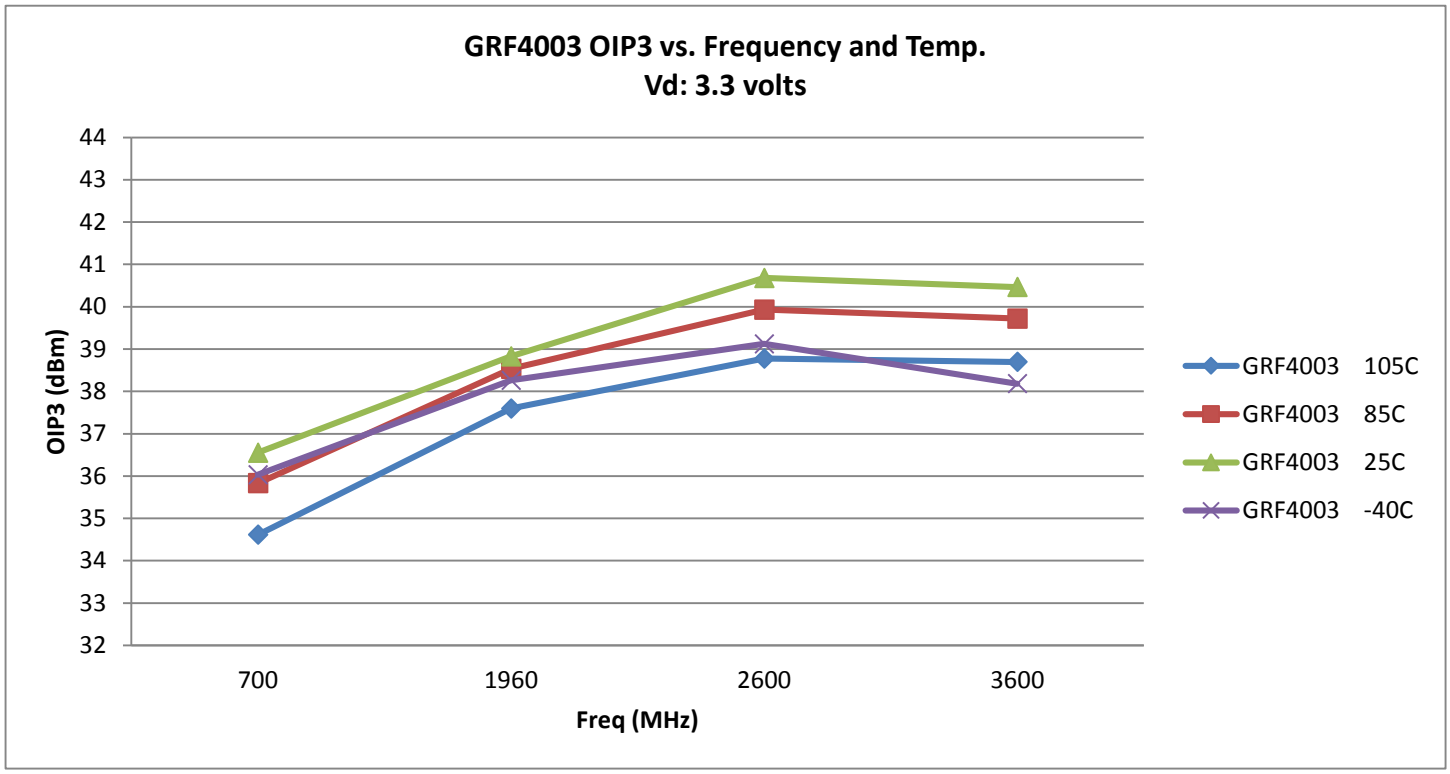

GRF4003 OIP3 vs Frequency and Temp.
Vd: 4.0 volts
OIP3 (dBm)
44
43
42
41
40
39
38
37
36
35
34
700
1960
2600
3600
Freq (MHz)
GRF4003 105C
GRF4003 85C
GRF4003 25C
GRF4003 -40C

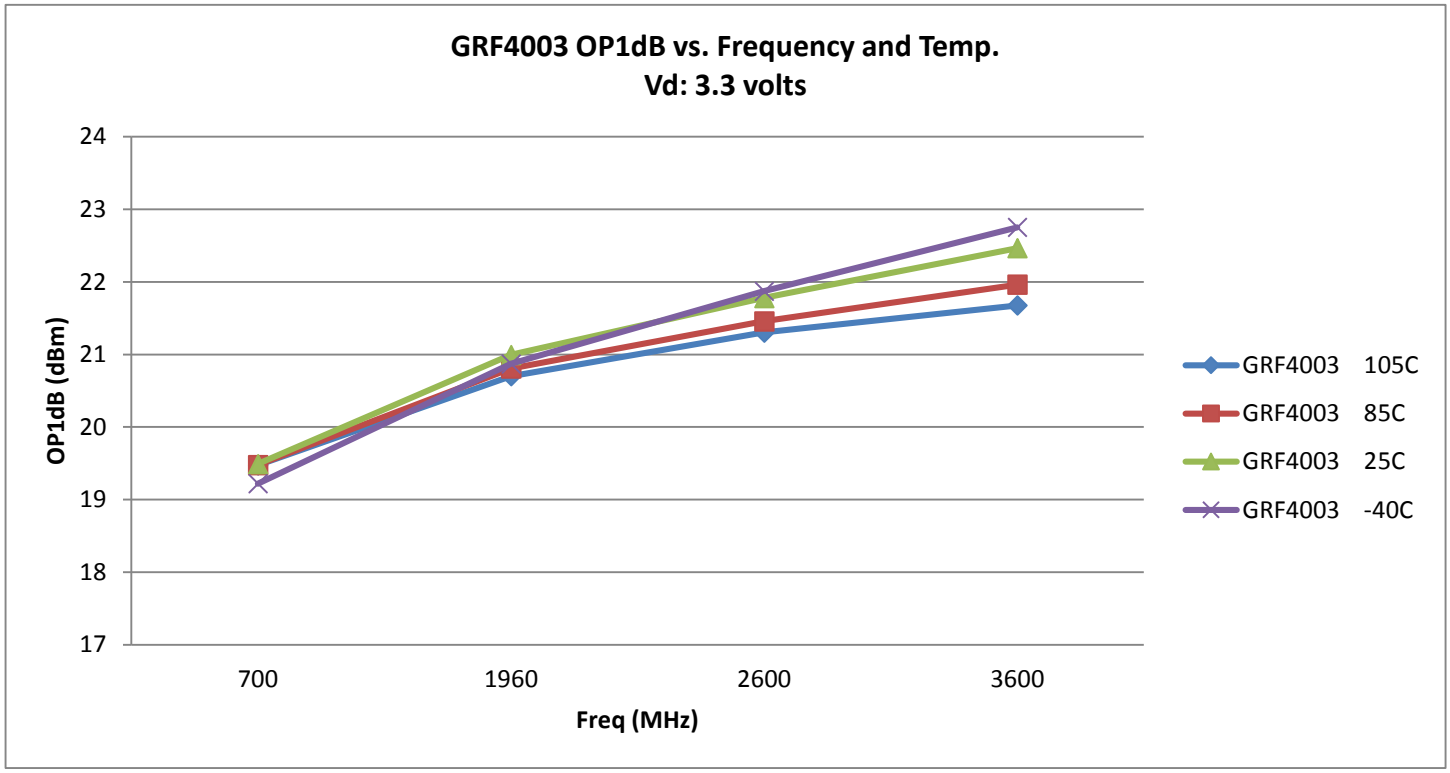

GRF4003 OP1dB vs. Frequency and Temp.
Vd: 4.0 volts
OP1dB (dBm)
25
24.5
24
23.5
23
22.5
22
21.5
21
20.5
20
700
1960
2600
3600
Freq (MHz)
GRF4003 105C
GRF4003 85C
GRF4003 25C
GRF4003 -40C

3.3 Volt Evaluation Board Performance:

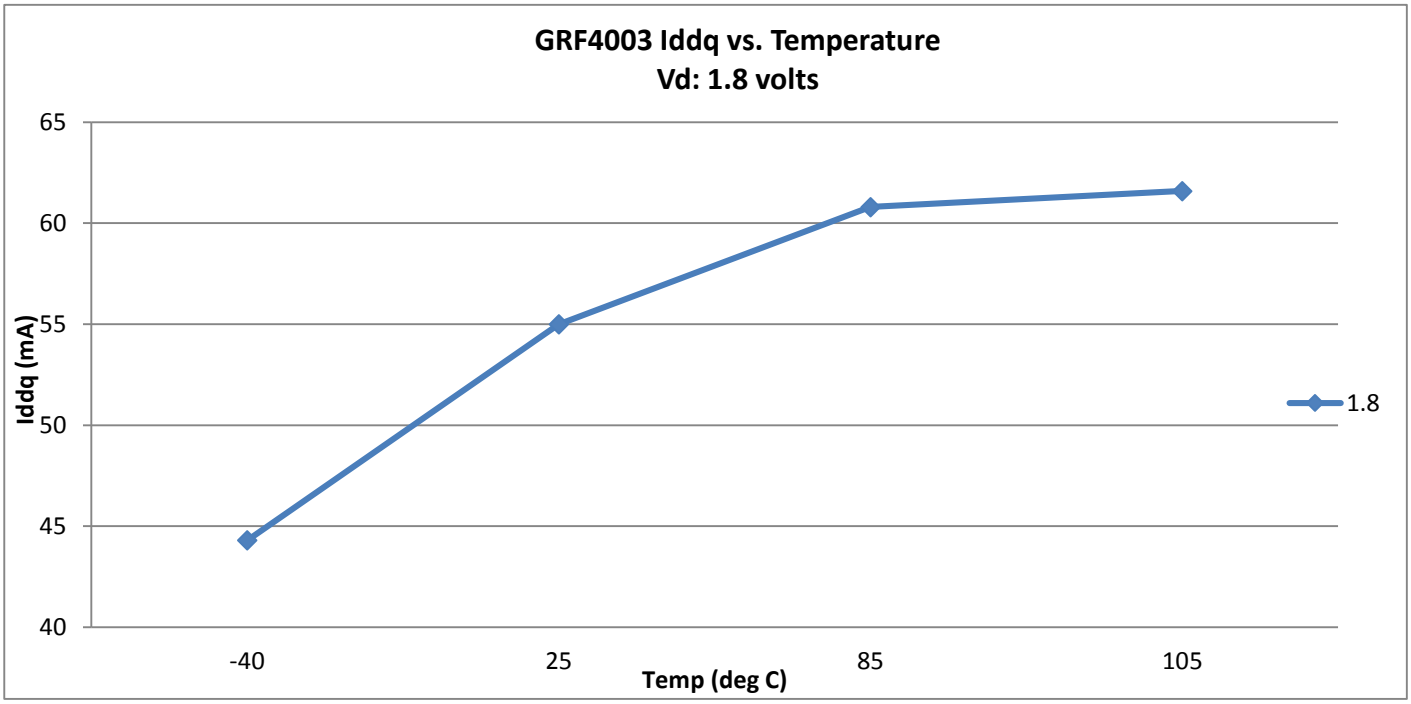


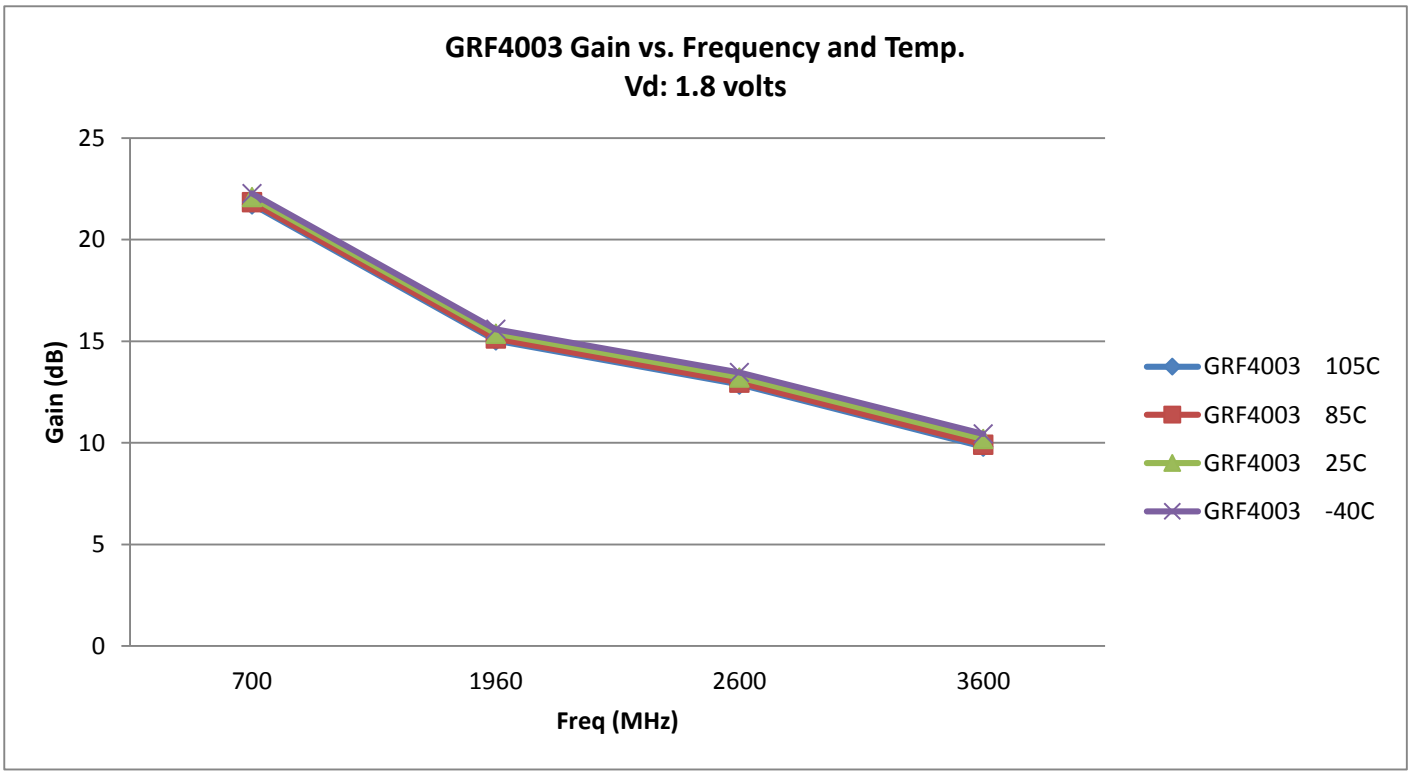


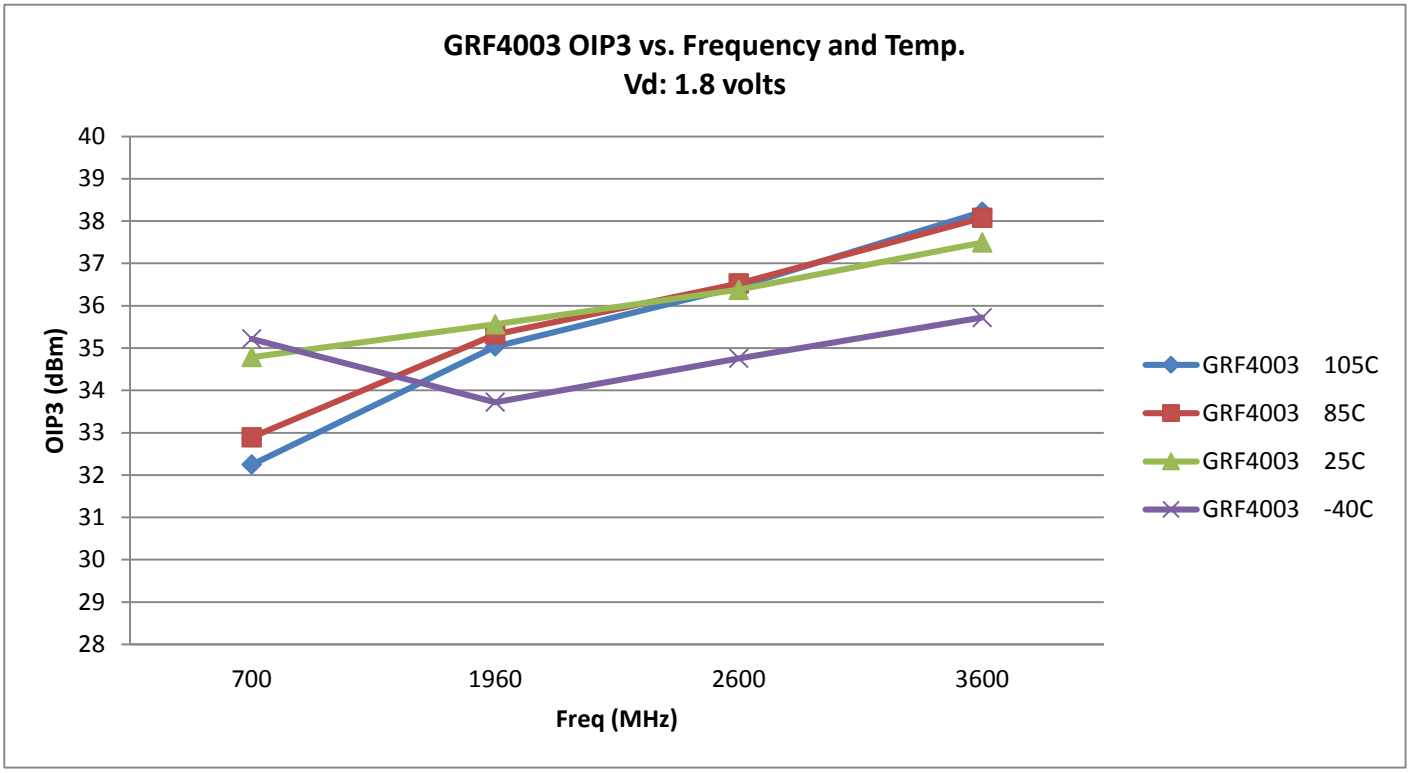

GRF4003 OIP3 vs. Frequency and Temp.
Vd: 3.3 volts
OIP3 (dBm)
44
43
42
41
40
39
38
37
36
35
34
33
32
700
1960
2600
3600
Freq (MHz)
GRF4003 105C
GRF4003 85C
GRF4003 25C
GRF4003 -40C

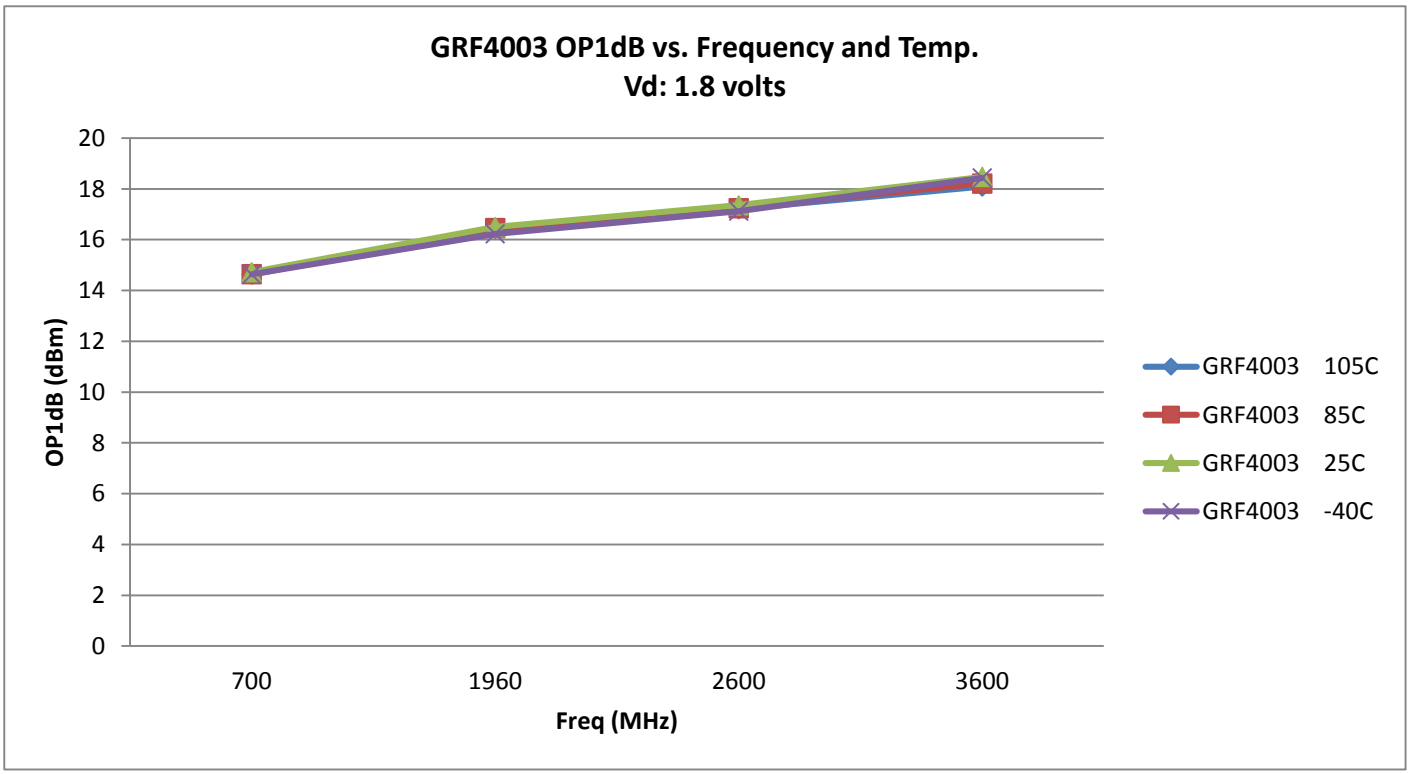

GRF4003 OP1dB vs. Frequency and Temp.
Vd: 3.3 volts
OP1dB (dBm)
24
23
22
21
20
19
18
17
700
1960
2600
3600
Freq (MHz)
GRF4003 105C
GRF4003 85C
GRF4003 25C
GRF4003 -40C

1.8 Volt Evaluation Board Performance:






GRF4003 OIP3 vs. Frequency and Temp.
Vd: 1.8 volts
OIP3 (dBm)
40
39
38
37
36
35
34
33
32
31
30
29
28
700
1960
2600
3600
Freq (MHz)
GRF4003 105C
GRF4003 85C
GRF4003 25C
GRF4003 -40C


GRF4003 OP1dB vs. Frequency and Temp.
Vd: 1.8 volts
OP1dB (dBm)
20
18
16
14
12
10
8
6
4
2
0
700
1960
2600
3600
Freq (MHz)
GRF4003 105C
GRF4003 85C
GRF4003 25C
GRF4003 -40C

GRF4003 Theory of Operation:

The GRF4003 is a single-stage, high-performance, low noise linear amplifier that is suitable for a wide range of applications. The device is internally matched to 50 ohms and covers 100-3800 MHz with a single set of DC blocking caps (M1) and (M7) and bias inductor (M6).

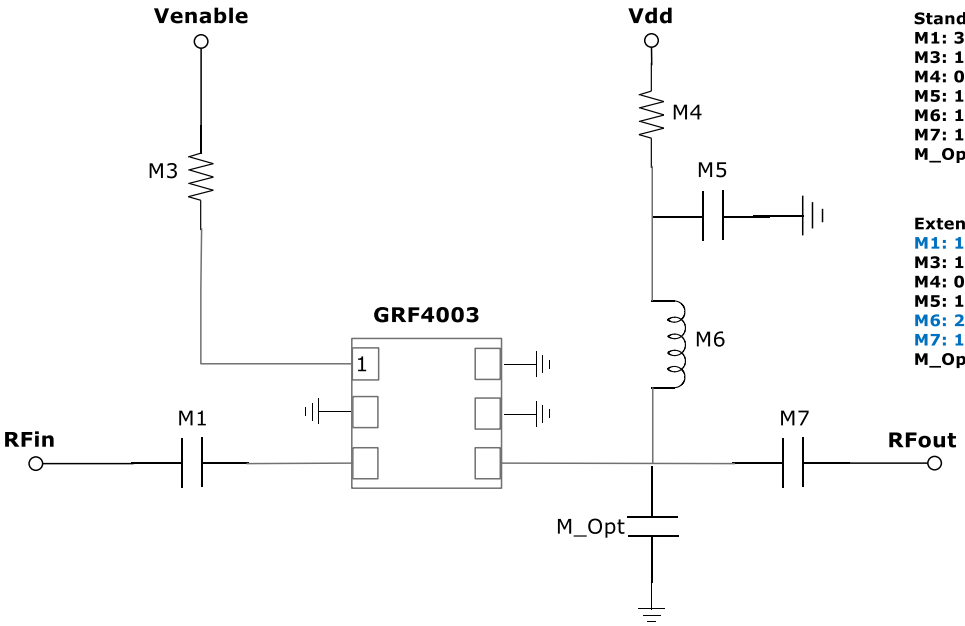
The device Iddq can be set independently from the drain voltage Vd via the resistor M3 in series with Venable. This allows the device Iddq to be optimized to meet a given linearity requirement with the highest possible efficiency. For a given Venable, increasing M3 will result in lower Iddq. As shown in the data sheet plots, GRF4003 exhibits excellent gain, NF and linearity over a wide range of Vd values from 1.8 V up to 4.0 V. The tables on the following page show bias resistor M3 values and resulting Iddq for a wide range of Venable and Vdd settings. The standard evaluation board is populated with a 1k Ohm resistor at M3 for evaluation purposes. With this resistor in place, the Venable voltage can be varied to achieve the desired Iddq to meet the target linearity requirements. The GRF applications team sees little performance benefit from GRF4003 Iddq values greater than 100 mA.

A note about biasing GRF4003 with supply voltage Vdd levels > 4.0 volts: Applications in which the average output power is expected to approach OP1dB should use a small valued resistor in series with Vdd (M4) to drop Vd to around 4.0 - 4.1 volts. This is necessary to prevent excessive self-biasing of the device especially at low temperatures. As an example, with Iddq set to 100 mA, the net resistance of M4 plus the DC resistance of the bias inductor M6 should be roughly 5 ohms for a Vdd of 4.5 volts and 10 ohms for a Vdd of 5.0 volts. At a 4.0 Vd, the GRF4003 will yield excellent OIP3 and OP1dB so there is little performance hit from the series R. Device applications with Vdd at 4.0 volts or lower or those in which the average output power will not approach the device compression point do not need to accommodate the series bias R (M4) and it can be omitted from the application schematic.

M_Opt is a 0.5 pF capacitor which was added to the application schematic and evaluation board to slightly optimize the device return losses.

GRF4003 Bias Resistor vs. Iddq Tables

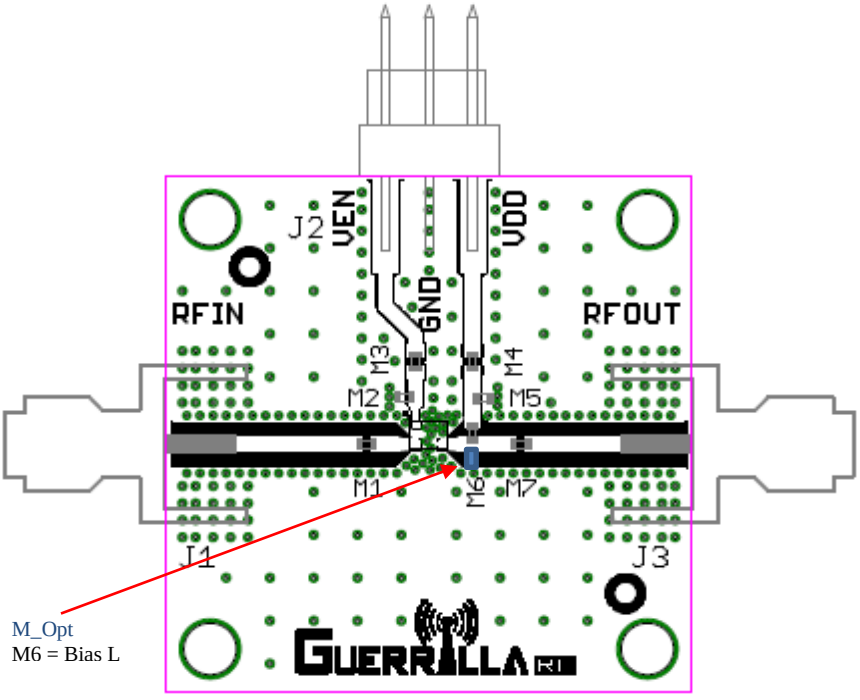
Device	Vdd	Venable	M3 (ohms)	Iddq (mA)		Device	Vdd	Venable	M3 (ohms)	Iddq (mA)		Device	Vdd	Venable	M3 (ohms)	Iddq (mA)
GRF4003	5.0	5.0	1500	100		GRF4003	4.5	4.5	1500	90		GRF4003	4.0	4.0	1000	97
GRF4003	5.0	5.0	2000	88		GRF4003	4.5	4.5	2000	80		GRF4003	4.0	4.0	1500	80
GRF4003	5.0	5.0	2500	80		GRF4003	4.5	4.5	2500	71		GRF4003	4.0	4.0	2000	70
GRF4003	5.0	5.0	3000	72		GRF4003	4.5	4.5	3000	64		GRF4003	4.0	4.0	2500	62
GRF4003	5.0	5.0	4000	61		GRF4003	4.5	4.5	4000	55		GRF4003	4.0	4.0	3000	55
GRF4003	5.0	5.0	5000	54		GRF4003	4.5	4.5	5000	48		GRF4003	4.0	4.0	4000	47
GRF4003	5.0	5.0	6000	49		GRF4003	4.5	4.5	6000	43		GRF4003	4.0	4.0	5000	37
GRF4003	5.0	5.0	7000	45		GRF4003	4.5	4.5	7000	39		GRF4003	4.0	4.0	6000	35
GRF4003	5.0	5.0	8000	41		GRF4003	4.5	4.5	8000	36		GRF4003	4.0	4.0	7000	32
GRF4003	5.0	5.0	10000	37		GRF4003	4.5	4.5	10000	32		GRF4003	4.0	4.0	8000	29
GRF4003	5.0	5.0	20000	24		GRF4003	4.5	4.5	15000	24		GRF4003	4.0	4.0	10000	26
GRF4003	5.0	5.0	30000	19		GRF4003	4.5	4.5	20000	20		GRF4003	4.0	4.0	15000	20
Device	**Vdd**	**Venable**	**M3 (ohms)**	**Iddq (mA)**		**Device**	**Vdd**	**Venable**	**M3 (ohms)**	**Iddq (mA)**		**Device**	**Vdd**	**Venable**	**M3 (ohms)**	**Iddq (mA)**
GRF4003	3.3	3.3	750	89		**GRF4003**	3.0	3.0	500	98		GRF4003	1.8	1.8	100	91
GRF4003	3.3	3.3	1000	78		**GRF4003**	3.0	3.0	750	80		GRF4003	1.8	1.8	150	83
GRF4003	3.3	3.3	1500	64		**GRF4003**	3.0	3.0	1000	70		GRF4003	1.8	1.8	200	76
GRF4003	3.3	3.3	2000	55		**GRF4003**	3.0	3.0	1500	58		GRF4003	1.8	1.8	300	67
GRF4003	3.3	3.3	2500	49		**GRF4003**	3.0	3.0	2000	49		GRF4003	1.8	1.8	400	61
GRF4003	3.3	3.3	3000	43		**GRF4003**	3.0	3.0	2500	43		GRF4003	1.8	1.8	500	57
GRF4003	3.3	3.3	4000	36		**GRF4003**	3.0	3.0	3000	39		GRF4003	1.8	1.8	750	47
GRF4003	3.3	3.3	5000	32		**GRF4003**	3.0	3.0	4000	32		GRF4003	1.8	1.8	1000	40
GRF4003	3.3	3.3	6000	28		**GRF4003**	3.0	3.0	5000	28		GRF4003	1.8	1.8	1500	32
GRF4003	3.3	3.3	7000	25		**GRF4003**	3.0	3.0	6000	25		GRF4003	1.8	1.8	2000	27
GRF4003	3.3	3.3	8000	23		**GRF4003**	3.0	3.0	7000	22		GRF4003	1.8	1.8	2500	23
GRF4003	3.3	3.3	10000	20		**GRF4003**	3.0	3.0	8000	20		GRF4003	1.8	1.8	3000	20



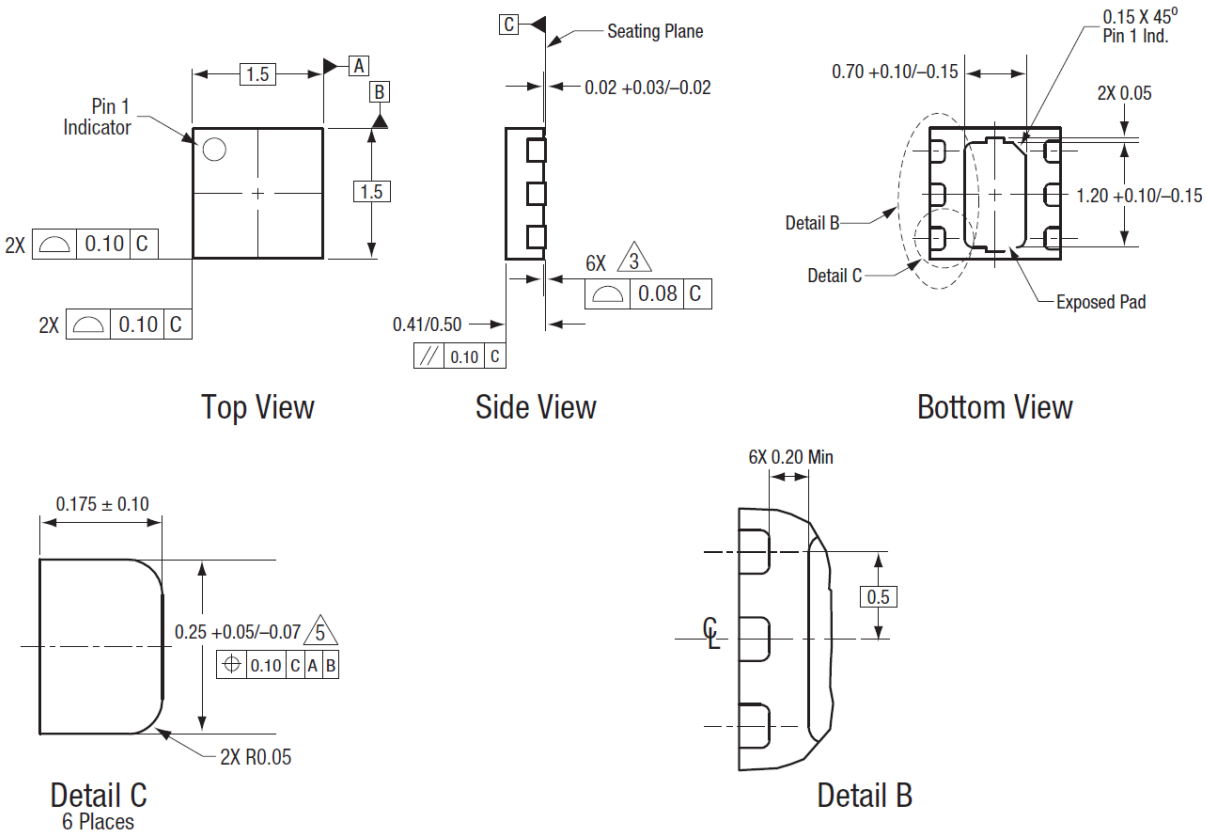
Standard BOM: 700-3800 MHz
M1: 30 pF (High Q)
M3: 1000 Ohm (Placeholder)
M4: 0 Ohm
M5: 1.0 uF
M6: 100 nH wire wound
M7: 10 pF
M_Opt: 0.5 pF

Extended BW BOM: 100-3800 MHz
M1: 100 pF (High Q)
M3: 1000 Ohm (Placeholder)
M4: 0 Ohm
M5: 1.0 uF
M6: 220 nH wire wound
M7: 100 pF
M_Opt: 0.5 pF

GRF4003 Evaluation Board Application Schematic

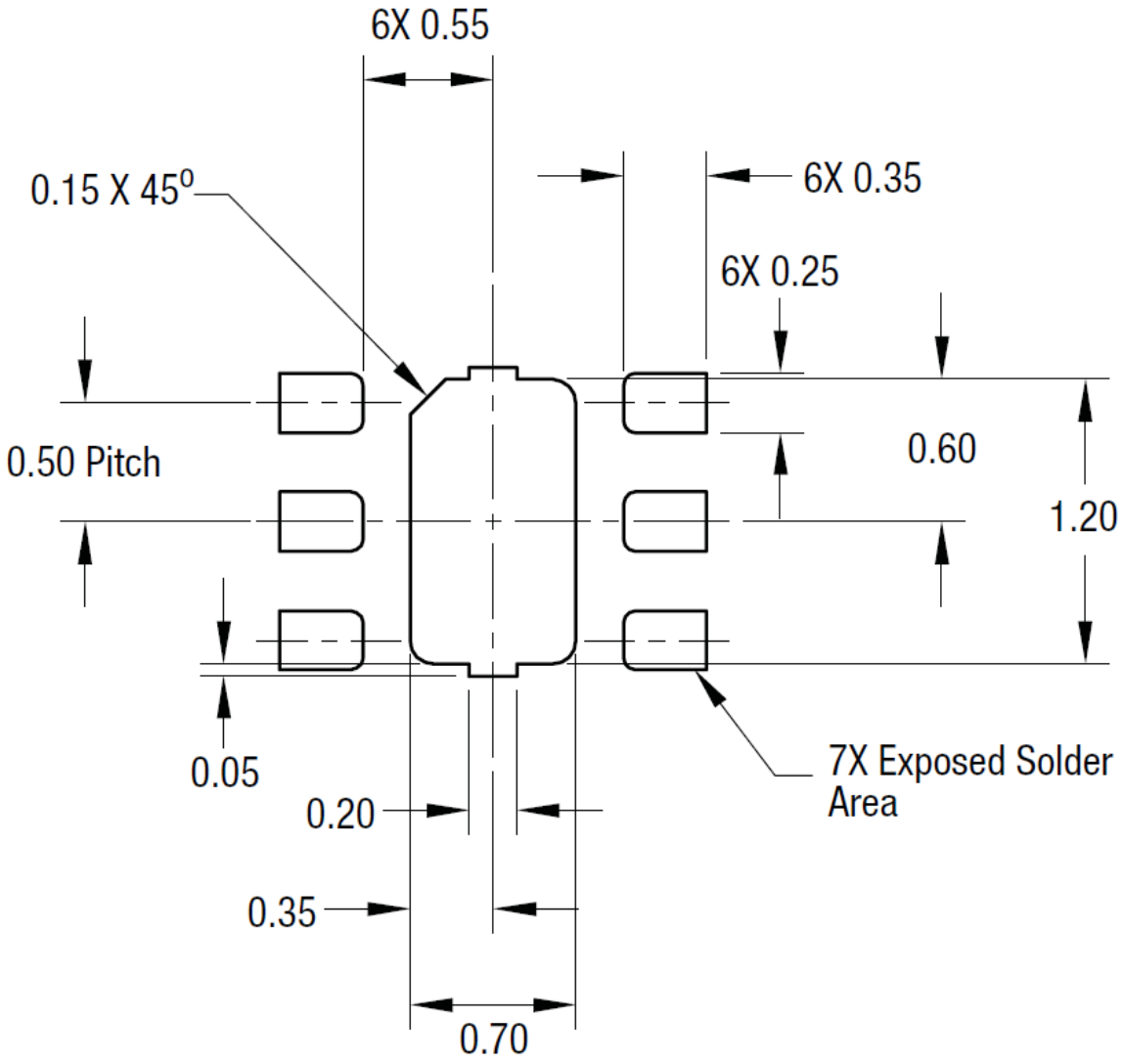


GRF400X Evaluation Board Assembly Diagram



All measurements are in millimeters.
Dimensioning and tolerancing according to ASME Y14.5M-1994.
Coplanarity applies to the exposed heat sink slug as well as the terminals..
Plating requirement per source control drawing (SCD) 2504.
Dimension applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

GRF4003 1.5mm x 1.5mm 6-Pin DFN Package Dimensions



GRF4003 1.5mm x 1.5mm 6-Pin DFN PCB Layout Footprint