PRELIMINARY DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUITS

μPC2757TB, μPC2758TB

SILICON MMIC 1st FREQUENCY DOWNCONVERTER FOR CELLULAR/CORDLESS TELEPHONE

DESCRIPTION

The μPC2757TB and μPC2758TB are silicon monolithic integrated circuit designed as 1st frequency downconverter for cellular/cordless telephone receiver stage. The ICs consist of mixer and local amplifier. The μPC2757TB features low current consumption and the μPC2758TB features improved intermodulation. From these two version, you can chose either IC corresponding to your system design. These TB suffix ICs which are smaller package than conventional T suffix ICs contribute to reduce your system size.

The μPC2757TB and μPC2758TB are manufactured using NEC's 20 GHz fT NESAT™III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability

FEATURES

- Wideband operation : f_{RFin} = 0.1 GHz to 2.0 GHz, f_{IFin} = 20 MHz to 300 MHz
- High-density surface mounting : 6-pin super mini mold package
- Low current consumption : I_{CC} = 5.6 mA$_{TYP.}$ @ μPC2757TB
  I_{CC} = 11 mA$_{TYP.}$ @ μPC2758TB
- Supply voltage : V_{CC} = 2.7 to 3.3 V
- Minimized carrier leakage : Due to double balanced mixer
- Built-in power save function

APPLICATION

- Cellular/cordless telephone up to 2.0 GHz MAX (eg GSM, PDC800M, PDC1.5G and so on): μPC2758TB
- Cellular/cordless telephone up to 2.0 GHz MAX (eg CT1, CT2 and so on): μPC2757TB

ORDERING INFORMATION

Part Number	Markings	Product Type	PACKAGE	Supplying Form
μPC2757TB-E3	C1X	Low current consumption	6-pin super minimold	Embossed tape 8 mm wide. Pin 1, 2, 3 face to tape perforation side. QTY 3kp/Reel.
μPC2758TB-E3	C1Y	High OIP3		

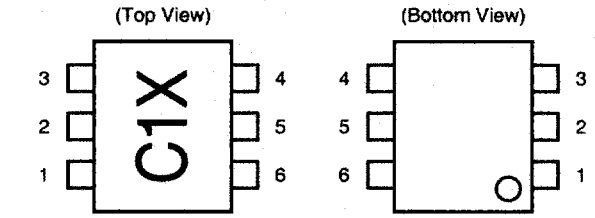
Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μPC2757TB, μPC2758TB)

Caution Electro-static sensitive devices

The information in this document is subject to change without notice.

Document No. P12771EJ1V0DS00 (1st edition)
Date Published August 1998 CP(K)
Printed in Japan

PIN CONNECTIONS



Example marking is for μPC2757TB

Pin NO.	Pin name
1	RF in
2	GND
3	LOin
4	PS
5	Vcc
6	IFout

PRODUCT LINE-UP (T_A = +25 °C, V_{CC} = 3.0 V, Z_L = Z_S = 50 Ω)

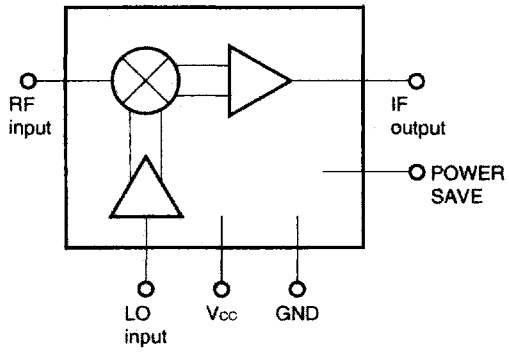
Items / Part No.	No RF I_{CC} (mA)	900 MHz SSB · NF (dB)	1.5 GHz SSB · NF (dB)	1.9 GHz SSB · NF (dB)	900 MHz CG (dB)	1.5 GHz CG (dB)	1.9 GHz CG (dB)	900 MHz IIP_3 (dBm)	1.5 GHz IIP_3 (dBm)	1.9 GHz IIP_3 (dBm)
μPC2757T	5.6	10	10	13	15	15	13	−14	−14	−12
μPC2757TB										
μPC2758T	11	9	10	13	19	18	17	−13	−12	−11
μPC2758TB										
μPC8112T	8.5	9	11	11	15	13	13	−10	−9	−7
μPC8112TB										

Items / Part No.	900 MHz P_{osat} (dBm)	1.5 GHz P_{osat} (dBm)	1.9 GHz P_{Osat} (dBm)	900 MHz RF_{Io} (dB)	1.5 GHz RF_{Io} (dB)	1.9 GHz RF_{Io} (dB)	IF Output Configuration	Packages
μPC2757T	−3	−	−8				Emitter follower	6-pin minimold
μPC2757TB								6-pin super minimold
μPC2758T	+1	−	−4					6-pin minimold
μPC2758TB								6-pin super minimold
μPC8112T	−2.5	−3	−3	−80	−57	−55	Open collector	6-pin minimold
μPC8112TB								6-pin super minimold

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.
To know the associated product, please refer to each latest data sheet.

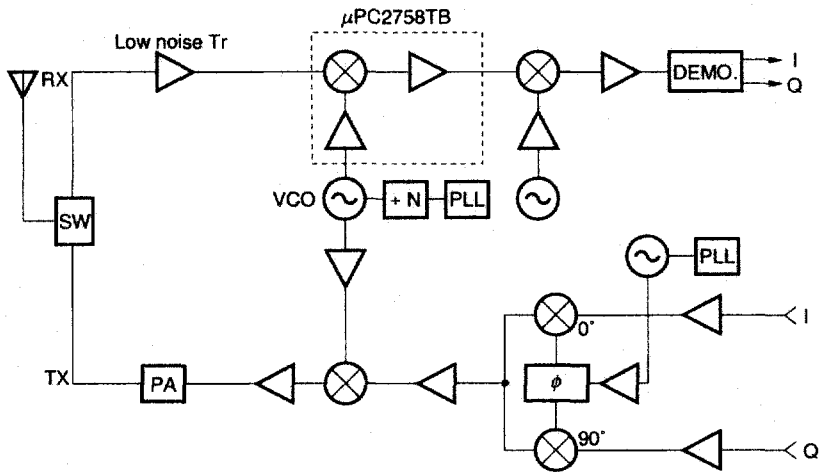
Notice μPC2757 and μPC2758's IIP_3 are calculated with ΔIM_3 = 3 which is the same IM_3 inclination as μPC8112.
On the other hand, OIP_3 of Standard characteristics in page 4 is cross point IP.

INTERNAL BLOCK DIAGRAM (μPC2757TB, μPC2758TB in common)



SYSTEM APPLICATION EXAMPLE

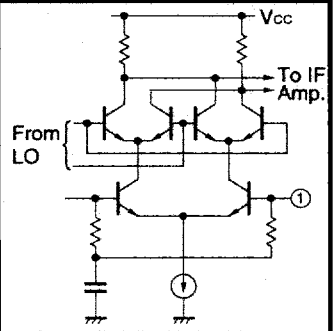
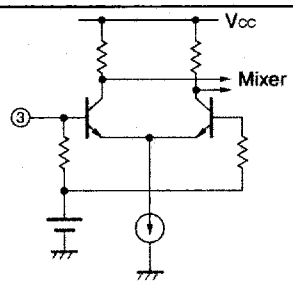
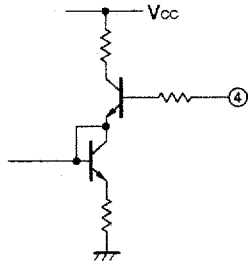
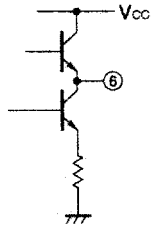
DIGITAL CELLULAR TELEPHONE



These examples show only IC's location on the system use schematically, do not present or recommend the actual application circuit in detail.

To know the associated products, please refer to each latest data sheet.

PIN EXPLANATION (Both μPC2757TB, 2758TB)

Pin No.	Pin Name	Applied Voltage V	Pin Voltage V[Note]	Function and Application	Internal Equivalent Circuit
1	RF in	–	1.2	This pin is RF input for mixer designed as double balance type. This circuit contributes to suppress spurious signal with minimum LO and bias power consumption. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution.	
2	GND	GND	–	This pin is ground of IC. Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible.)	–
3	LO in	–	1.3	This pin is LO input for local buffer designed as differential amplifier. Recommendable input level is –15 to –0 dBm. Also this symmetrical circuit can keep specified performance insensitive to process-condition distribution.	
4	PS	Vcc/GND	–	This pin is for power-save function. This pin can control ON/OFF operation with bias as follows; <table><tr><th></th><th>Bias: V</th><th>Operation</th></tr><tr><td rowspan="2">VPS</td><td>≥ 2.5</td><td>ON</td></tr><tr><td>0 - 0.5</td><td>OFF</td></tr></table> Rise time/fall time using this pin are approximately 10 μs.	
5	Vcc	2.7 - 3.3	–	Supply voltage 3.0 ±0.3 V for operation. Must be connected bypass capacitor. (e.g. 1 000 pF) to minimize ground impedance.	–
6	IF out	–	1.7	This pin is output from IF buffer amplifier designed as single-ended push-pull type. This pin is assigned for emitter follower output with low-impedance. In the case of connecting to high-impedance stage, please attach external matching circuit.	

Note Each pin voltage is measured with Vcc = 3.0 V

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25 °C	5.5	V
PS Pin Voltage	V_{PS}	T_A = +25 °C	5.5	V
Power Dissipation of Package Allowance	P_D	Mounted on 50 × 50 × 1.6 mm double sided copper clad epoxy glass board at T_A = +85 °C	200	mW
Operating Ambient Temperature	T_A		−40 to +85	°C
Storage Temperature	T_{stg}		−55 to +150	°C

RECOMMENDED OPERATING RANGE

Parameters	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}	2.7	3.0	3.3	V
Operating Ambient Temperature	T_A	−40	+25	+85	°C
LO Input Level	P_{LOin}	−15	−10	0	dBm

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = V_{PS} = 3.0 V, P_{LOin} = −10 dBm, Z_L = Z_S = 50 Ω)

Parameters	Symbol	Conditions	μPC2757TB			μPC2758TB			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Circuit Current	I_{CC}	No input signal	3.7	5.6	7.7	6.6	11	14.8	dB
RF Frequency Response	f_{RF}	CG ≥ (CG1 −3 dB) f_{IFout} = 130 MHz constant	0.1		2.0	0.1		2.0	GHz
IF Frequency Response	f_{IF}	CG ≥ (CG1 −3 dB) f_{RFin} = 0.8 GHz constant	20		300	20		300	MHz
Conversion Gain 1	CG1	f_{RFin} = 0.8 GHz, f_{IFout} = 130 MHz P_{RFin} = −40 dBm, Upper local	12	15	18	16	19	22	dB
Conversion Gain 2	CG2	f_{RFin} = 2.0 GHz, f_{IFout} = 250 MHz P_{RFin} = −40 dBm, Lower local	10	13	16	14	17	20	dB
Single Sideband Noise Figure 1	SSB NF1	f_{RFin} = 0.8 GHz, f_{IFout} = 130 MHz, Upper local		10	13		9	12	dB
Single Sideband Noise Figure 2	SSB NF2	f_{RFin} = 2.0 GHz, f_{IFout} = 250 MHz, Lower local		13	16		13	15	dB
Maximum IF Output Level 1	$P_{O(SAT)}$ 1	f_{RFin} = 0.8 GHz, f_{IFout} = 130 MHz P_{RFin} = −10 dBm, Upper local	−11	−3		−7	+1		dBm
Maximum IF Output Level 2	$P_{O(SAT)}$ 2	f_{RFin} = 2.0 GHz, f_{IFout} = 250 MHz P_{RFin} = −10 dBm, Lower local	−11	−8		−7	−4		dBm

STANDARD CHARACTERISTICS FOR REFERENCE

(Unless otherwise specified: T_A = +25 °C, V_{CC} = V_{PS} = 3.0 V, P_{LOin} = −10 dBm, Z_L = Z_S = 50 Ω)

Parameters	Symbol	Conditions	Reference value		Unit
			μPC2757TB	μPC2758TB	
Output 3rd intercept point	OIP_3	f_{RFin} = 0.8 to 2.0 GHz, f_{IFout} = 0.1 GHz, Cross point IP	+5	+11	dBm
LO leakage at RF pin	LO_{rf}	f_{LOin} = 0.8 to 2.0 GHz	−35	−30	dBm
LO leakage at IF pin	LO_{if}	f_{LOin} = 0.8 to 2.0 GHz	−23	−15	dBm
Power-saving current	I_{PS}	V_{PS} = 0.5 V	0.1	0.1	μA

TEST CIRCUIT

μPC2757TB, μPC2758TB

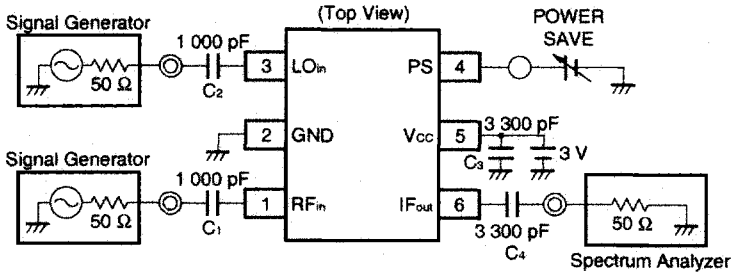
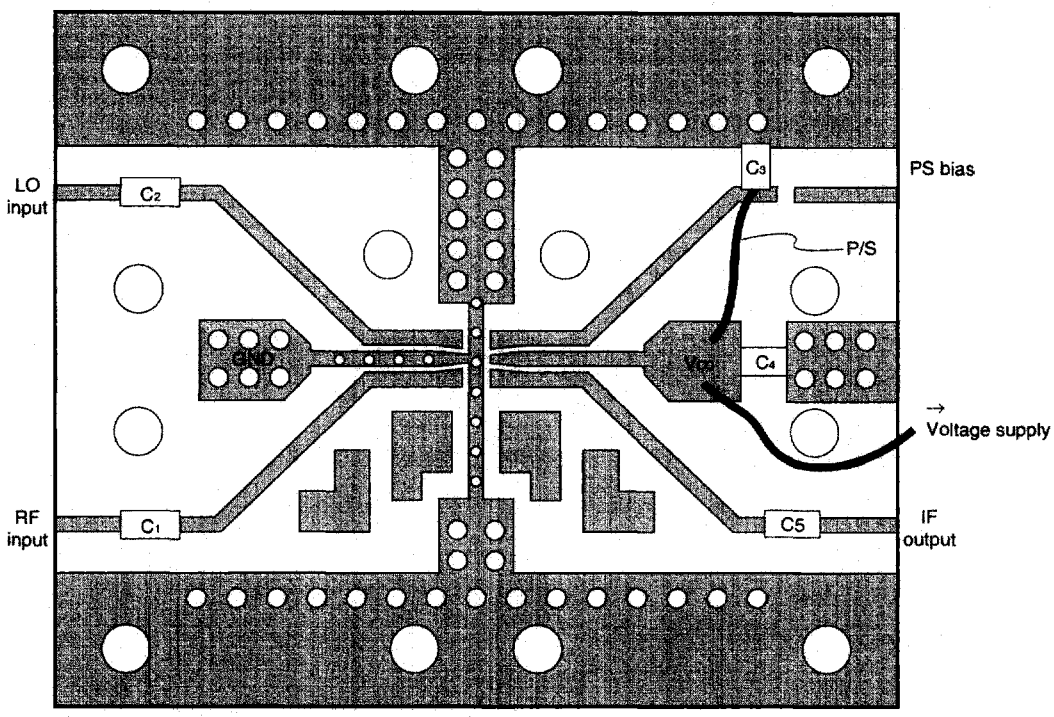


ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



Component List

No.	Value
$C_{1 to 2}$	1 000 pF
$C_{3 to 5}$	3 300 pF

Notes 1. 35 × 42 × 0.4 mm double sided copper clad polyimide board.

2. Back side: GND pattern

3. Solder plated on pattern

4. °O: Through holes

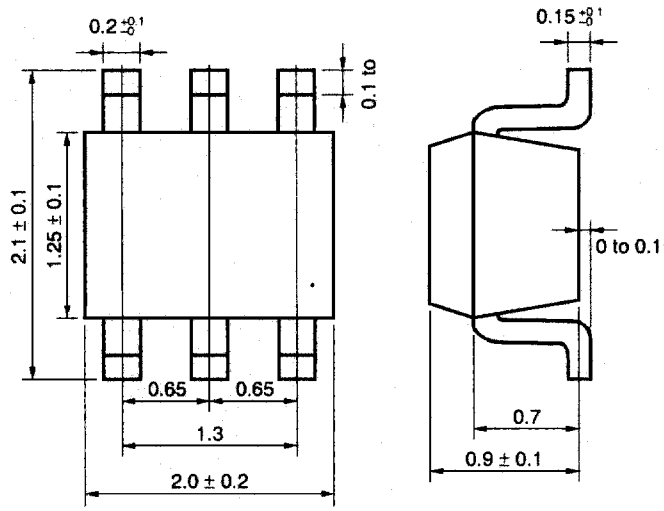
APPLICATION

This IC is guaranteed on the test circuit constructed with 50 Ω equipment and transmission line.

This IC, however, does not have 50 Ω input/output impedance, but electrical characteristics such as conversion gain and intermodulation distortion are described herein on these conditions without impedance matching. So, you should understand that conversion gain and intermodulation distortion at input level will vary when you improve VS of RF input with external circuit (50 Ω termination or impedance matching.)

PACKAGE DIMENSIONS

6 pin super minimold (Unit: mm)



NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.g. 1 000 pF) to the Vcc pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

μPC2756TB

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit[Note]: None	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit[Note]: None	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit[Note]: None	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit[Note]: None	–

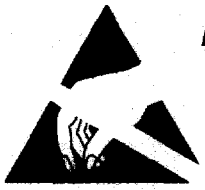
Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]



ATTENTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

M4 96.5