



# DC to 6 GHz, 45 dB Envelope Threshold Detector

Preliminary Technical Data

## ADL5910

### FEATURES

- Broad Input Frequency Range: DC to 6 GHz
- RF Input Range: 45 dB (-30 dBm to +15 dBm)
- Input Envelope Threshold Detection and Latching
- Programmable Threshold and Latch Reset Function
- Fast Response Time: 20 ns from RFIN to Latch
- All functions temperature and supply stable
- Operates at 3 V and 5 V from -55°C to +125°C
- Low power: 2.5 mA at 3.0 V supply
- Power-down capability to <100  $\mu$ A
- 16-pin, 3mm x 3mm LFCSP package

### APPLICATIONS

- Transmitter Signal Strength Indication (TSSI)
- Wireless Power Amplifier Input and Output Protection
- Wireless Receiver Input Protection

### GENERAL DESCRIPTION

The ADL5910 is an envelope threshold detector that operates from DC to 6 GHz. The RF input signal drives an internal envelope detector. The output voltage from this envelope detector drives a comparator which is also driven by a user-defined input voltage. When the voltage from the envelope detector exceeds the user-defined threshold voltage, the event is latched to an S-R flip flop. The response time from the RF input signal exceeding the user-programmed threshold voltage to the output latching is 20 ns. The latched event is held on the flip-flop until a reset pulse is applied.

### FUNCTIONAL BLOCK DIAGRAM

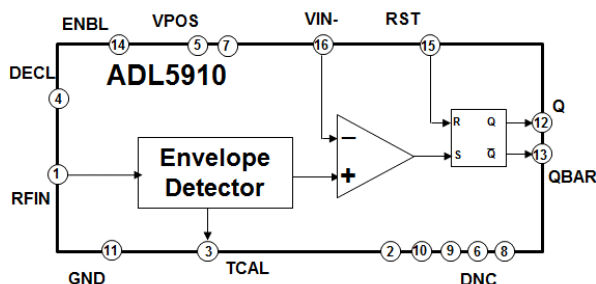


Figure 1. ADL5910 Block Diagram

The RF Input of ADL5910 is dc-coupled, allowing for operation down to arbitrarily low input frequencies. It operates on either a 3V or 5V supply and consumes 2.5 mA. A disable mode reduces this current to 100  $\mu$ A when a logic low is applied to the ENBL pin.

The ADL5910 is supplied in a 3 mm  $\times$  3 mm, 16-lead LFCSP for operation over the wide temperature range of -55°C to +125°C.

#### PrE

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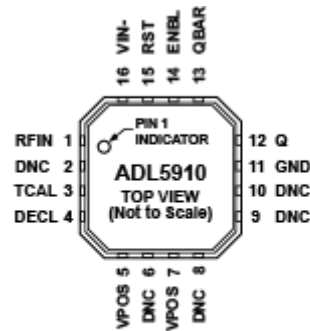
## SPECIFICATIONS

 $V_{POS} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $Z_O = 50\ \Omega$ ,  $C_{RMS} = 0.1\ \mu\text{F}$ .

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range			DC to 6000		MHz
RF INPUT INTERFACE	Pin RFIN				
Nominal Input Impedance	Single-ended drive, External shunt matching resistor		50		$\Omega$
THRESHOLD DETECT and LATCH	Pin Q, QBAR, VIN-, RST				
Peak Envelope Power, Threshold Detection Range	PEP(dBm)= $P_{RMS}(\text{dBm}) + \text{Pk-to-Average Ratio}(\text{dB})$		-30 to +15		dBm
Output Response Time	Transition time from RFIN exceeding VIN-threshold to Q and Qbar settled (VIN- = TBD V, Threshold overdrive = TBD dB, $P_{IN} = -\text{TBD dBm}$ )		20		ns
Reset Time	Transition time from RST high to Q and Qbar settled		TBD		ns
Q, Qbar Source/Sink Current			TBD/TBD		mA
COMPARATOR INTERFACE	Pin VIN-				
VIN- Input Range			0 to 2		V
VIN- Input Bias Current			TBD		$\mu\text{A}$
FLIP FLOP RESET INTERFACE	Pin RST				
Logic High Level		TBD		VPOS	V
Logic Low Level		0		TBD	V
Input Bias Current			TBD		
POWER-UP INTERFACE	Pin ENBL				
Voltage Level to Enable		TBD		VPOS	V
Voltage Level to Disable		0		TBD	V
Input Bias Current			TBD		
POWER SUPPLY INTERFACE	Pin VPOS				
Supply Voltage		3.0		5.0	V
Quiescent Current	$T_A = 25^\circ\text{C}$ , No signal at RFIN, VPOS=5V		3		mA
	$T_A = 25^\circ\text{C}$ , No signal at RFIN, VPOS=3V		3		mA
	$T_A = 125^\circ\text{C}$ , No signal at RFIN, VPOS =5V		TBD		mA
Power-Down Current	ENBL = LOW, VPOS = 3V		100		$\mu\text{A}$
	ENBL = LOW, VPOS = 5V		100		$\mu\text{A}$

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. EXPOSED PADDLE. CONNECT TO A LOW IMPEDANCE THERMAL AND ELECTRICAL GROUND PLANE.

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	Signal Input. This pin is internally ac-coupled on pre-release engineering samples and has a nominal input impedance of 50 Ohms. The mass-production version of ADL5910 will be dc-coupled and will require an external ac-coupling capacitor and external shunt resistor for 50 ohm operation.
2,6,8,9,10	DNC	No Connect.
3	TCAL	Threshold calibration. The voltage on this pin is used to determine the correct threshold voltage that should be applied to Pin 16 (VIN-) to set a particular RF power threshold. This is a two-step process. First measure the output voltage on TCAL with no RF signal applied to RFIN (this voltage will be approximately 750 mV). Next apply the RF input power to RFIN which should cause the circuit to trip and again measure the voltage on the TCAL pin. The difference between these two voltages is equal to the voltage that should be applied to VIN- during operation.
4	DECL	Internal Decoupling. Bypass this pin to ground using a 4 Ohm resistor connected in series with a 100 nF capacitor.
5,7	VPOS	Supply Voltage range is 3V to 5V. Decoupling capacitors should be placed on Pin 5. There is no requirement for power supply decoupling capacitors on Pin 7
11	GND	Device Ground. Connect GND pin to system ground using a low impedance path.
12,13	Q, Qbar	Differential digital outputs of threshold detect flip flop. Q latches high when the output of the internal envelope detector exceeds the threshold voltage on the internal comparator's VIN- input.
14	ENBL	Device Enable. Connect the ENBL pin to logic high to enable the device.
15	RST	Flip flop reset. Taking RST high clears the latched flip flop output, setting outputs Q and Qbar to low and high respectively.
16	VIN-	Inverting input to threshold detect comparator. The voltage on this pin is compared to the output voltage of the internal envelope detector which is driven by the RF input level. If the output voltage of the envelope detector exceeds the voltage on VIN-, the flip flop will latch the Q output to high and the Qbar output to low.
	EPAD	Exposed Pad. The exposed pad should have good thermal and electrical connection to the pcb ground plane.

## EVALUATION BOARD

The ADL5910-EVALZ is a fully populated, 4-layer, FR4-based evaluation board. A power supply of either 3V or 5V should be applied to the VPOS and GND test loops. To operate the Threshold Detect circuitry, the RF signal that is being monitored should be applied to the RFIN SMA connector. The dc threshold voltage that should cause the circuit to trip should

be applied to the VIN\_N SMA connector or to the TPVIN\_N yellow test point. The internal S/R flip-flop should be reset by pressing the RST button.

Detailed configuration options for the evaluation board are listed in Table 3.

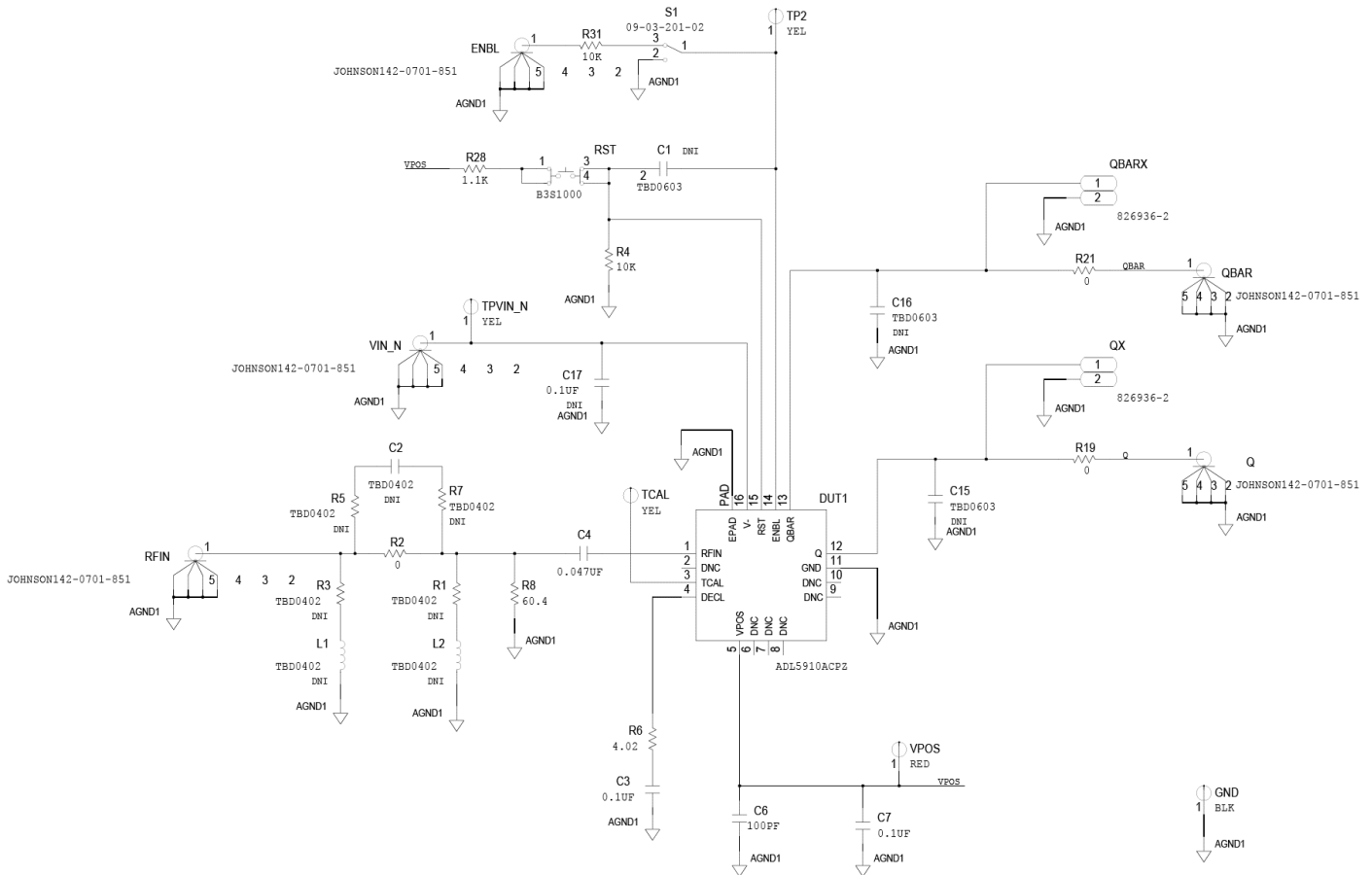


Figure 2. Evaluation Board Schematic

Table 3. Evaluation Board Configuration Options

Component	Function/Notes	Default Value
RFIN, R1, R2, R3, R5, R7, R8, L1, L2, C2, C4	<b>RF Input:</b> The RF input signal to the ADL5910 should be applied to the SMA connector labelled RFIN. The ADL5910's RFIN pin (Pin 1) is dc-coupled and is not internally matched. A broadband 50 ohm match is achieved using an external 82.5 ohm shunt resistor with a 0.47uF ac-coupling capacitor placed between the shunt resistor and the RF input. An external pre-emphasis network can be built to improve flatness vs frequency using the components between R8 and the RFIN SMA connector.	C4= 0.47uF (0402) R8 = 82.5 $\Omega$ (0402) R2 = 0 $\Omega$ (0402) R1,R3,R5,R7 = open (0402) L1,L2 = open (0402) C2 = open (0402)
TCAL, VIN_N, TPVIN_N, C17,	<b>TCAL:</b> The output voltage from the Threshold Calibration pin (TCAL, Pin 3) is available on the yellow TCAL clip lead. The voltage on this pin is used to determine the correct threshold voltage that should be applied to Pin 16 (VIN-) to set a particular RF power threshold. This is a two-step process. First measure the output voltage on the TCAL yellow clip lead with no RF signal applied to RFIN (this voltage will be approximately 750 mV). Next apply the RF input power to RFIN which should cause the circuit to trip and again measure the voltage on the TCAL yellow clip lead. The difference between these two voltages is equal to the voltage that should be applied to VIN- during operation. This voltage can be either applied to the VIN_N SMA connector or to the TPVIN_N yellow clip lead. C17 can be used to provide noise decoupling of the applied input voltage.	C17 = open (0603)
R6, C3	<b>DECL Internal Decoupling Node:</b> A resistor in series with a capacitor to ground should be connected to the ADL5910's DECL pin (Pin 4).	C3 = 100 nF (0402) R6 = 4.02 $\Omega$ ,
VPOS, GND, C7, C6	<b>Power Supply Interface:</b> Apply the power supply for the evaluation board to the VPOS (red) and GND (black) test loops. The nominal supply decoupling consists of a 100 pF capacitor and a 0.1 $\mu$ F capacitor, with the 100pF capacitor placed closest to the VPOS pin (pin 5).	C7 = 0.1 $\mu$ F (0402), C6 = 100 pF (0402)
Q, QBAR, QX, QBARX, R19, R21 C15, C16	<b>Threshold Detect Output (Q and Qbar):</b> The threshold detect flip-flop outputs (Q and Qbar) are available on the SMA connectors labelled Q and QBAR and on the 2-pin headers labelled QX and QBARX. To test the response time of Q and QBAR, remove R19 and R21 and probe QX and QBARX with low capacitance FET probes.	C15 = C16 = open (0603) R19, R21 = 0 $\Omega$ (0603)
ENBL, S1, R31	<b>Enable Interface:</b> The ADL5910 can be enabled by applying 3-5V to the ENBL SMA connector or using the S1 switch. The enable voltage should equal to but not greater than the supply voltage (3V to 5V).	R31 = 10 K $\Omega$ (0603)
RST push-button Switch R4, C1, R28	<b>Threshold Detect Reset:</b> The Threshold Detect flip-flop is reset using the RST push-button switch. The RST switch is connected the VPOS supply voltage through a 1.1K resistor (R28). A 100K pull-down resistor (R4) is connected to the ADL5910's RST pin. This pulls RST low in the absence of any other stimulus. The ADL5910 will normally power up with the Q and QBAR outputs high and low respectively. A reset-on-power-up circuit can be implemented by installing a capacitor on C1. When the VPOS supply is turned on, this will cause RST to go high momentarily before being pulled low by R4.	R4 = 10 K $\Omega$ (0603) R28 = 1.1 K $\Omega$ (0603) C1 = open (0603)
VIN_N, TPVIN_N, C17	<b>Threshold Detect Level Set:</b> The voltage applied to the VIN_N SMA connector or to the TPVIN_N yellow test loop drives the inverting input of the threshold detect comparator (VIN-) and thereby defines the RF power level that will trip the threshold detect comparator and flip-flop. The threshold detect voltage can be optionally decoupled using C17.	C17 = open (0603)

Figure 1 is a mechanical drawing of the package showing top, bottom, and side views with dimensions.

**Top View:**

- Overall width: 3.10
- Overall height: 3.00 SQ
- Pin 1 Indicator: Located in the top-left corner.
- Internal dimensions: 2.90 (width of the main body), 0.30 (width of the top-left corner), 0.23 (width of the top-right corner), and 0.18 (width of the bottom-right corner).

**Bottom View:**

- Overall width: 3.10
- Overall height: 3.00 SQ
- Pin 1 Indicator: Located in the top-right corner.
- Exposed Pad: Located in the center.
- Dimensions: 0.50 BSC (Bottom Surface Contour), 1.75 (width of the exposed pad), 1.60 SQ (width of the exposed pad), 1.45 (width of the exposed pad), 0.25 MIN (minimum distance from the exposed pad to the edge), 0.50 (width of the top-left corner), 0.40 (width of the top-right corner), and 0.30 (width of the bottom-right corner).

**Side View:**

- Overall height: 0.80
- Seating Plane: Indicated by a horizontal line.
- Dimensions: 0.75 (height of the package), 0.70 (height of the package), 0.05 MAX (maximum coplanarity), 0.02 NOM (nominal coplanarity), 0.08 (coplanarity), and 0.20 REF (reference dimension).

**16-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]**  
**3 x 3 mm Body, Very Very Thin Quad**  
**(CP-16-22)**  
**Dimensions shown in millimeters**

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