RFMD + TriQuint = Qorvo

RFFM8506

4.9 GHz to 5.85 GHz 802.11a/n/ac WiFi Front End Module

Package: QFN, 16-pin,
2.5 mm x 2.5 mm x 0.45 mm

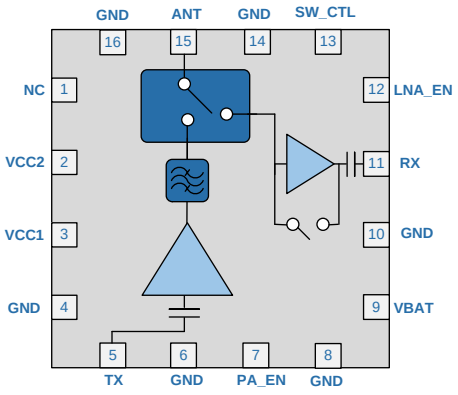
The RFFM8506 provides a complete integrated solution in a single front end module (FEM) for WiFi 802.11a/n/ac systems. The ultra-small factor and integrated matching minimizes layout area in the customer's application and greatly reduces the number of external components. This simplifies the total front end solution by reducing the bill of materials, system footprint, and manufacturing cost. The RFFM8506 integrates a 5 GHz power amplifier (PA), single pole double throw switch (SP2T) and an LNA with bypass. The device is provided in a 2.5 mm x 2.5 mm x 0.45 mm, 16-pin QFN package. This module meets or exceeds the RF front end needs of IEEE 802.11a/n/ac WiFi RF systems.

Features

- P_{OUT}=+17.5 dBm, 11ac, 80 MHz MCS9 at −36.5dB (1.5%) EVM
- Small Size
- High performance FEM
- Input and Output Matched to 50 Ω
- Integrated 5 GHz PA, SP2T, Switch, and LNA (with Bypass if required)
- Low Height Package, Suited for SiP and CoB designs

Applications

- Cellular Handsets
- Mobile Devices
- Tablets
- Consumer Electronics
- Gaming
- Netbooks/Notebooks
- TV/Monitors/Video



Functional Block Diagram

Ordering Information

RFFM8506SB	Standard 5-piece sample bag
RFFM8506SQ	Standard 25-piece sample bag
RFFM8506SR	Standard 100-pieces reel
RFFM8506TR7	Standard 2500-piece reel
RFFM8506PCK-410	Fully assembled eval board w/ 5-piece sample bag

Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	−0.5 to +5.4	V_{DC}
PA Enable Voltage	−0.5 to 5	V_{DC}
DC Supply Current	500	mA
Storage Temperature	−40 to +150	°C
Maximum TX Input Power into 50Ω Load for 11a/n/ac (No Damage)	+12	dBm
Moisture Sensitivity	MSL1	

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Compliance					**802.11a, 802.11n, 802.11ac**
Operating Frequency	5.15		5.85	GHz	
Extended Frequency	4.9		5.15	GHz	Functional with reduced performance
Operating Temperature	−30		+85	°C	
Power Supply V_{CC} (V_{CC1}, V_{CC2}, V_{BAT})	3.0	3.6	4.2	V	
Switch Control Voltage – SW_CTL High	2.75	2.9	4.2	V	TX switch “ON” at high control voltage
Switch Control Voltage – SW_CTL Low		0.1	0.4	V	RX switch “ON” with low control voltage
PA Enable – High	2.75	2.9	4.2	V	PA in “ON” state
PA Enable voltage – Low		0.1	0.4	V	PA in “OFF” state, do not leave floating
Transmit (TX-ANT) Mode					**T= +25 °C; V_{CC}=+3.6 V; PA_EN=High; SW_CTL=High; LNA_EN=Low; Unless otherwise noted**
Gain (5.15 to 5.85 GHz)	25.5	29		dB	
20 MHz Output Power*	18.5	19		dBm	802.11ac HT20 MCS7
11ac 20 MHz Dynamic EVM		−33	−30	dB	
		2.2	3.2	%	
40 MHz Output Power*	17.5	18		dBm	802.11ac VHT40 MCS9
11ac 40 MHz Dynamic EVM		−36.5	−35.0	dB	
		1.5	1.8	%	
80 MHz Output Power*	16.5	17		dBm	802.11ac VHT80 MCS9
11ac 80 MHz Dynamic EVM		−36.5	−35.0	dB	
		1.5	1.8	%	
80 MHz Output Power*		13.5		dBm	802.11ac VHT80 MCS9
11ac 80 MHz Dynamic EVM		−40		dB	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
		1.0		%	
Spectral Mask 20 MHz Output Power*		22		dBm	802.11ac HT20 with 3dB margin
Spectral Mask 40 MHz Output Power*		21		dBm	802.11ac VHT40 with 3dB margin
Spectral Mask 80 MHz Output Power*		20		dBm	802.11ac VHT80 with 3dB margin
Operating Current - Nominal		270	330	mA	P_{OUT} = +19 dBm
Transmit (TX-ANT) Mode (continued)					**T= +25 °C; V_{CC}=+3.6 V; PA_EN=High; SW_CTL=High; LNA_EN=Low; Unless otherwise noted**
Second Harmonic			−40	dBm/MHz	Fundamental frequency is between 4900 and 5850 MHz; RF P_{OUT} = +19 dBm; Measured in 1 MHz resolution bandwidth (FCC limit max = −30 dBm)
Third Harmonic			−38	dBm/MHz	
PA Selectivity/Out of Band Gain					
30 to 2900 MHz		−6		dB	
3600 to 4400 MHz		20		dB	
7250 to 7750 MHz		16		dB	
TX Port Return Loss	10	12		dB	
ANT Port Return Loss	12	15		dB	
Noise Figure			6	dB	
Receive (ANT-RX) LNA On					**T= +25 °C; V_{CC}=+3.6 V; PA_EN=Low; SW_CTL=Low; LNA_EN=High; Unless otherwise noted**
Gain	10	12		dB	
Noise Figure		2.5		dB	
Rx Port Return Loss	8	10		dB	
ANT Port Return Loss	8	10		dB	
Input IP2		50		dBm	
Input IP3	5	6		dBm	
Current Consumption		12		mA	
LNA_EN Control Current		75	120	µA	
LNA Turn On Time			300	nS	
Receive (ANT-RX) Bypass Mode					**T = +25 °C; V_{CC}=+3.6 V; PA_EN=Low; SW_CTL=Low; LNA_EN=Low; Unless otherwise noted**
Insertion Loss		3.5		dB	
Noise Figure		3.5		dB	
RX Port Return Loss	8	10		dB	
ANT Port Return Loss	8	10		dB	
ANT-RX Isolation	26			dB	Transmit Mode; PA_EN=High; Maximum Power
Input IP3	18	20		dBm	
LNA Bypass Current		15		µA	
General Specifications					

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Switch Control Current – High			2	µA	
Switch Control Current – Low			0.1	µA	Do not leave floating
PA_EN Current		30		µA	
Leakage Current – Nominal		2	15	µA	RF Off; PA_EN=Low; SW_CTL=Low, LNA_EN=Low
Switching Speed			200	nS	
PA Turn-On Time from PA_EN edge			300	nS	Output stable within 90 % of final gain
PA Turn-Off Time from PA_EN edge			300	nS	Output stable within 90% of final gain
ESD – Human Body Model	1000			V	EIA/JESD22-114A all pins
ESD – Charge Device Model	1000			V	EIA/JESD22-101C all pins
Ruggedness			10:1	VSWR	With nominal input power

*For 4900 MHz to 5150 MHz, P_{OUT} is reduced by 1dB

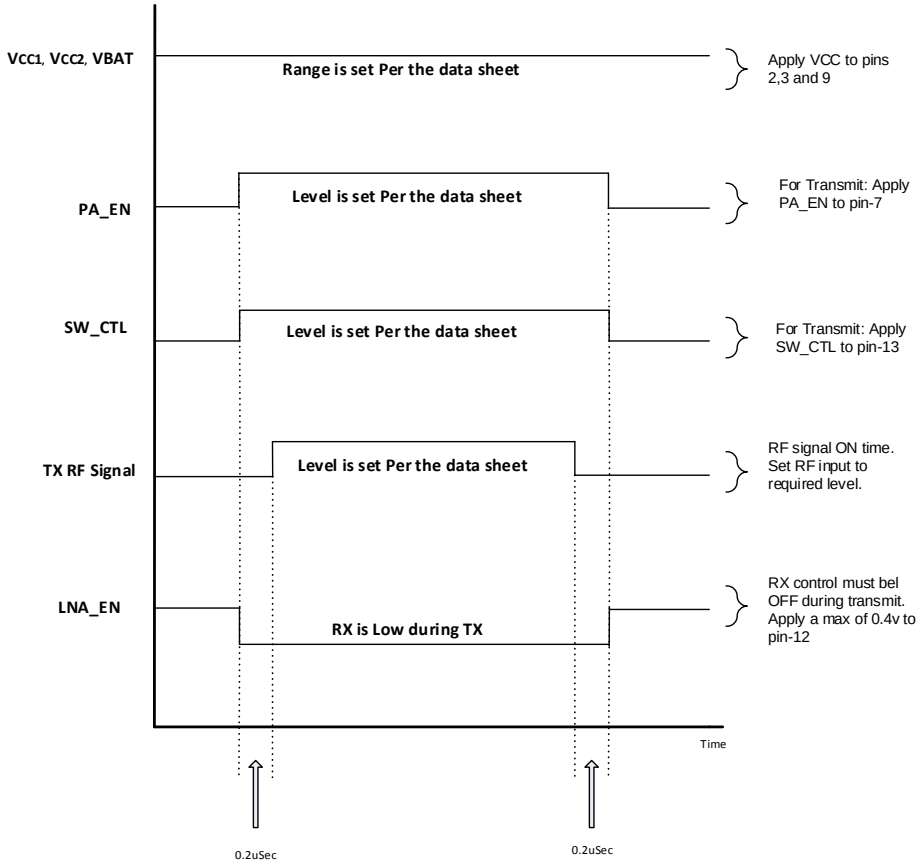
Switch Control Logic Truth Table

Operating Mode	PA_EN	SW_CTL	LNA_EN
802.11a/n/ac TX	High	High	Low
802.11a/n/ac RX Gain	Low	Low	High
802.11a/n/ac RX Bypass	Low	Low	Low

Note: All Logic Low pins ≤ 0.4V

Timing Diagram

Transmit Timing Diagram
Power ON / OFF Sequence



Note:
1. RF Signal for each specific mode is applied after the DC bias is applied.
2. Total ON/OFF time includes from 10% of control switching to 90% of RF power.
3. Listed values on diagram are typical. Tx/Rx simultaneous transition is allowed.
4. For DC voltage levels use the values indicated in the datasheet.

Timing Sequence Notes

802.11a/n/ac Transmit Biasing Instructions

1. Connect the FEM to a signal generator at the input and a spectrum analyzer at the output. Terminate unused ports with 50 Ohms
2. Set the power supply voltage to +3.0 V to +4.2 V first with PA_EN < 0.4 V. Leakage current will be <15 uA typical.
3. Refer to switch operational truth table to set the control lines at the proper levels for WiFi TX. All OFF voltages must be < 0.4 V (do not leave floating.)
4. Turn on PA_EN with levels indicated in the datasheet. PA_EN controls the current drawn by the 802.11a/n/ac power amplifier and the current should quickly rise to ~200 mA +/- 20 mA for a typical part but the actual operating current will be based on the output power desired. Be extremely careful not to exceed 5.0 V on the PA_EN pin or the part may exceed device current limits.

802.11a/n/ac Transmit Turn ON Sequence (See Transmit Timing Diagram)

1. Turn ON power supply.
2. Turn ON PA_EN.
3. Turn ON SW_CLT
4. Apply RF.

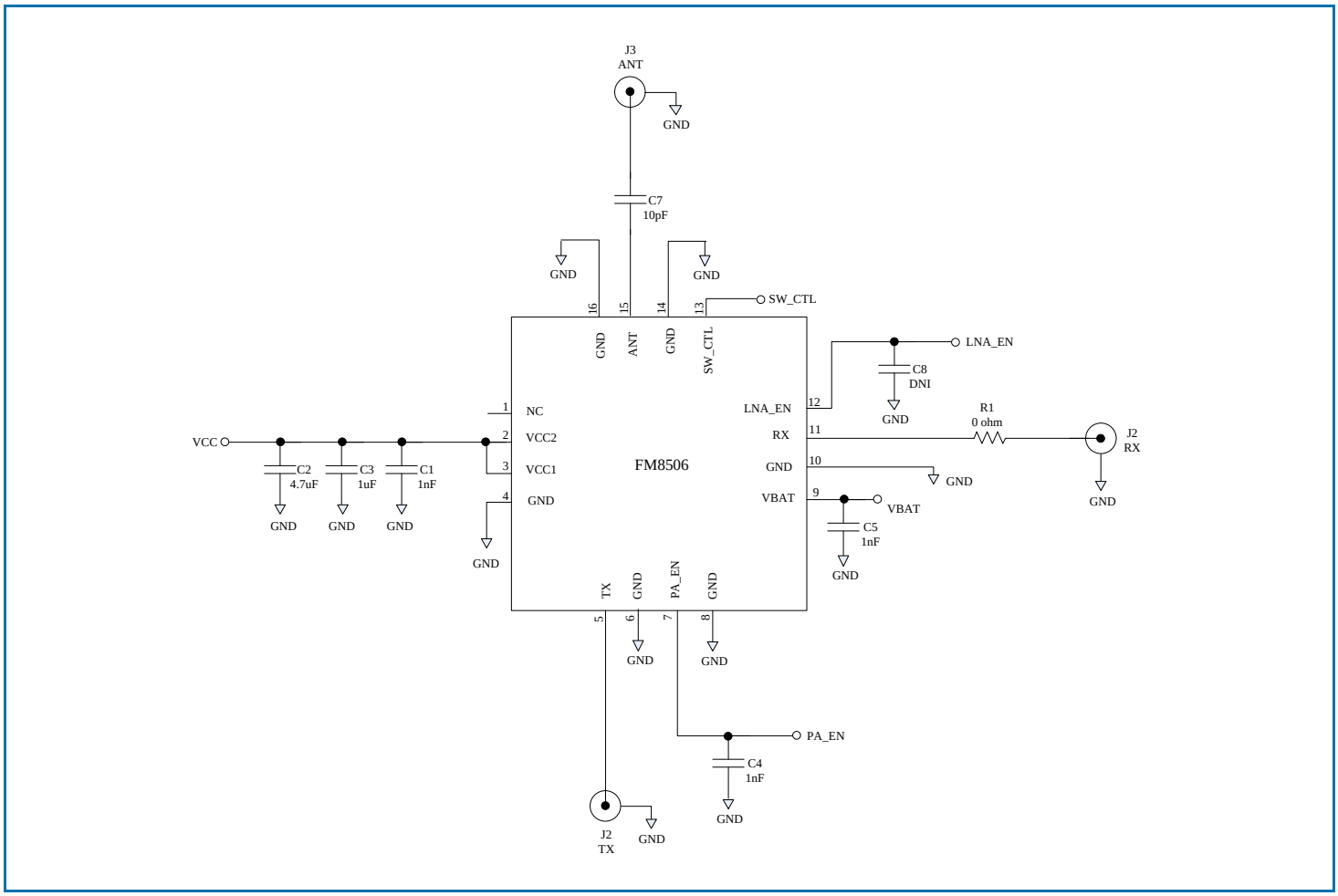
802.11a/n/ac Transmit Turn OFF Sequence

1. Turn OFF RF.
2. Turn OFF SW_CLT
3. Turn OFF PA_EN.
4. Turn OFF power supply.

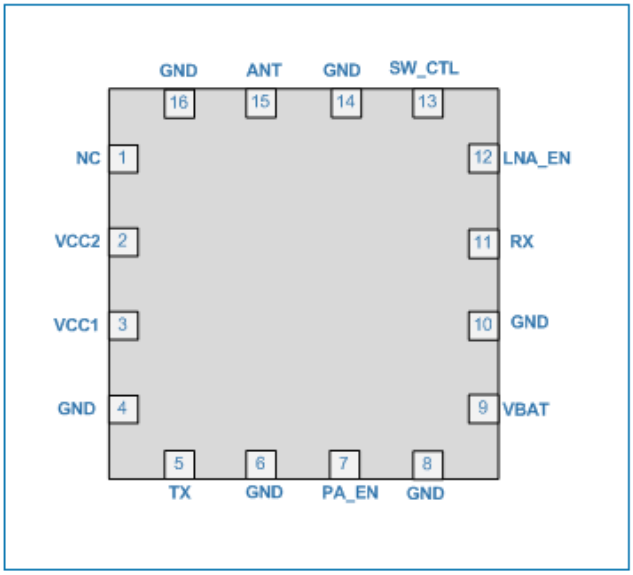
802.11a/n/ac Receive

1. To receive WiFi set the switch control lines per the truth table.
2. Antenna port is input and RX port is output for this test.
3. Follow Timing Diagram for biasing instructions.

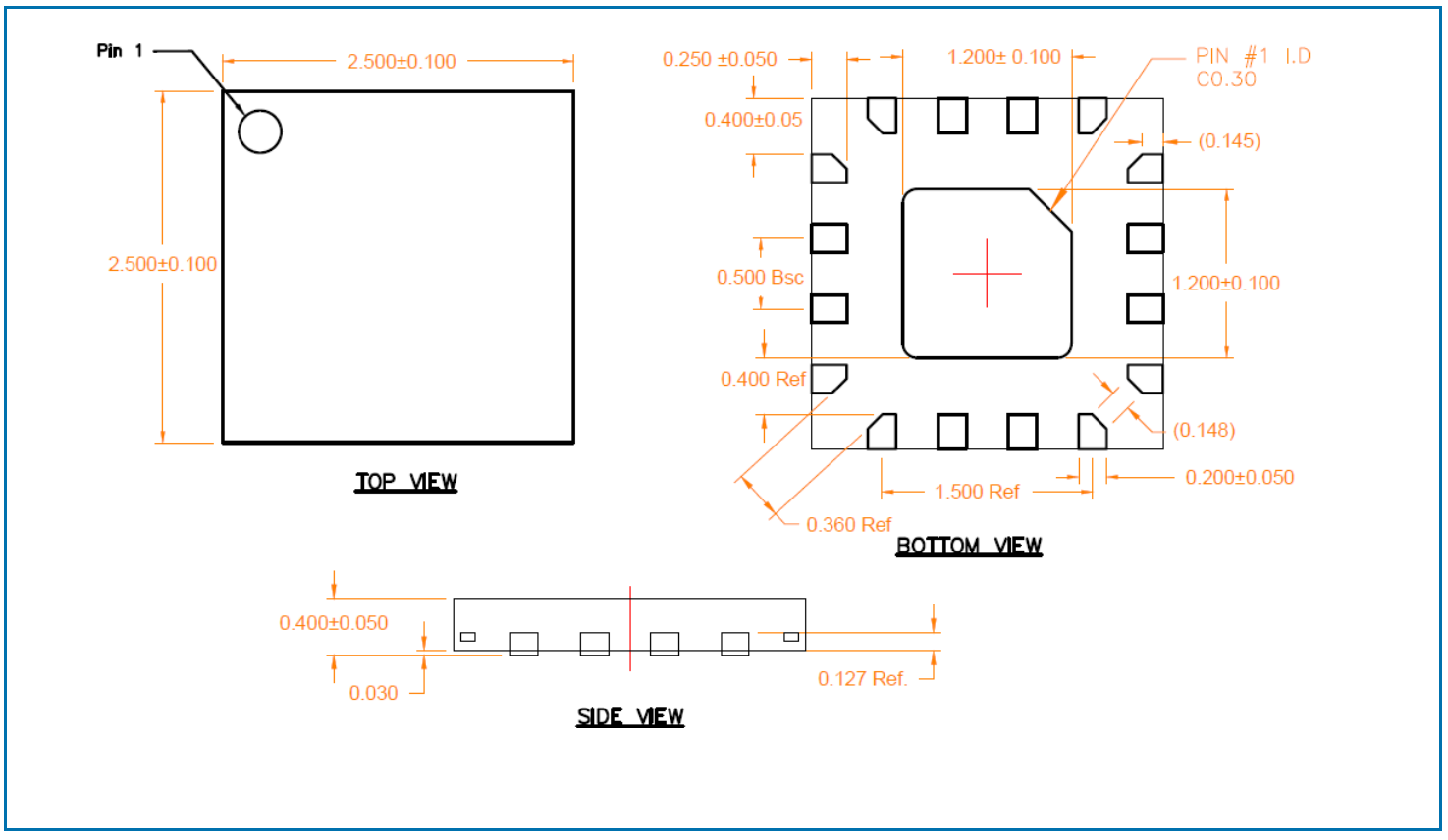
Evaluation Board Schematic



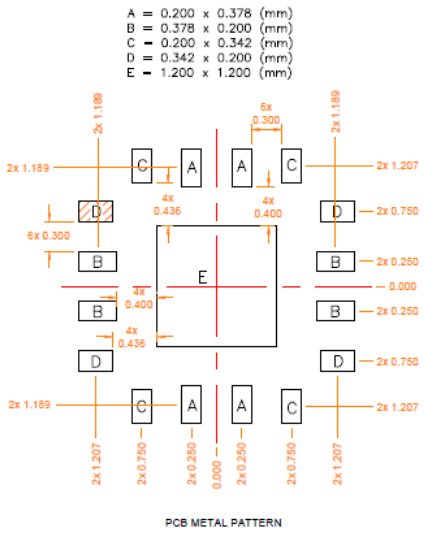
Pin Out

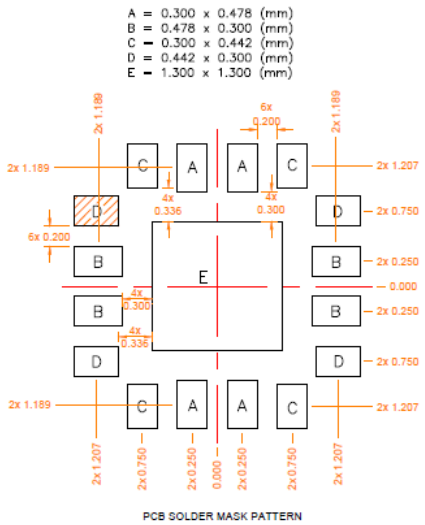


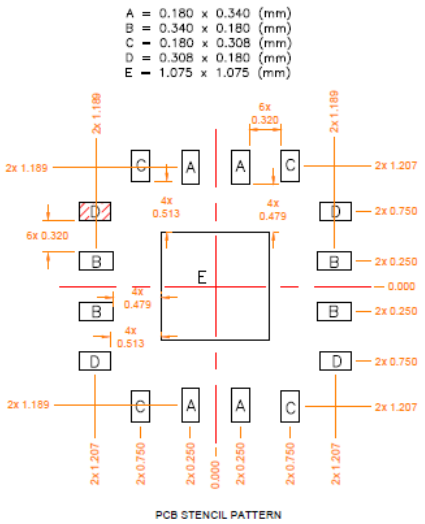
Package Outline and Branding Drawing (Dimension in millimeters)



PCB Patterns







Thermal vias for center slug "E" should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout.

Note: Shaded area represents Pin 1 location

Pin Names and Descriptions

Pin	Name	Description
1	NC	This pin is not connected internally and can be left floating but is recommended to connect to ground.
2	VCC2	Supply voltage for the PA. See applications schematic for biasing and bypassing components.
3	VCC1	Supply voltage for the PA. See applications schematic for biasing and bypassing components.
4	GND	Ground Connection. This pin is not connected internally and can be left floating or connected to ground.
5	TX	RF input port for the 802.11a/n/ac PA. Input is matched to 50Ω and DC blocked internally
6	GND	Ground Connection. This pin is not connected internally and can be left floating or connected to ground.
7	PA_EN	Control voltage for the PA. See “Switch Control Truth Table” for proper settings.
8	GND	No Connect. This pin is not connected internally and can be left floating or connected to ground.
9	VBAT	Supply voltage for the LNA, Switch & Bias Regulator. See applications schematic for biasing and bypassing components.
10	GND	Ground Connection. This pin is not connected internally and can be left floating or connected to ground.
11	RX	RF output port for the 802.11a/n/ac LNA. This port is matched to 50Ω and DC blocked internally.
12	LNA_EN	Control voltage for the LNA. When this pin is set to a LOW logic state, the bypass mode is enabled.
13	SW_CTL	Switch control voltage. High control voltage turns ON the TX path and low control voltage turns on the RX path (see “Switch Control Truth Table”)
14	GND	Ground Connection. This pin is not connected internally and can be left floating or connected to ground.
15	ANT	RF bidirectional antenna port matched to 50Ω.
16	GND	Ground Connection. This pin is not connected internally and can be left floating or connected to ground.
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., PCB vias under the device are recommended.