Rad-Hard Solid State SPST Latching Relay

Manufactured in a Certified Class-K Facility

Features

- 100 V Breakdown Voltage (N.O. contact)
- 1 Amp Design
- Neutron Fluence Level >1.8E12 n/cm^2
- Optically Coupled
- Total Dose Capability >100 Krad (Si)
- >1,000 VDC Input to Output Isolation
- Buffered Input Stage
- 3.3 V Compatible Logic Level Input
- AC version available (higher "on" resistance)

Description

The AP10N01L is a radiation hardened SPST normally open solid-state latching relay in a hermetic package. It is configured as one contact which is open in the "reset state," and closed in the "set" state. This device is characterized for >100 Krad (Si) total ionizing dose, and neutron fluence level of >1.8E12 n/cm^2. The output FETs utilize advanced technology, and the device is actuated by standard inputs (i.e. 3.3 V and higher logic levels).

Table 1 – Absolute Maximum Ratings (Tc = +25°C Unless Otherwise Noted)

(Exceeding maximum ratings may damage the device.)

Symbol	Parameters / Test Conditions (Notes Page 3)	Value	Unit
V_S	Output N.O. Switch Voltage (5)	100	V
I_O	Output N.O. Switch Current (4) (5)	1	A
V_S	Output N.C. Switch Voltage (5)	N/A	V
I_O	Output N.C. Switch Current (4) (5)	N/A	A
$V_{set\ or\ reset}$	Input Actuation Voltage (Pin 1 & 3) (3)	48	V
$V_{set\ or\ reset}$	Input Actuation Current	2.5	mA
V_R	Input Supply Voltage (Pin 6) (7)	40	V
I_R	Input Supply Current (7)	12	mA
P_{DISS}	Power Dissipation (4) (5)	2.5	W
T_J	Operating Temperature Range	-55 to +125	°C
T_S	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature	300	°C

Table 2 – General Characteristics per Channel @ -55°C < TC < +125°C

(Unless Otherwise Specified)

Parameter	Group A Subgroups	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Input Latch Threshold Voltage (1) (3)	--	V_R = 12 V, I_O = 1 A	$V_{IN(TH)}$	-	--	2.5	V
Input-to-Output Leakage Current (1)	--	V_{I-O} = 1.0KVdc, dwell = 5.0s T_C = 25°C	I_{I-O}	--	--	1.0	mA
Output Capacitance (1)	--	V_{IN} = 0.1V, f = 1.0MHz, V_S = 25V, T_C = 25°C	C_{OSS}	--	110	--	pF
Thermal Resistance (1)	--	V_{IN} = 3.3V, V_{DD} = 5.0V (1, 4)	R_{THJC}	--	--	20	°C/W
MTBF (Per Channel)	--	MIL-HDBK-217F, SF@Tc= 25°C		6.0	--	--	MHrs
Weight	--	--	W	--	--	25	grams

Table 3 – Pre-Irradiation Electrical Characteristics per Channel

@ -55°C < TC < +125°C (Unless Otherwise Specified)

Parameter	Group A Subgroups	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Output On-Resistance	1	V_R = 12 V I_O= 1A	$R_{DS(ON)}$	--	--	0.8	Ohms
	2			--	--	1.6	
Output Leakage Current N.O. output	1	V_S = 100V	I_O	--	--	25	uA
	2	V_S = 80V		--	--	250	
Input Supply Current	1, 2, 3	V_R = 12.0V	I_{DD}	--	6	15	mA
				--	--		
Input Set/Reset Current	1	V_{in} = 10V	I_{IN}	--	--	1.0	mA
	2, 3			--	--	1.5	
Turn-On Delay (6)	1, 2, 3	V_{IN} = 3.3V, V_R = 12V, V_S = 50V R_L = 5Ω, P.W. = 50ms	ton	--	--	TBD	mS
Turn-Off Delay (6)	1, 2, 3	V_{IN} = 0.1V, V_R = 12V, V_S = 50V R_L = 5Ω, P.W. = 50ms	toff	--	--	TBD	
Rise Time (2) (6)	1, 2, 3	V_{IN} = 3.3V, V_R = 12V, V_S = 50V R_L = 5Ω, P.W. = 50ms	tr	--	--	TBD	
Fall Time (2) (6)	1, 2, 3	V_{IN} = 0.1V, V_{DD} = 12V, V_S = 50V R_L = 5Ω, P.W. = 50ms	tf	--	--	TBD	

Table 4 – Post Total Dose Irradiation [8, 9]
Electrical Characteristics per Channel @ 25°C (unless otherwise specified)

Parameter	Group A Subgroups	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Output On-Resistance	1	V_R = 12 V, I_O= 1 A	$R_{DS(ON)}$			1	Ohms
Input Supply Current	1	V_R= 12V	I_{DD}		10	15	mA
Output Leakage Current	1	V_R = 0.1V, V_S = 100V	I_O			25	mA
Input Set/Reset Current	1	V_{IN} = 10V	I_{IN}			1.2	
Turn-On Delay [6]	1	V_{IN} = 3.3V, V_{DD} = 5.0V, V_S = 50V R_L = 5W, P_W = 50ms	ton			TBD	ms
Turn-Off Delay [6]	1	V_{IN} = 0.1V, V_{DD} = 5.0V, V_S = 50V R_L = 5W, P_W = 50ms	toff			TBD	
Rise Time [2] [6]	1	V_{IN} = 3.3V, V_{DD} = 5.0V, V_S = 50V R_L = 5W, P.W. = 50ms	tr			TBD	
Fall Time [2] [6]	1	V_{IN} = 0.1V, V_{DD} = 5.0V, V_S = 50V R_L = 5W, P.W. = 50ms	tf			TBD	

Notes for Maximum Ratings and Electrical Characteristic Tables

1. Specification is guaranteed by design.
2. Rise and fall times are controlled internally.
3. Set and Reset inputs protected for V_{IN} > -10 V to < +48 V.
4. Optically coupled Solid State Relays (in reality a FET with isolated Gate drive) have relatively slow turn on and turn off times. Care must be taken to insure that transient currents during these times do not cause violation of SOA limits for the particular switch used. If transient conditions are present, we recommend that a complete simulation be performed by the end user to insure compliance with SOA requirements as specified in the data sheet of the applicable switching transistor.
5. While the SSR design meets the design requirements specified in MIL-PRF-38534, the end user is responsible for product derating, as required for the application.
6. Reference Figures 3 & 4 for Switching Test Circuits and Waveform; Output Voltage (V_O) of Figure 4, Switching Test Waveform, is representative of the Output FET Drain-to-Source Voltage.
7. Input Supply voltage shall not exceed 40 V.
8. Total Dose Irradiation takes place with an Input Voltage of 24 V applied and V_{DS} = 80 V.
9. API Technologies' Marlborough Operations does not currently have a DLA certified Radiation Hardness Assurance Program.

Radiation Performance

API's Radiation Hardened Solid State Relays are tested to verify their hardness capability. The hardness assurance program uses a Cobalt-60 (60 Co) Source and heavy ion irradiation. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions to provide a direct comparison.

Table 5 - Ordering Information

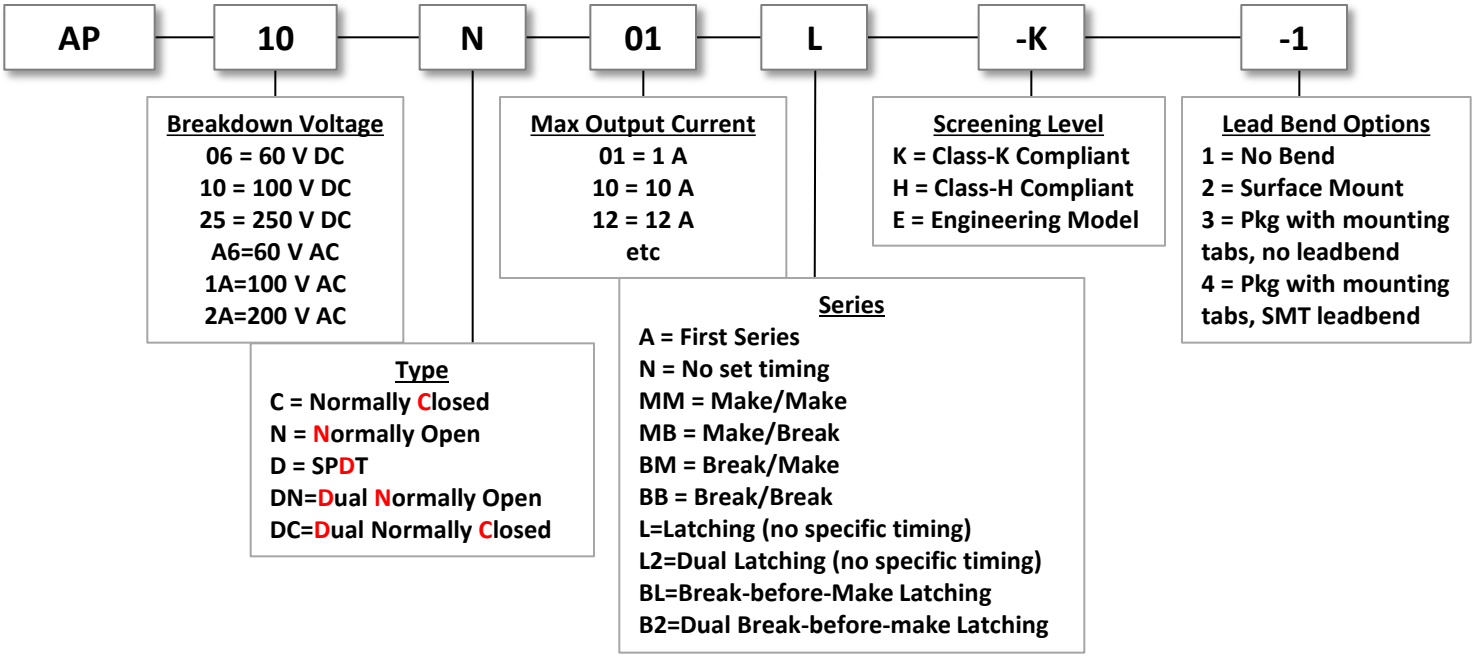

Table 6 - Screening Options

Tests	Screening Levels		Mil-Std-883-Method
	H	K	
	Compliant- MIL-PRF-38534		
100 % Non-Destruct Wire-Pull	Sample	100%	2023
Pre-Cap Visual	N/A	100%	2017
Temperature Cycle	100%	100%	1010
Constant Acceleration	100%	100%	2001
PIND	N/A	100%	2020
Pre-Burn-In Electrical (Ta= 25C)	100%	100%	
Burn-In	100% (240 Hours)	100% (320 Hours)	1015
Final Electrical	100%	100%	(6)
Hermeticity (Fine & Gross Leak)	100%	100%	1014
X-Ray [5]	N/A	100%	2012
External Visual	100%	100%	2009

Figure 1 – Maximum Drain Current vs. Case Temperature per Channel

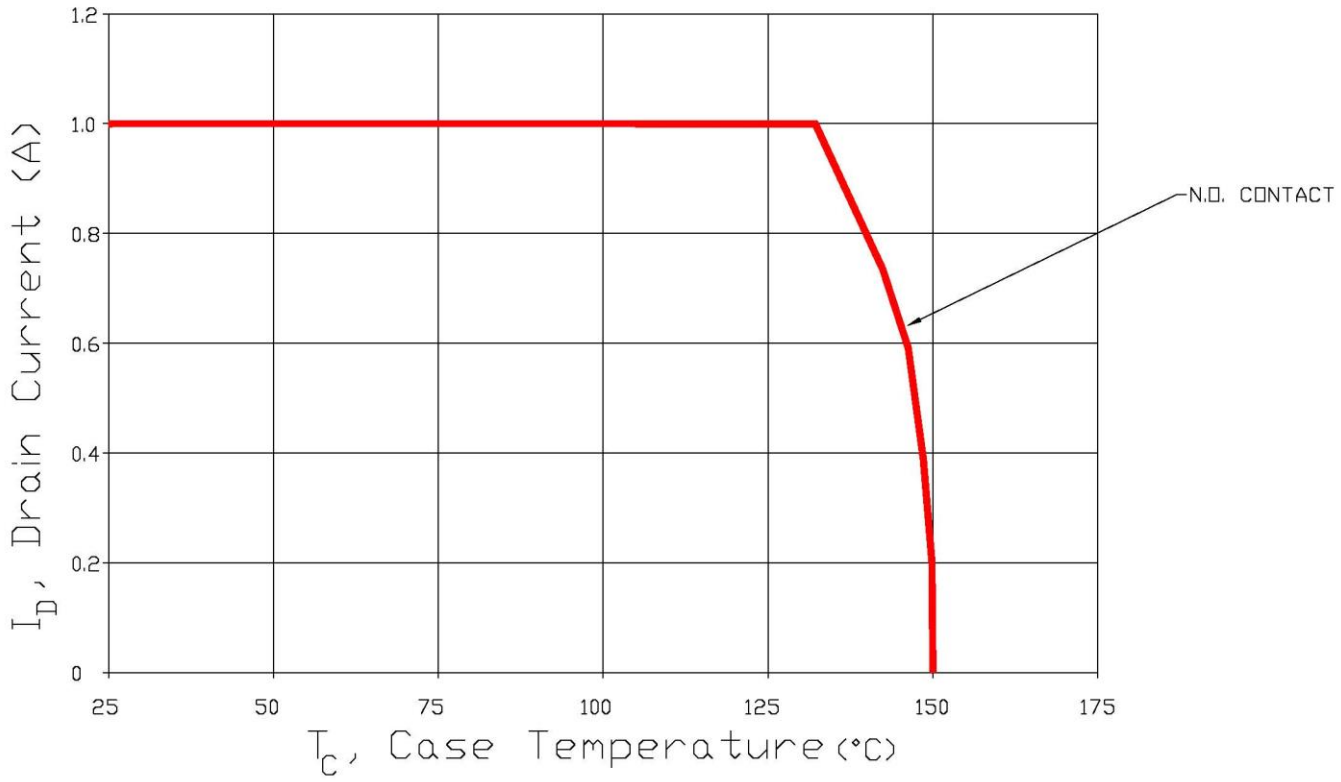

Figure 2 – Functional Block Diagram

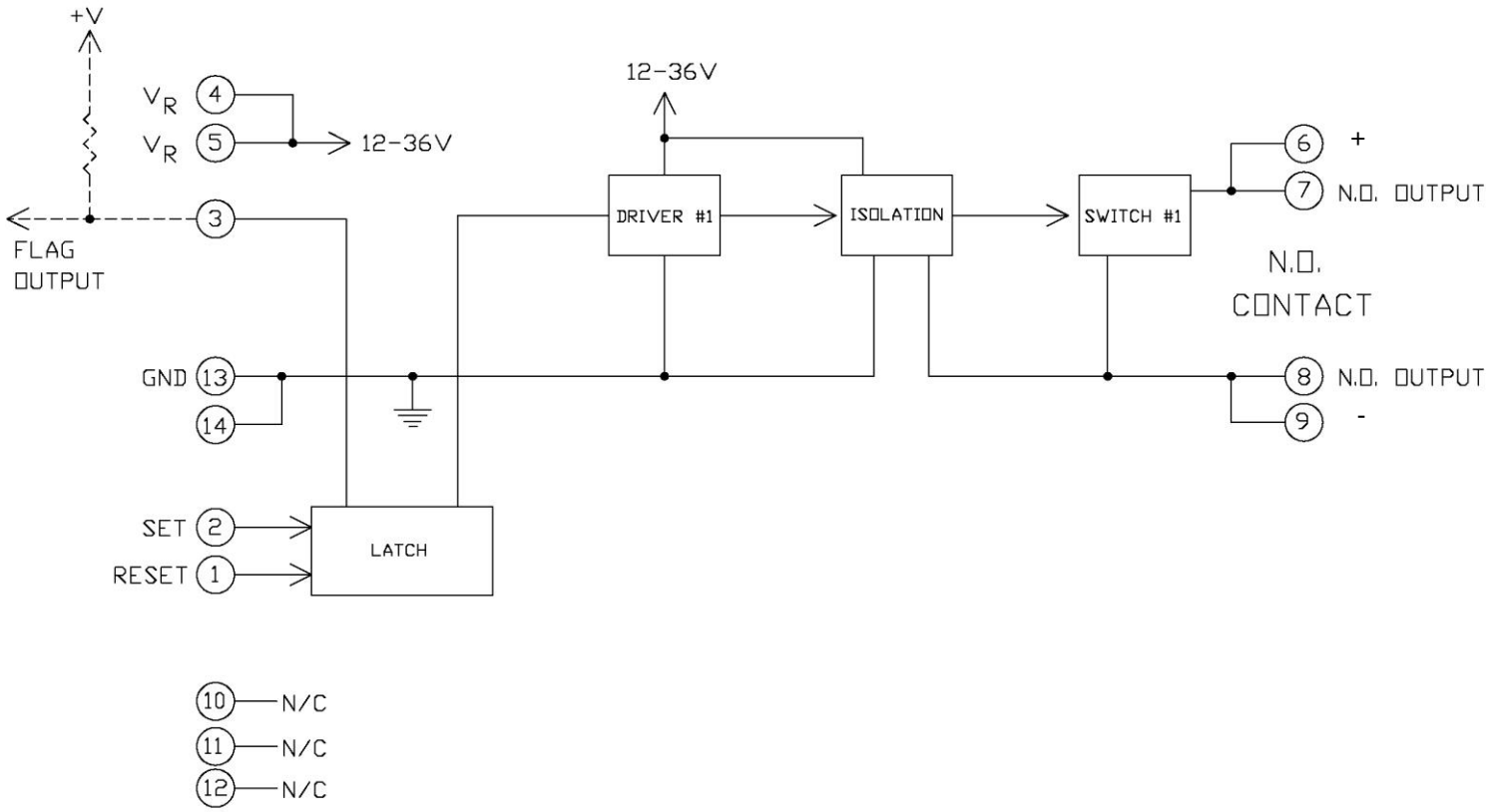

Figure 3 – Switching Test Circuit

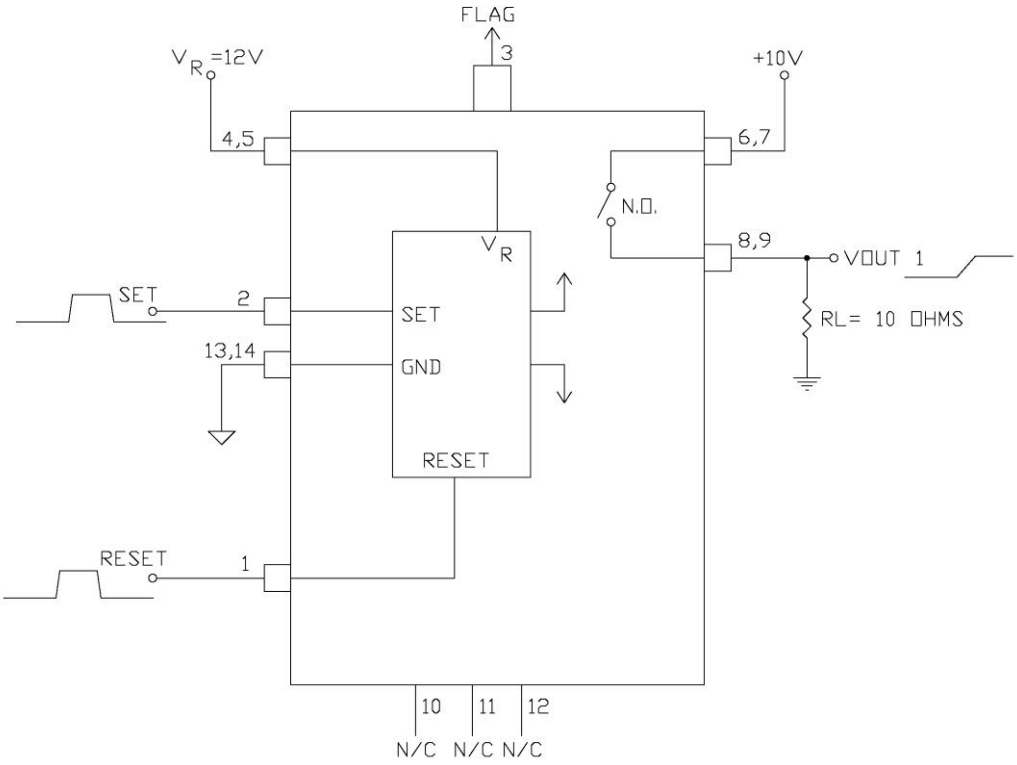

Figure 4 – Switching Test Waveform

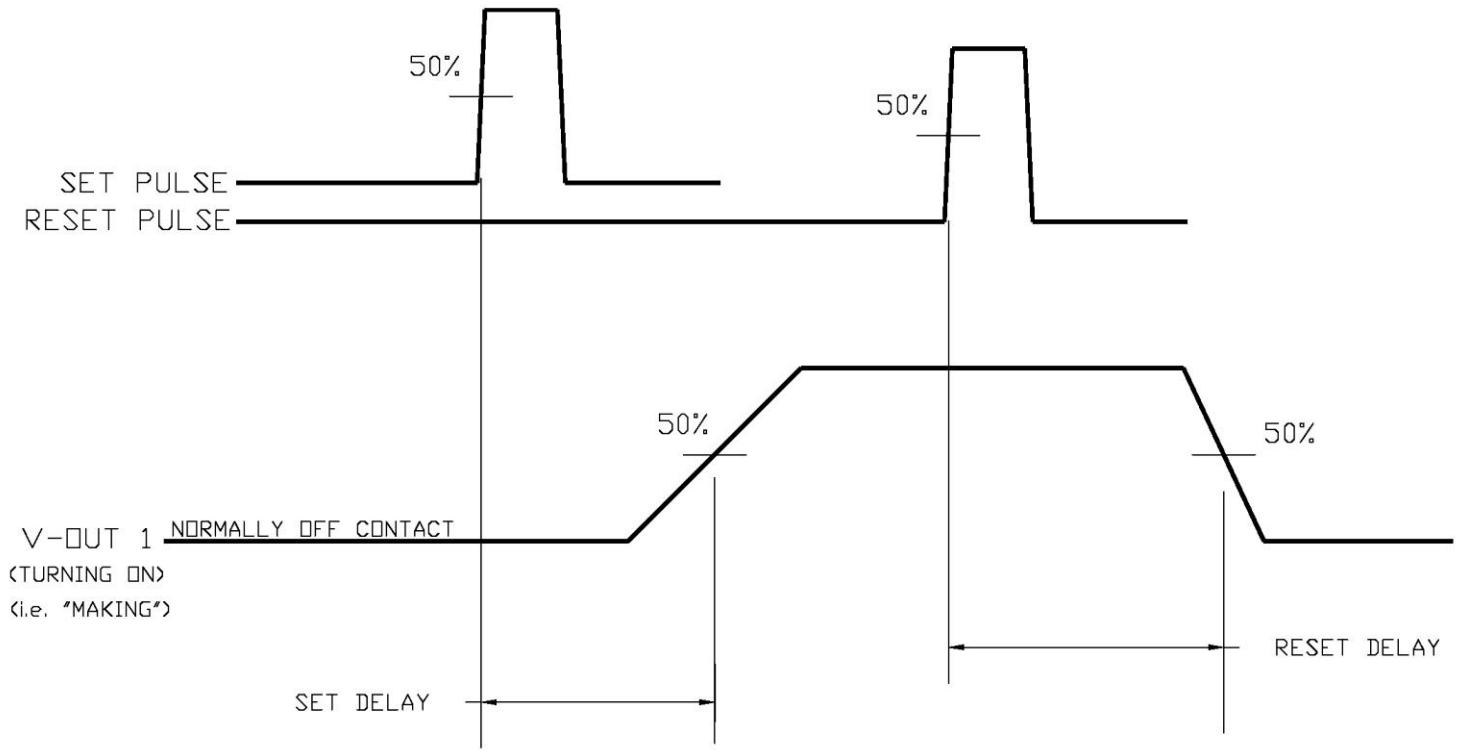

Figure 5 - Package, Dimensions, bottom view

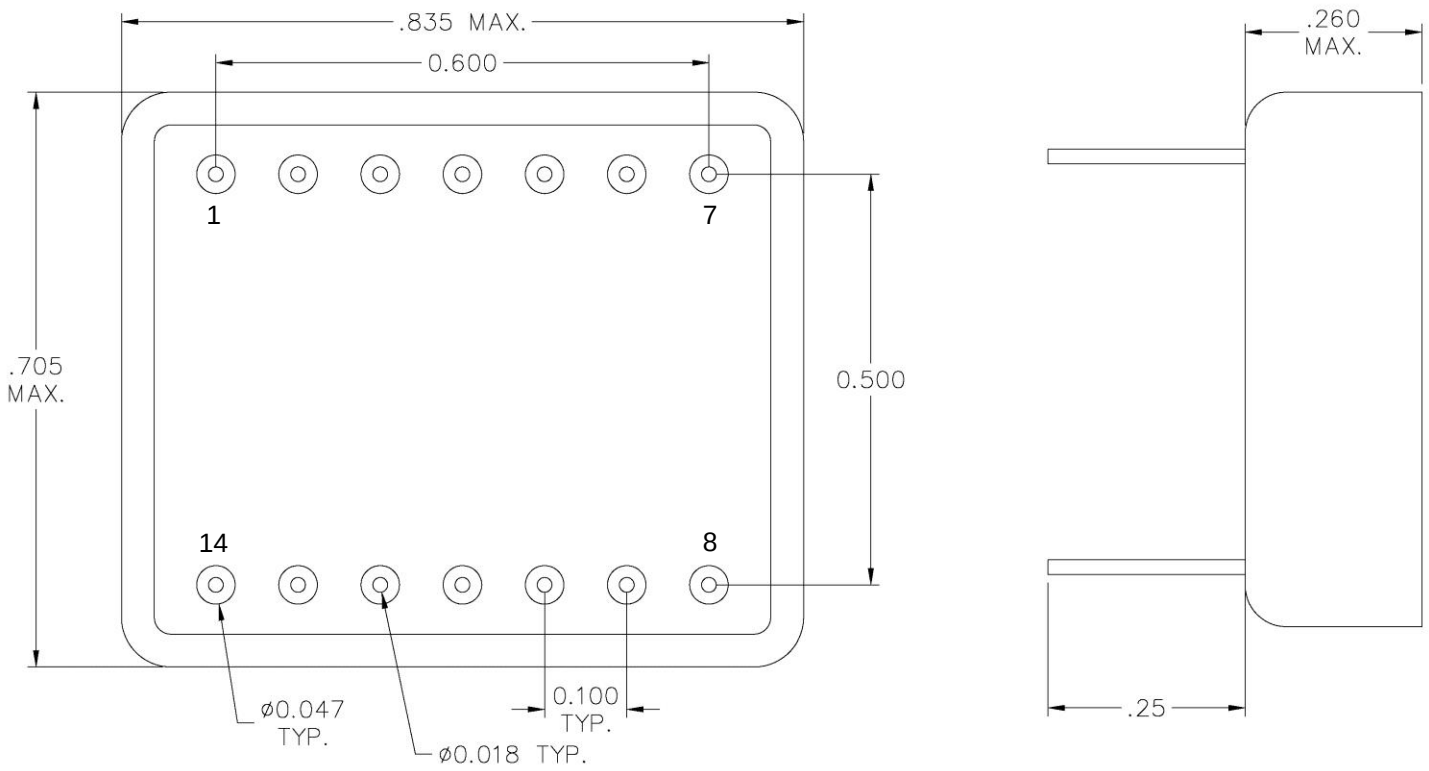

Figure 6 – Alternate Package, Dimensions

TBD

Table 7 – Pin Designations

Pin #	Pin Description
1	RESET
2	SET
3	FLAG
4	V_R
5	V_R
6	N.O. Switch (+)
7	N.O. Switch (+)
8	N.O. Switch (-)
9	N.O. Switch (-)
10	Not Connected
11	Not Connected
12	Not Connected
13	Power Return
14	Power Return

1.- Dimensioning and Telebanking per ASME Y14.53M-1994
2.- Controlling Dimension: Inch
3.- Dimensions are shown in inches
4.- Tolerances are +/-0.005 UOS
5.- Lead Dimensions are prior to Hot Solder Dip (if used)
6.- Lead finish per MIL-PRF-38534, Finish A, hot solder dip (Sn 63/Pb37) only on SMT lead bend option.
7.- For no leadbend, leads exit package as above and extend out 0.5” minimum.