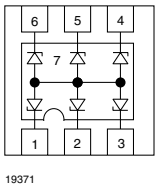
6-Line ESD-Protection Diode Array in LLP75



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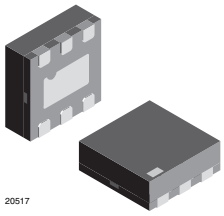
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FEATURES

- Ultra compact LLP75-7L package
- 6-line ESD-protection
- Low leakage current I_R < 1 µA
- Low load capacitance C_D = 40 pF
- ESD-immunity acc. IEC 61000-4-2
  ± 30 kV contact discharge
  ± 30 kV air discharge
- Working voltage range V_{RWM} = 5 V
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

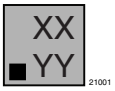
Pb-free

e4

RoHS COMPLIANT

HALOGEN FREE GREEN (5-2008)

MARKING (example only)



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Dot = pin 1 marking
XX = date code
YY = type code (see table below)

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VESD05A6-HAF	VESD05A6-HAF-GS08	3000	15 000

PACKAGE DATA

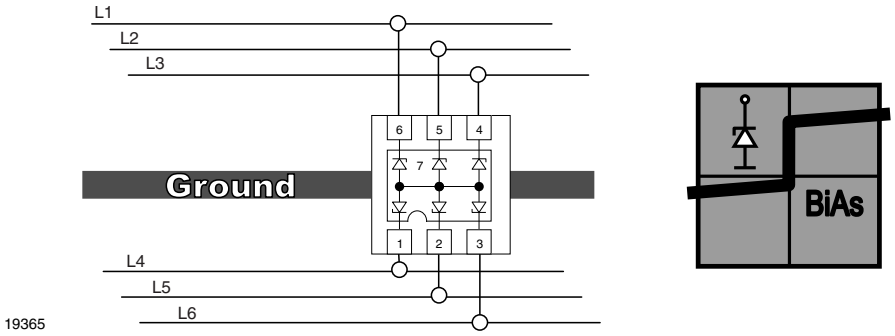
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VESD05A6-HAF	LLP75-7L	AS	4.2 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

ABSOLUTE MAXIMUM RATINGS VESD05A6-HAF

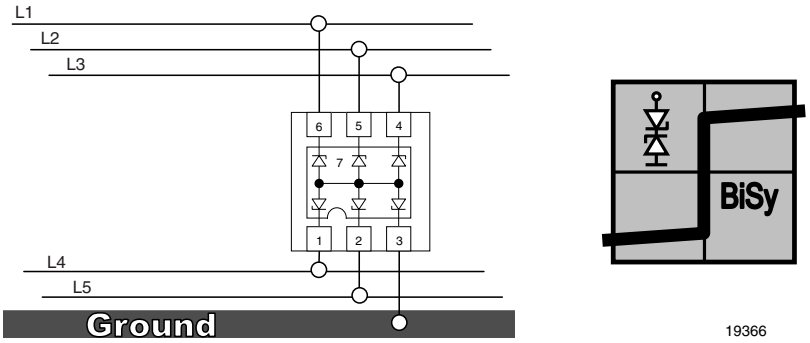
RATING	TEST CONDITION		SYMBOL	VALUE	UNIT
Peak pulse current	BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2); acc. IEC 61000-4-5; t_p = 8/20 µs; single shot		I_{PPM}	5	A
Peak pulse power	BiAs-mode: each input (pin 1 to pin 6) to ground (pin 2); acc. IEC 61000-4-5; t_p = 8/20 µs; single shot		P_{PP}	60	W
ESD immunity	Acc. IEC61000-4-2; 10 pulses BiAs-Mode: each input (pin 1 to pin 6) to ground (pin 2)	Contact discharge	V_{ESD}	± 30	kV
		Air discharge	V_{ESD}	± 30	kV
Operating temperature	Junction temperature		T_J	-40 to +125	°C
Storage temperature			T_{STG}	-55 to +150	°C

APPLICATION NOTE:

a) With the VESD05A6-HAF 6 different signal or data lines can be clamped to ground. Due to the different clamping levels in forward and reverse direction the VESD05A6-HAF clamping behavior is bidirectional and asymmetrical (BiAs).



b) If symmetrical clamping behaviour is required the VESD05A6-HAF can also be used as a bidirectional symmetrical protection device protecting up to 5 lines. In this case pin 7 must not be connected.



ELECTRICAL CHARACTERISTICS VESD05A6-HAF (Between pin 1, 2, 3, 4, 5 or 6, and pin 7) (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITIONS/REMARKS**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	6	lines
Reverse stand-off voltage	Max. reverse working voltage	V_{RWM}	-	-	5	V
Reverse voltage	at I_R = 1 µA	V_R	5	-	-	V
Max. reverse current	at V_R = 5 V	I_R	-	< 0.1	1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	6	6.6	7.5	V
Reverse clamping voltage	at I_{PP} = 1 A	V_C	-	8.1	10	V
	at I_{PP} = I_{PPM} = 5 A	V_C	-	11.3	12	V
Forward clamping voltage	at I_{PP} = 1 A	V_F	-	1.5	1.8	V
	at I_{PP} = I_{PPM} = 5 A	V_F	-	3.2	4.5	V
Line capacitance	at V_R = 0 V; f = 1 MHz	C_D	-	40	50	pF
	at V_R = 2.5 V; f = 1 MHz	C_D	-	24	-	pF

Note

- BiAs mode (between pin 1, 2, 3, 4, 5 or 6 and pin 7)

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

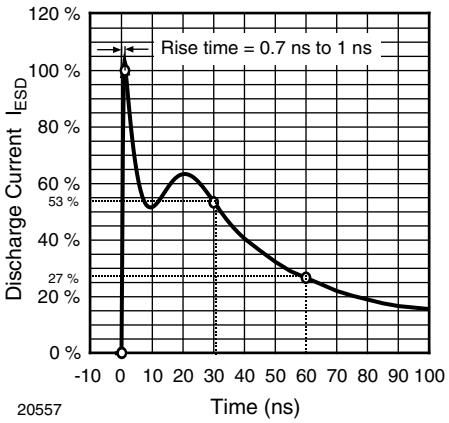


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

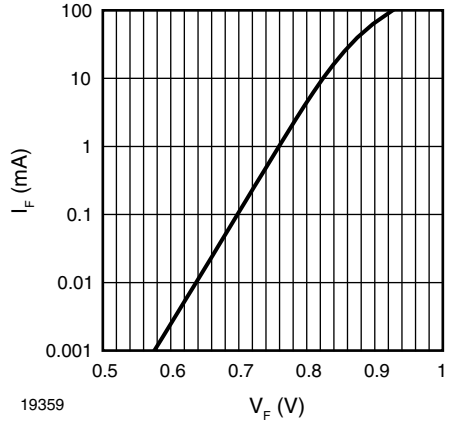


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

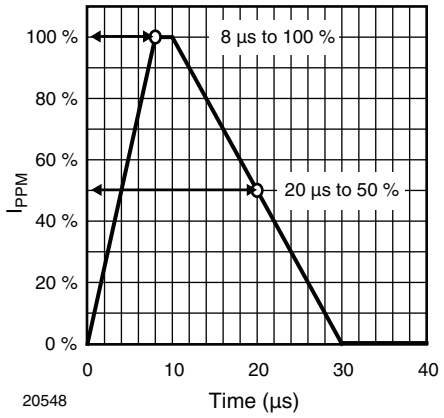


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

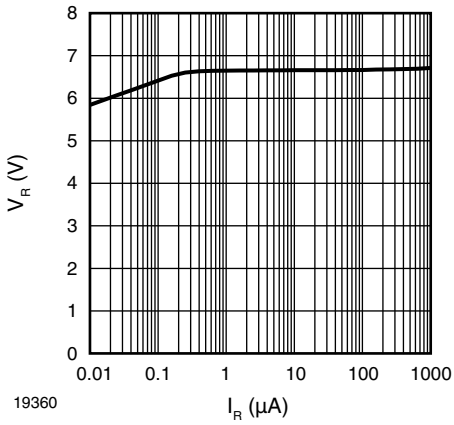


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

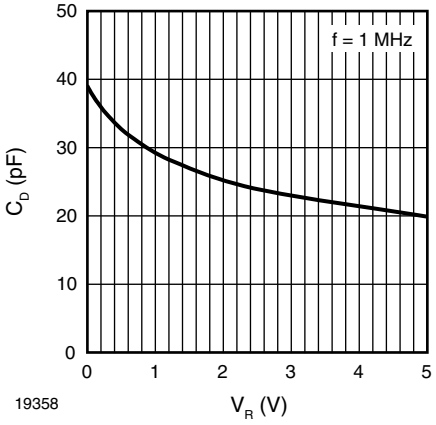


Fig. 3 - Typical Capacitance C_D vs. Reverse Voltage V_R

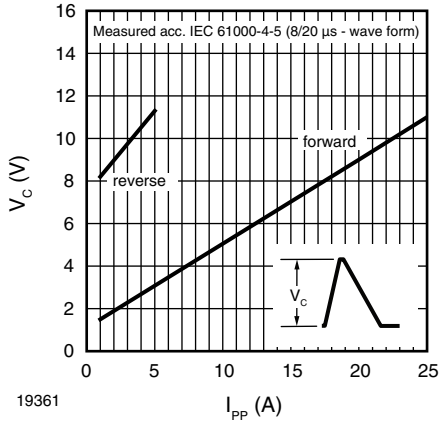


Fig. 6 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

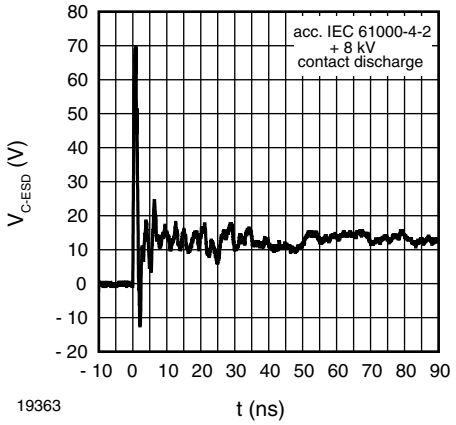


Fig. 7 - Typical Clamping Performance at + 8 kV
Contact Discharge (acc. IEC 61000-4-2)

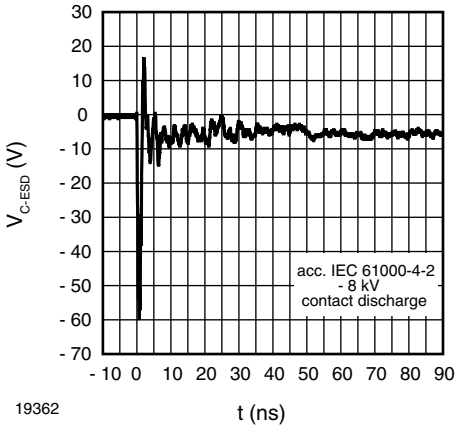


Fig. 8 - Typical Clamping Performance at - 8 kV
Contact Discharge (acc. IEC 61000-4-2)

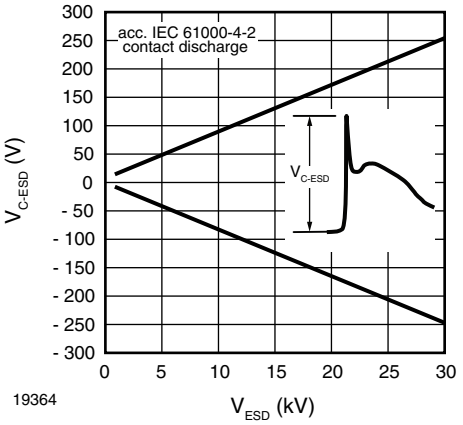
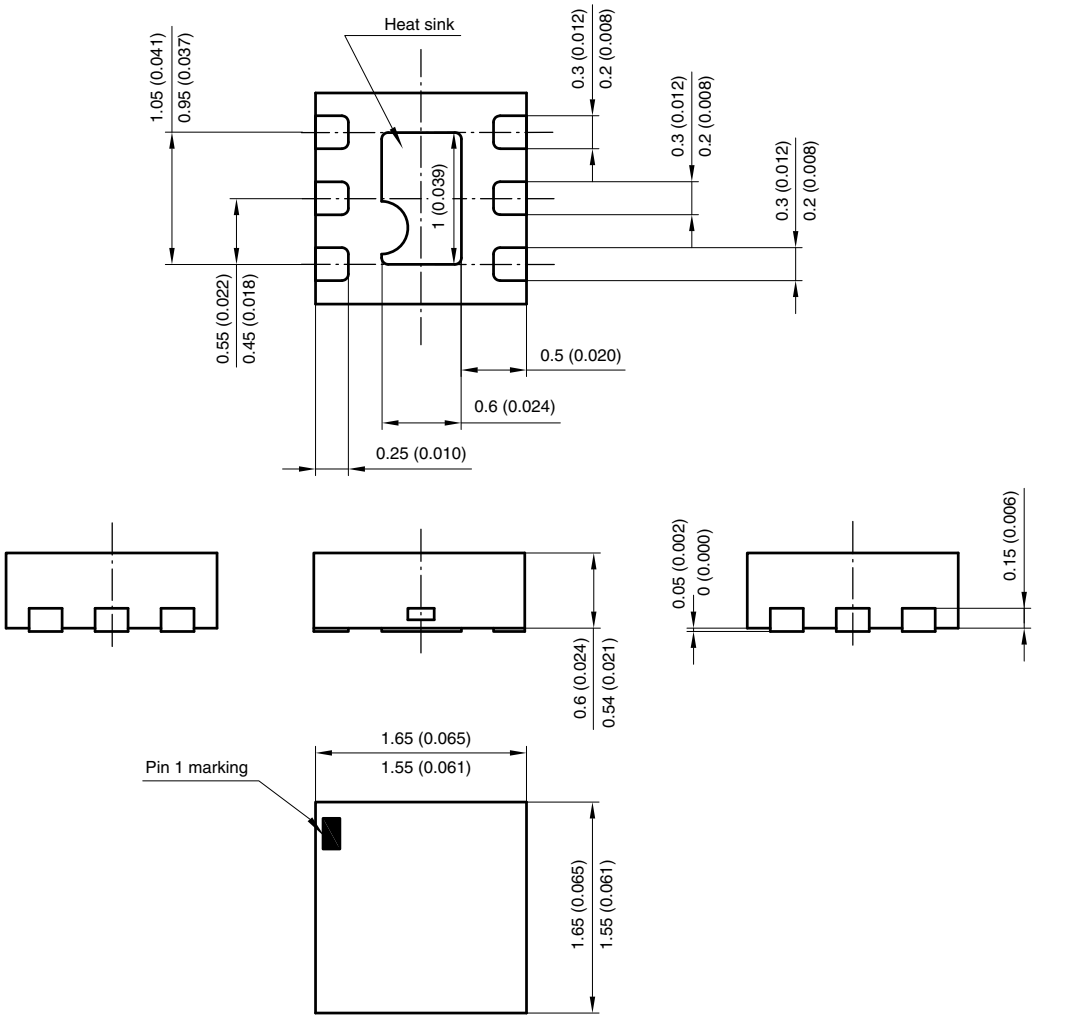
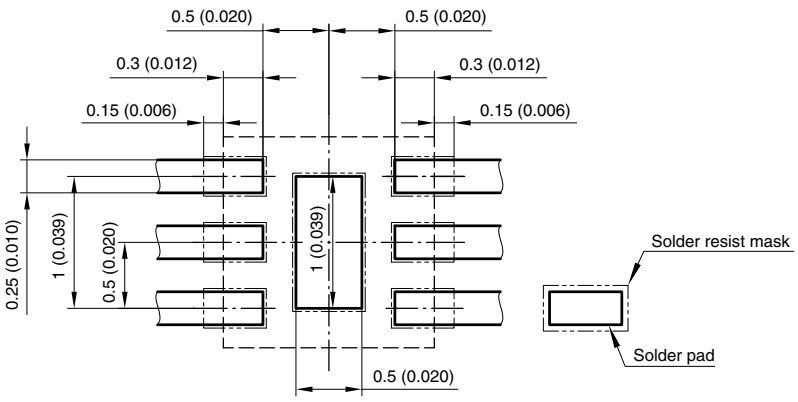


Fig. 9 - Typical Peak Clamping Voltage at ± ESD Contact Discharge
(acc. IEC 61000-4-2)

PACKAGE DIMENSIONS in millimeters (Inches): **LLP75-7L**



Foot print recommendation:



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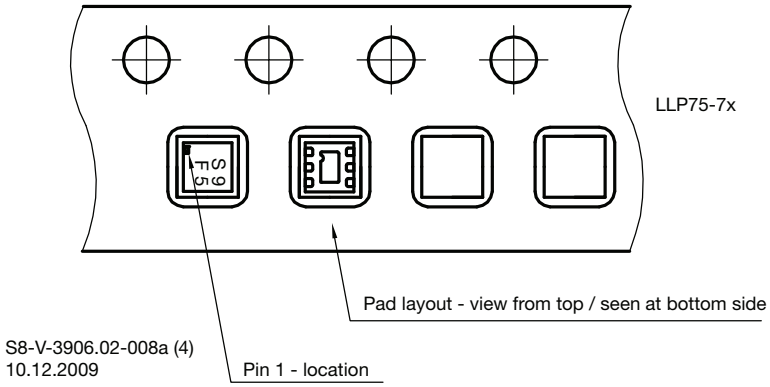

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