PE4314

Document Category: Advance Information

UltraCMOS® RF Digital Step Attenuator, 1 MHz–2.5 GHz

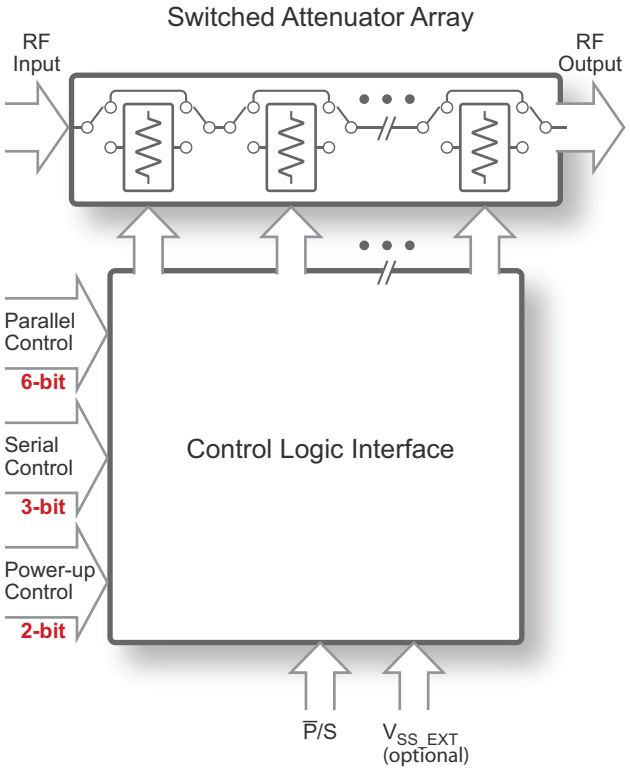
Features

- Attenuation step of 0.5 dB up to 31.5 dB
- Glitch-less attenuation state transitions
- Low distortion for CATV and multi-carrier applications
- Extended +105 °C operating temperature
- Parallel and Serial programming interfaces
- Packaging – 20-lead 4 × 4 × 0.85 mm QFN

Applications

- DOCSIS 3.0/1 customer premises equipment (CPE) and infrastructure
- Satellite CPE and infrastructure
- Fiber CPE and infrastructure

Figure 1 • *PE4314 Functional Diagram*



Product Description

The PE4314 is a 75Ω HaRP™ technology-enhanced, 6-bit RF digital step attenuator (DSA) that supports a frequency range from 1 MHz to 2.5 GHz. It features glitch-less attenuation state transitions and supports 1.8V control voltage and an extended operating temperature range up to +105 °C, making this device ideal for multiple wired broadband applications.

The PE4314 is a pin-compatible upgraded version of the PE4304, PE4307, PE4308 and PE43404. An integrated digital control interface supports both Serial and Parallel programming of the attenuation, including the capability to program an initial attenuation state at power up.

The PE4314 covers a 31.5 dB attenuation range in a 0.5 dB step. It is capable of maintaining 0.5 dB monotonicity through 2.5 GHz. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

The PE4314 is manufactured on Peregrine's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

Peregrine's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Optional External V_{SS}

For proper operation, the V_{SS_EXT} control pin must be grounded or tied to the V_{SS} voltage specified in **Table 2**. When the V_{SS_EXT} control pin is grounded, FETs in the switch are biased with an internal negative voltage generator. For applications that require the lowest possible spur performance, V_{SS_EXT} can be applied externally to bypass the internal negative voltage generator.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE4314*

Parameter/Condition	Min	Max	Unit
Supply voltage, V_{DD}	–0.3	5.5	V
Digital input voltage	–0.3	3.6	V
RF input power, 75mΩ		+28	dBm
Storage temperature range	–65	+150	°C
ESD voltage HBM(1), all pins		1500	V
ESD voltage CDM(2), all pins		1000	V

Notes:
1) Human body model (MIL-STD 883 Method 3015).
2) Charged device model (JEDEC JESD22-C101).

Recommended Operating Conditions

Table 2 lists the recommending operating conditions for the PE4314. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE4314*

Parameter	Min	Typ	Max	Unit
Normal mode, V_{SS_EXT} = 0V(1)				
Supply voltage, V_{DD}	2.3	3.3	5.5	V
Supply current, I_{DD}		130	200	µA
Bypass mode, V_{SS_EXT} = –3.4V(2)				
Supply voltage, V_{DD} (V_{DD} ≥ 3.4V. See **Table 3** for full spec compliance.)	2.7	3.4	5.5	V
Supply current, I_{DD}		65	95	µA
Negative supply voltage, V_{SS_EXT}	–3.6		–3.2	V
Negative supply current, I_{SS}	–40	–16		µA
Normal or bypass mode				
Digital input high	1.17		3.6	V
Digital input low	–0.3		0.6	V
Digital input current(3)			1	µA
RF input power, CW(4) • 1–50 MHz • >50 MHz–2.5 GHz			 TBD +24	 dBm dBm
RF input power, pulsed(5)			TBD	dBm
Operating temperature range	–40	+25	+105	°C

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 12) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 12) to bypass and disable internal negative voltage generator.
3) Applies to all pins except pins 1, 5, 7 and 20. Pins 1, 7 and 20 have an internal 1 MΩ pull-down resistor to ground and pin 5 has an internal 2 MΩ pull-up resistor to internal V_{DD}.
4) 100% duty cycle, all bands, 75Ω.
5) Pulsed, 5% duty cycle of 4620 µs period, 75Ω.

Electrical Specifications

Table 3 provides the PE4314 key electrical specifications @ +25 °C, Z_S = Z_L = 75Ω, unless otherwise specified. Normal mode[1] is @ V_{DD} = 3.3V and V_{SS_EXT} = 0V. Bypass mode[2] is @ V_{DD} = 3.4V and V_{SS_EXT} = –3.4V.

Table 3 • *PE4314 Electrical Specifications*

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operation frequency			1 MHz		2.5 GHz	As shown
Attenuation range	0.5 dB step			0–31.5		dB
Insertion loss	Reference state	1–204 MHz 204–870 MHz 870–1218 MHz 1218–2500 MHz		1 1.2 1.3 1.5		dB dB dB dB
Attenuation error	Any bit or bit combination	1–204 MHz 204–870 MHz 870–1218 MHz 1218–1794 MHz			± (0.15 + 4.0% of attenuation setting)	dB
		1794–2500 MHz			± (0.15 + 8.0% of attenuation setting)	dB
Return loss	Input port or output port, reference state	1–204 MHz 204–870 MHz 870–1794 MHz 1794–2500 MHz		19 18 16 17		dB dB dB dB
Relative phase	All states	2500 MHz		40		deg
Input 0.1dB compression point[3]		2500 MHz		28		dBm
Input IP2		5 MHz 10 MHz 17 MHz 35 MHz 35–2500 MHz		TBD TBD 80 87 98		dBm dBm dBm dBm dBm
Input IP3	Two-tones at +18 dBm, 20 MHz spacing	5 MHz 10 MHz 17 MHz 35 MHz 35–2500 MHz		TBD TBD 63 62 56		dBm dBm dBm dBm dBm
Video feed-through	DC measurement			10		mV_{PP}
Switching time	50% CTRL to 90% or 10% RF				1	µs
Attenuation transient (envelope)				0.5		dB

Table 3 • *PE4314 Electrical Specifications (Cont.)*

Parameter	Condition	Frequency	Min	Typ	Max	Unit

Notes:

1) Normal mode: connect V_{SS_EXT} (pin 12) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
2) Bypass mode: use V_{SS_EXT} (pin 12) to bypass and disable internal negative voltage generator.
3) The input 0.1dB compression point is a linearity figure of merit. Refer to **Table 2** for the operating RF input power (75Ω).

Switching Frequency

The PE4314 has a maximum 25 kHz switching frequency in normal mode (pin 12 tied to ground). A faster switching frequency is available in bypass mode (pin 12 tied to V_{SS_EXT}). The rate at which the PE4314 can be switched is then limited to the switching time as specified in **Table 3**.

Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reached 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spur-Free Performance

The typical spurious performance of the PE4314 in normal mode is TBD dBm (pin 12 tied to ground). If spur-free performance is desired, the internal negative voltage generator can be disabled by applying a negative voltage to V_{SS_EXT} (pin 12).

Glitch-less Attenuation State Transitions

The PE4314 features a novel architecture to provide the best-in-class glitch-less transition behavior when changing attenuation states. When RF input power is applied, the output power spikes are greatly reduced (0.5 dB) during attenuation state changes when comparing to previous generations of DSAs.

Truth Tables

Table 4 and **Table 5** provide the truth tables for the PE4314.

Table 4 • *Parallel Truth Table for PE4314*(*)

$\overline{P}$/S	C16	C8	C4	C2	C1	C0.5	Attenuation Setting RF1–RF2
0	0	0	0	0	0	0	Reference IL
0	0	0	0	0	0	1	0.5 dB
0	0	0	0	0	1	0	1 dB
0	0	0	0	1	0	0	2 dB
0	0	0	1	0	0	0	4 dB
0	0	1	0	0	0	0	8 dB
0	1	0	0	0	0	0	16 dB
0	1	1	1	1	1	1	31.5 dB

Note: * Not all 64 possible combinations of C0.5–C16 are shown.

Table 5 • *Parallel Control Bits Truth Table for PE4314*(*)

$\overline{P}$/S	LE	PUP1	PUP2	Attenuation Setting RF1–RF2
0	0	0	0	Reference IL
0	0	0	1	8 dB
0	0	1	0	16 dB
0	0	1	1	31.5 dB
0	1	X	X	Defined by C0.5–C16

Note: * Power up with LE = 1 provides normal parallel operation with C0.5–C16, and PUP1 and PUP2 are not active.

Programming Options

Parallel/Serial Selection

Either a Parallel or Serial interface can be used to control the PE4314. The $\overline{P}$/S bit provides this selection, with $\overline{P}$/S = LOW selecting the Parallel interface and $\overline{P}$/S = HIGH selecting the Serial interface.

Parallel Mode Interface

The Parallel interface consists of six CMOS-compatible control lines that select the desired attenuation state, as shown in **Table 4**.

The Parallel interface timing requirements are defined by **Figure 3**, **Table 7** and switching time in **Table 3**.

For Latched Parallel programming, the latched enable (LE) should be held LOW while changing attenuation state control values, then pulsed LE HIGH to LOW (per **Figure 3**) to latch new attenuation state into the device.

For Direct Parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches or jumpers).

In Parallel mode, DATA and CLOCK (CLK) pins are “don’t care” and may be tied to logic LOW or logic HIGH.

Serial Interface

The Serial interface is a 6-bit Serial-in, Parallel-out shift register buffered by a transparent latch. It is controlled by using three CMOS-compatible signals: DATA, CLK and LE. The DATA and CLK inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input. Serial data is clocked in MSB first.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the Serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Serial timing for the operation is defined by **Figure 2** and **Table 6**.

Power-up Control Settings

The PE4314 always assumes a specifiable attenuation setting on power up. This feature exists for both the Serial and Parallel modes of operation, and allows a known attenuation state to be established before an initial Serial or Parallel control word is provided.

When the attenuator powers up in Serial mode ($\overline{P}$/S = 1), the six control bits are set to whatever data is present on the six Parallel data inputs (C0.5–C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

When the attenuator powers up in Parallel mode ($\overline{P}$/S = 0) with LE = 0, the control bits are automatically set to one of four possible values. These four values are selected by the two power-up (PUP) control bits, PUP1 and PUP2, as shown in **Table 5**.

Figure 2 • *Serial Interface Timing Diagram*

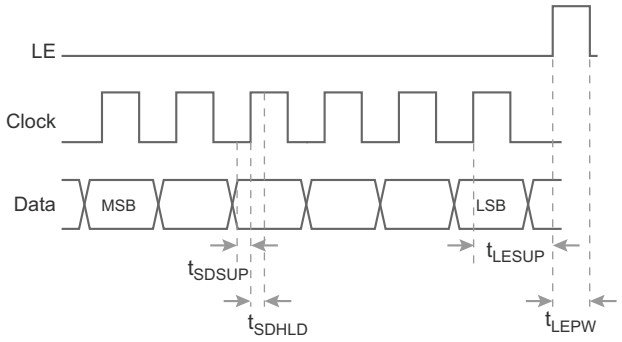
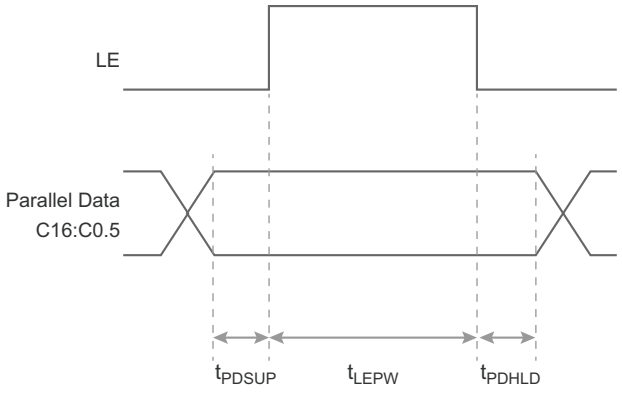


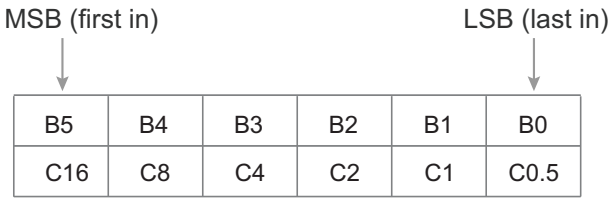
Figure 3 • *Parallel Interface Timing Diagram*



Serial Register Map

Figure 4 provides the Serial programming register map for the PE4314.

Figure 4 • *Serial Register Map*(*)



Note: * For backward compatibility, the same programming scheme can be used.

Table 6 • *Serial Interface AC Characteristics*(1)

Parameter	Min	Max	Unit
Serial data clock frequency, f_{CLK}(2)		10	MHz
Serial clock HIGH time, t_{CLKH}	30		ns
Serial clock LOW time, t_{CLKL}	30		ns
LE set-up time after last clock rising edge, t_{LESUP}	10		ns
LE minimum pulse width, t_{LEPW}	30		ns
Serial data set-up time before clock rising edge, t_{SDSUP}	10		ns
Serial data hold time after clock rising edge, t_{SDHLD}	10		ns

Notes:
1) V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +105 °C, unless otherwise specified.
2) f_{CLK} is verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10 MHz to verify f_{CLK} specification.

Table 7 • *Parallel Interface AC Characteristics*(*)

Parameter	Min	Max	Unit
LE minimum pulse width, t_{LEPW}	10		ns
Data set-up time before rising edge of LE, t_{PDSUP}	10		ns
Data hold time after falling edge of LE, t_{PDHLD}	10		ns

Note: * V_{DD} = 3.3V or 5.0V, –40 °C < T_A < +105 °C, unless otherwise specified.

Pin Information

This section provides pinout information for the PE4314. **Figure 5** shows the pin map of this device for the available package. **Table 8** provides a description for each pin.

Figure 5 • *Pin Configuration (Top View)*

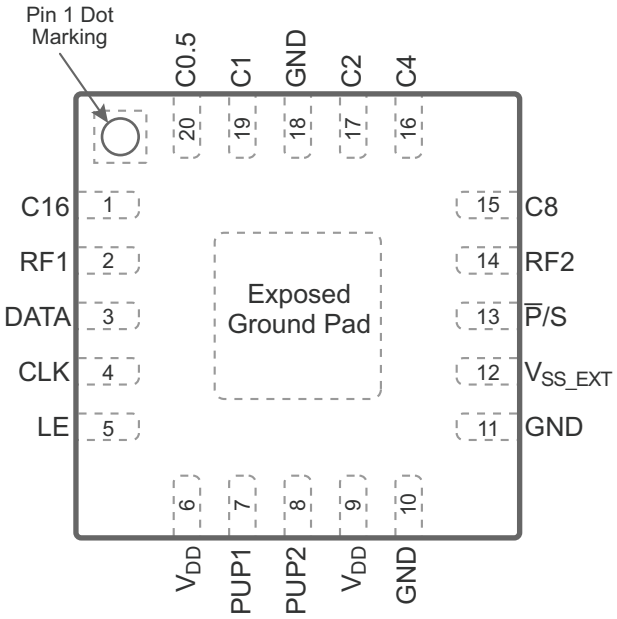


Table 8 • *Pin Descriptions for PE4314*

Pin No.	Pin Name	Description
1	C16[4]	Parallel control bit, 16 dB
2	RF1[1]	RF1 port
3	DATA	Serial interface data input
4	CLK	Serial interface clock input
5	LE[2]	Serial interface latch enable input
6, 9	V_{DD}	Supply voltage
7	PUP1[4]	Power-up control bit, MSB
8	PUP2	Power-up control bit, LSB
10, 11, 18	GND	Ground
12	V_{SS_EXT}[3]	External V_{SS} negative control voltage
13	$\overline{P}$/S	Parallel/Serial mode select
14	RF2[1]	RF2 port
15	C8[4]	Parallel control bit, 8 dB
16	C4[4]	Parallel control bit, 4 dB
17	C2[4]	Parallel control bit, 2 dB
19	C1[4]	Parallel control bit, 1 dB
20	C0.5[4]	Parallel control bit, 0.5 dB
Pad	GND	Exposed pad: ground for proper operation

Notes:

1) RF pins 2 and 14 must be at 0 VDC. The RF pins do not require DC blocking capacitors for proper operation if the 0 VDC requirement is met.
2) LE has an internal 2 MΩ resistor to internal V_{DD}.
3) Use V_{SS_EXT} (pin 12) to bypass and disable internal negative voltage generator. Connect V_{SS_EXT} (pin 12) to GND (V_{SS_EXT} = 0V) to enable internal negative voltage generator.
4) Ground PUP1, C0.5, C1, C2, C4, C8 or C16 if not in use.

Packaging Information

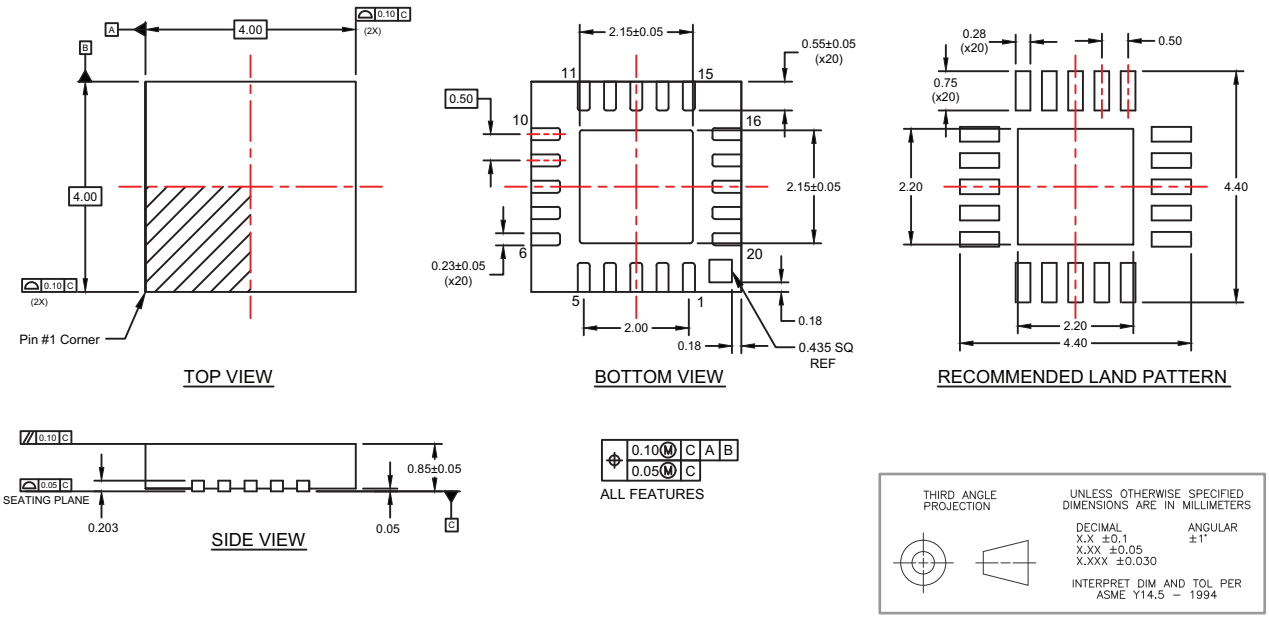
This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE4314 in the 20-lead 4 × 4 × 0.85 mm QFN package is MSL1.

Package Drawing

Figure 6 • ***Package Mechanical Drawing for 20-lead 4 × 4 × 0.85 mm QFN***



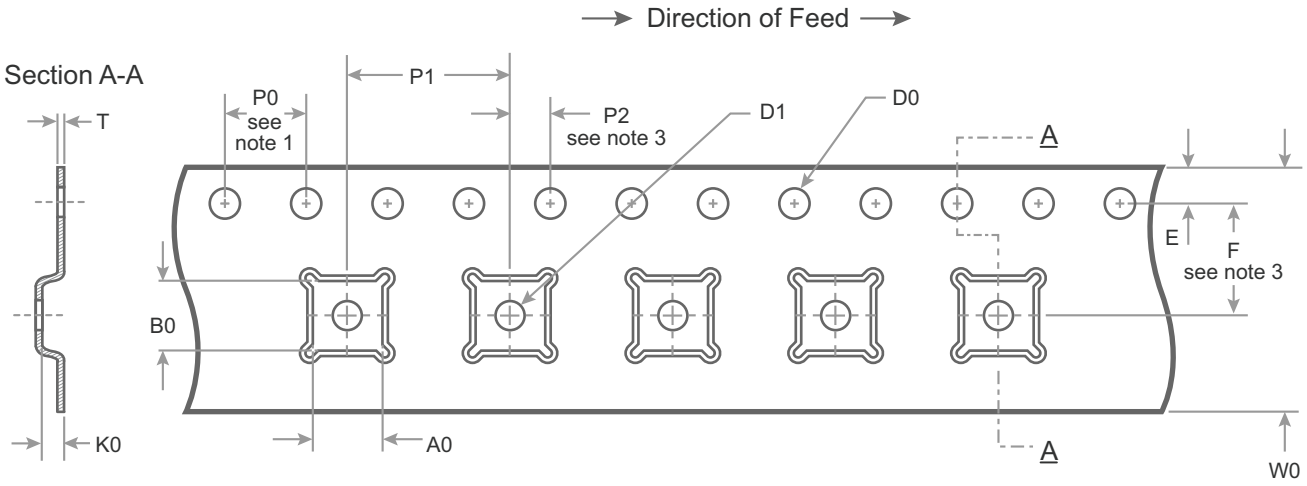
Top-Marking Specification

Figure 7 • ***Package Marking Specifications for PE4314***

● = Pin 1 indicator
YY = Last two digits of assembly year
WW = Assembly work week
ZZZZZZ = Assembly lot code (maximum six characters)

Tape and Reel Specification

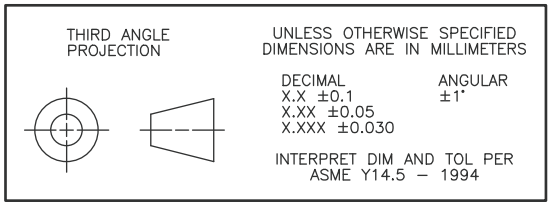
Figure 8 • ***Tape and Reel Specifications for 20-lead 4 × 4 × 0.85 mm QFN***

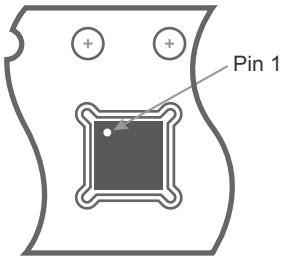


Notes:

1. 10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

A0	4.35
B0	4.35
K0	1.10
D0	1.50 + 0.10/ -0.00
D1	1.50 min
E	1.75 ± 0.10
F	5.50 ± 0.05
P0	4.00
P1	8.00
P2	2.00 ± 0.05
T	0.30 ± 0.05
W0	12.00 ± 0.30





Device Orientation in Tape

Ordering Information

Table 9 lists the available ordering codes for the PE4314 as well as available shipping methods.

Table 9 • *Order Codes for PE4314*

Order Codes	Description	Packaging	Shipping Method
PE4314A–Z	PE4314 digital step attenuator	Green 20-lead 4 × 4 mm QFN	3000 Units/T&R
EK4314–01	PE4314 evaluation kit	Evaluation kit	1/Box

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Not Recommended for New Designs (NRND)

This product is in production but is not recommended for new designs.

End of Life (EOL)

This product is currently going through the EOL process. It has a specific last-time buy date.

Obsolete

This product is discontinued. Orders are no longer accepted for this product.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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