Product Specification

PE95420

RF SPDT Switch
Hermetically sealed ceramic package
1 – 8500 MHz

Features

- HaRP™-Technology-Enhanced
  - Eliminates Gate and Phase Lag
  - No Insertion Loss or Phase Drift
- High Linearity: 60 dBm IIP3
- Low Insertion Loss:
  - 0.77 dB at 100 MHz
  - 1.0 dB at 3000 MHz
  - 1.15 dB at 6000 MHz
  - 1.38 dB at 8500 MHz
- High Isolation (RF1-RF2)
  - 86.5 dB at 100 MHz
  - 48.2 dB at 3000 MHz
  - 36.6 dB at 6000 MHz
  - 27.8 dB at 8500 MHz
- Fast Switching Time
  - 700 ns RF ON
  - 300 ns RF OFF
- Ultra-Low Power Consumption
  - 3.3 µW @ 3.3 V
- 1 dB Compression Point of +33 dBm
- Single-pin 3.3 V CMOS logic control
- ESD tolerant to 2000 V HBM
- Absorptive/Non-Reflective
- Offered in a 7-lead Hermetic CSOIC Surface-Mount Package and in DIE form

Product Description

The PE95420 is an RF SPDT (single pole double throw) switch and is available in a hermetically sealed ceramic package. The PE95420 is designed to cover a broad range of applications from 1 to 8500 MHz for use in various Hi-Rel industries and applications requiring broadband performance. It uses Peregrine's UltraCMOS™ process and features HaRP™ technology enhancements to deliver high linearity and exceptional harmonics performance. HaRP technology is an innovative feature of the UltraCMOS™ process providing upgraded linearity performance.

The PE95420 is an absorptive/non-reflective switch design which is an ideal termination method for RF elements in a system design. A single-pin 3.3V CMOS logic control in a single chip solution reduces the number of control lines.

Typical Industries

- Medical
- Automotive
- Telecom Infrastructure
- Test Instrumentation
- Down-hole oil/gas
- Military
- Commercial space applications

Figure 1. Functional Diagram

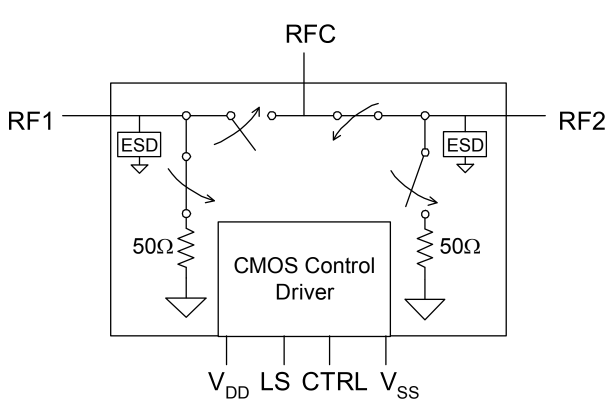


Figure 2. Package Type

7-lead CSOIC

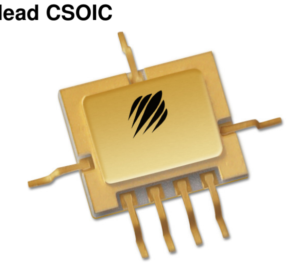


Table 1. Electrical Specifications @ -40°C ≤ T ≤ 85°C & 3.0V ≤ VDD ≤ 3.6V

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency		1		8500	MHz
Insertion Loss	100 MHz		0.77	0.95	dB
	3000 MHz		1	1.28	dB
	6000 MHz		1.15	1.42	dB
	8500 MHz		1.38	1.72	dB
Isolation – RFC to RF1	100 MHz	74	75.6		dB
	3000 MHz	46	47.4		dB
	6000 MHz	43.8	48		dB
	8500 MHz (note 2)	31	38		dB
Isolation – RFC to RF2	100 MHz	73.7	75.4		dB
	3000 MHz	46.8	48.3		dB
	6000 MHz	45	52.1		dB
	8500 MHz (note 2)	31	38		dB
Isolation – RF1 to RF2	100 MHz		86.5		dB
	3000 MHz		48.2		dB
	6000 MHz		36.6		dB
	8500 MHz		27.8		dB
Return Loss Active Port – ON State	100 MHz		21		dB
	3000 MHz		33		dB
	6000 MHz		20		dB
	8500 MHz		15		dB
Return Loss Active Port – OFF State	100 MHz		20		dB
	3000 MHz		18		dB
	6000 MHz		15		dB
	8500 MHz		8		dB
Input 1 dB Compression (note 1)	8500 MHz		33		dBm
Input IP3	8500 MHz, 18 dBm input power/tone		60		dBm
Switching Time	50% CTRL to 90% of final value when RF ON		700		ns
	50% CTRL to 10% of final value when RF OFF		300		ns

Note: 1. Please note Maximum Operating Pin (50Ω) of +24dBm in *Table 3*.
2. Guaranteed but not tested

Figure 3. Pin Layout (Top View)

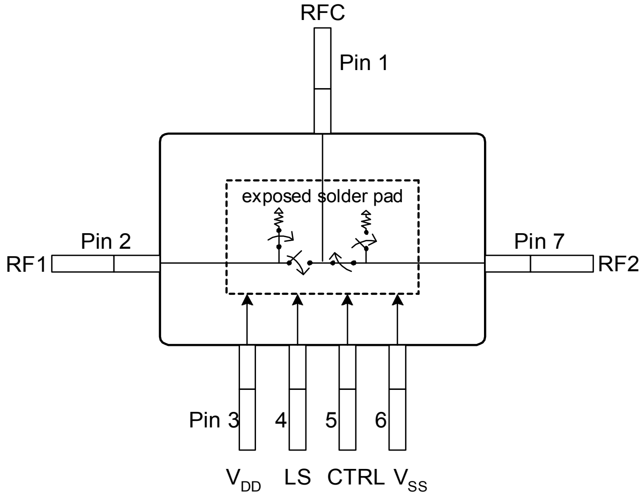


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RFC[1]	RF Common
2	RF1[1]	RF Port 1
3	V_{DD}	Nominal 3.3 V supply connection
4	LS	Selects the RF1 to RFC path (See *Table 6*)
5	CTRL	Selects the RF2 to RFC path (See *Table 6*)
6	V_{SS}	Negative power supply. Apply nominal –3.3 V supply
7	RF2[1]	RF Port 2
paddle	GND	Exposed Solder Pad, grounded for proper device operation.

Note 1: All RF pins must be DC blocked with an external series capacitor or held at 0 Vdc.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Positive Power Supply Voltage	3.0	3.3	3.6	V
V_{SS} Negative Power Supply Voltage	-3.6	-3.3	-3.0	V
I_{DD} Power Supply Current (V_{DD} = 3.3V, LS or CTRL = 3.3V)		< 1		µA
I_{SS} Power Supply Current (V_{SS} = -3.3V)		< 1		µA
Control Voltage High	0.7xV_{DD}			V
Control Voltage Low			0.3xV_{DD}	V
Operating temperature range	-40		85	°C
RF Power In (50Ω): 1 MHz ≤ 8.5 GHz			24	dBm

Table 4. Post Radiation Table

Total Dose	Parameter	Min	Max	Units
Post** 20krad	I_{DD} Positive Supply Current		100	µA
	I_{SS} Negative Supply Current	-500		µA
Post 100krad	I_{DD} Positive Supply Current		0.5	mA
	I_{SS} Negative Supply Current	-5		mA

**Characterized but not tested

Table 5. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_{C1}	Voltage on LS input	-0.3	V_{DD}+ 0.3	V
V_{C2}	Voltage on CTRL input	-0.3	V_{DD}+ 0.3	V
Θ_{JC}	Theta JC		24	°C/W
T_{ST}	Storage temperature range	-65	150	°C
V_{ESD}	ESD voltage (Human Body Model)		2000	V

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Truth Table

LS	CTRL	RFC-RF1	RFC-RF2	Logic State
0	0	off	off	OFF state
0	1	off	on	RF2 active
1	0	on	off	RF1 active
1	1	N/A*	N/A*	N/A*

* Invalid state that should not be used for normal operation.

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Switching Frequency

The PE95420 has a maximum 25 kHz switching rate.

Performance Plots

Figure 4. Insertion Loss: RF1 @ 3.3 V

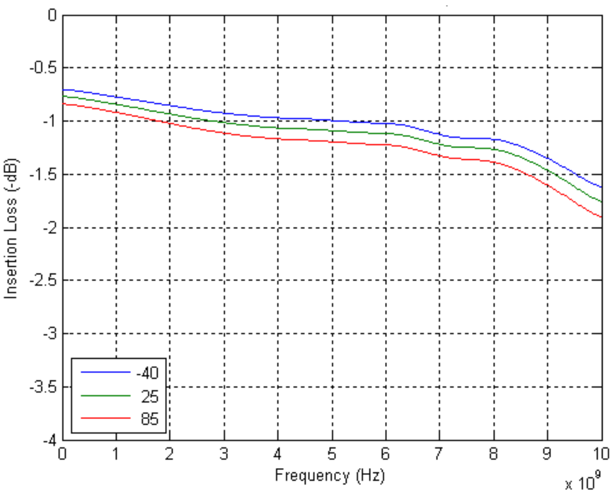


Figure 5. Insertion Loss: RF1 @ 25 °C

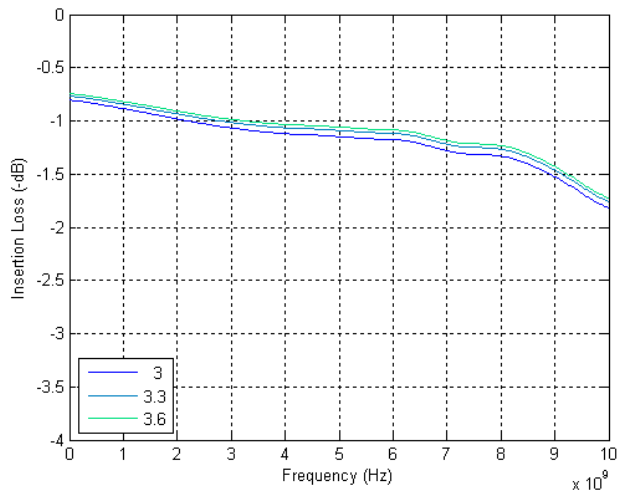


Figure 6. Insertion Loss: RF2 @ 3.3 V

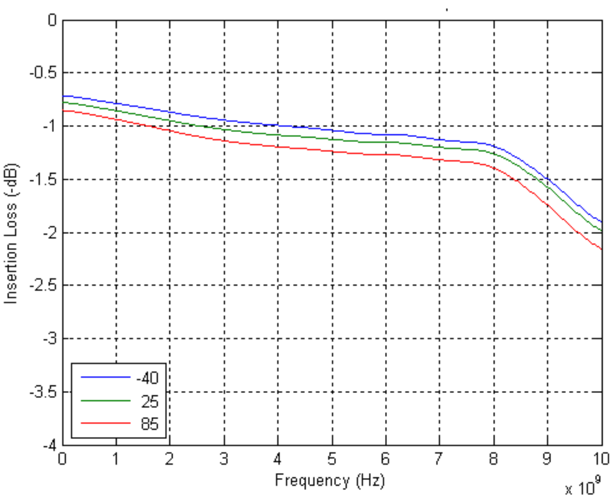
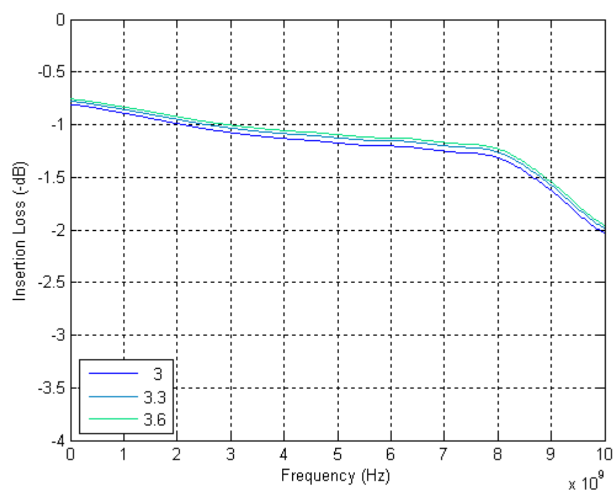


Figure 7. Insertion Loss: RF2 @ 25 °C



Performance Plots

Figure 8. Isolation: RF1-RF2, RF1 Active @ V_{DD} = 3.3V

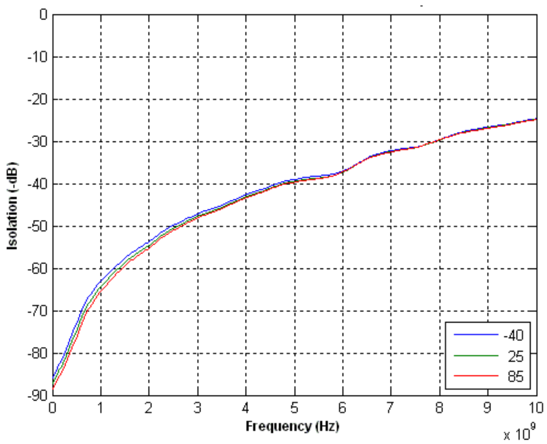


Figure 9. Isolation: RF2-RF1, RF2 Active @ V_{DD} = 3.3V

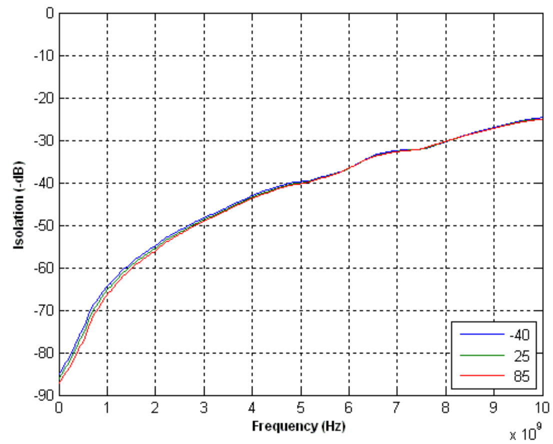


Figure 10. Isolation: RF1-RF2, RF1 Active @ 25°C

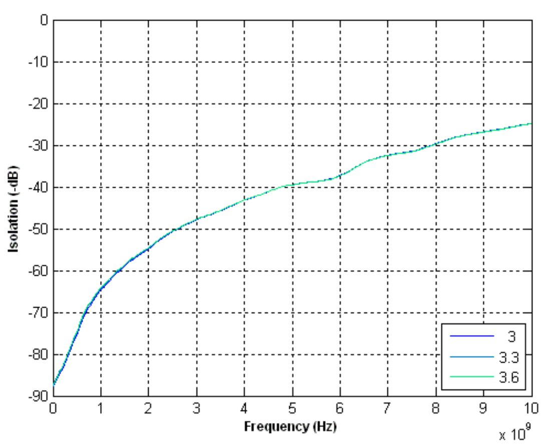


Figure 11. Isolation: RF2-RF1, RF2 Active @ 25°C

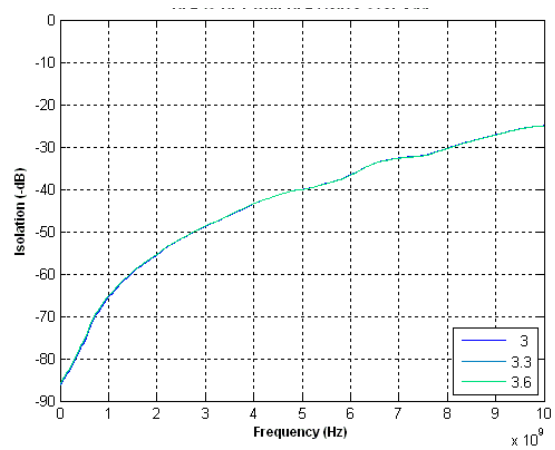


Figure 12. Isolation: RFC-RF1, RF2 Active @ V_{DD} = 3.3V

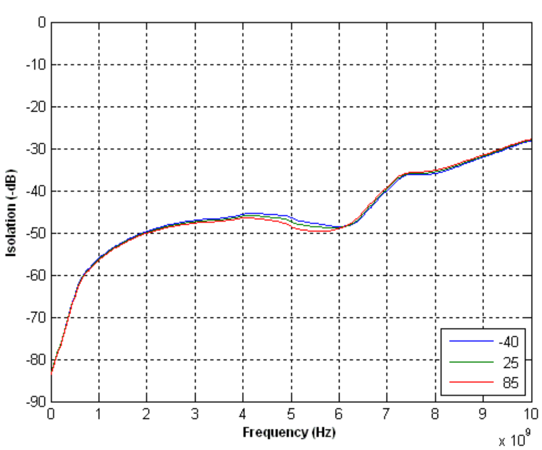
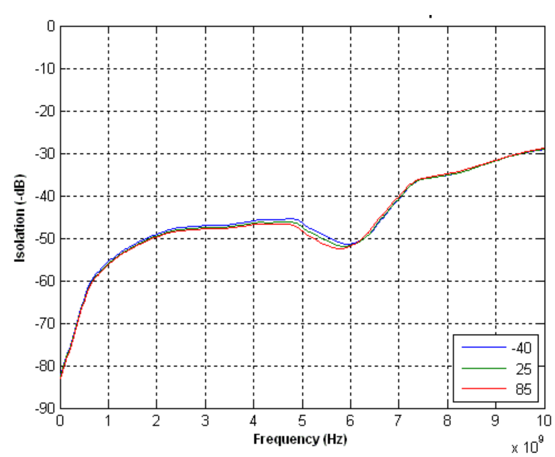


Figure 13. Isolation: RFC-RF2, RF1 Active @ V_{DD} = 3.3V



Performance Plots

Figure 14. Isolation: RFC-RF1, RF2 Active @ 25°C

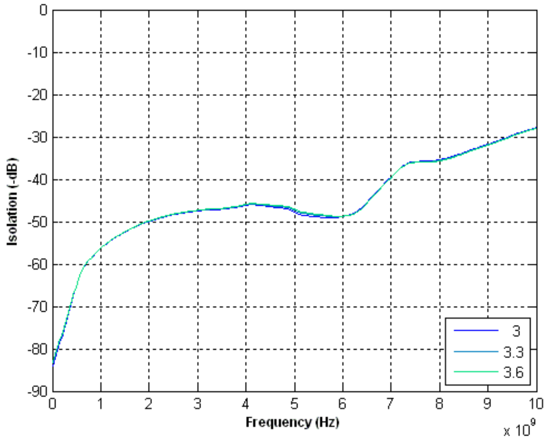


Figure 15. Isolation: RFC-RF2, RF1 Active @ 25°C

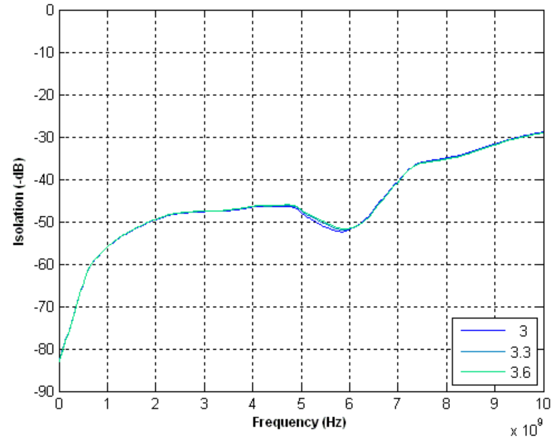


Figure 16. Isolation: RFC-RF1, OFF state @ V_{DD} = 3.3V

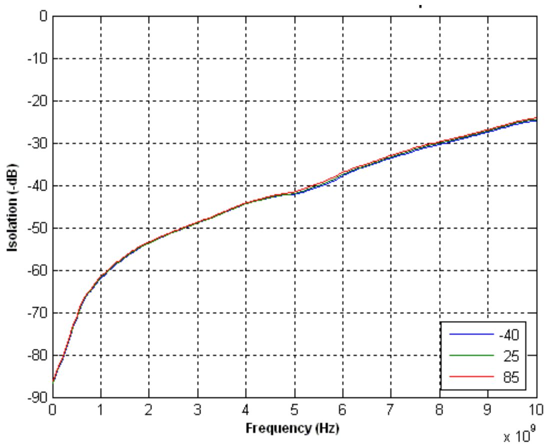


Figure 17. Isolation: RFC-RF2, OFF state @ V_{DD} = 3.3V

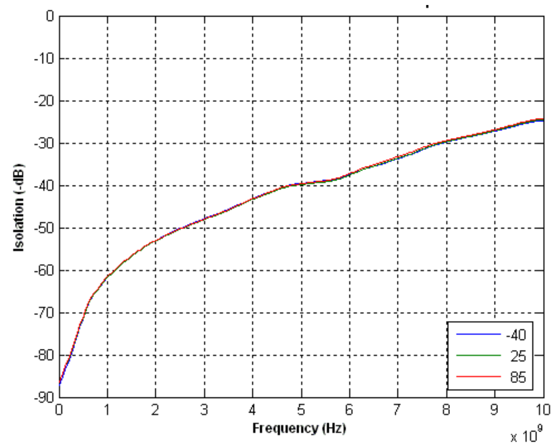


Figure 18. Isolation: RFC-RF1, OFF state @ 25°C

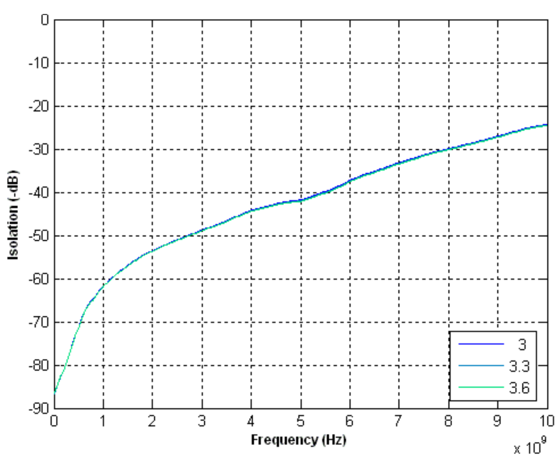
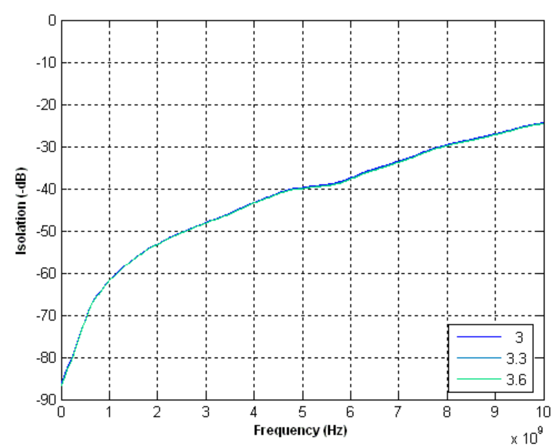


Figure 19. Isolation: RFC-RF2, OFF state @ 25°C



Performance Plots

Figure 20. Return Loss: RF1 @ V_{DD} = 3.3V

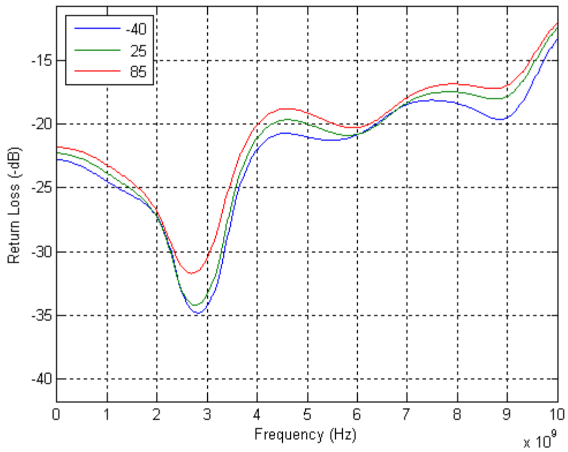


Figure 21. Return Loss: RF2 @ V_{DD} = 3.3V

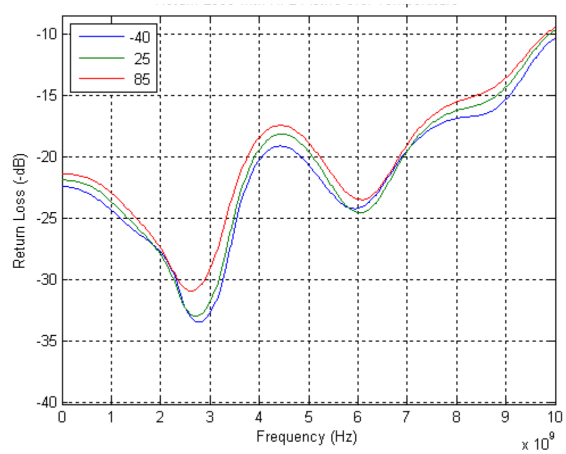


Figure 22. Return Loss: RF1 @ 25°C

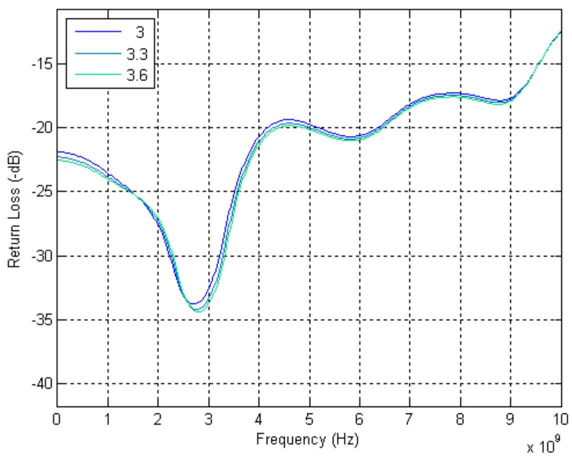
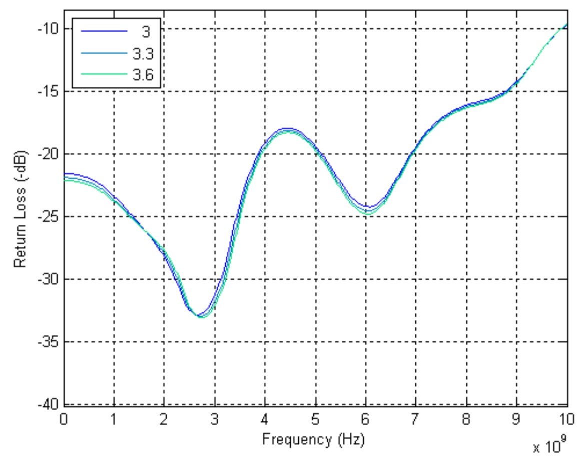


Figure 23. Return Loss: RF2 @ 25°C



Evaluation Board

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE95420. The RF common port is connected through a 50 Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50 Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50 Ω transmission is available via SMA connectors J5 and J6. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The evaluation kit board is constructed of four metal layers. The dual clad top RF layer is Rogers RO4003 material with an 8 mil RF core and er = 3.55. The other two dielectric layers are FR4 for DC control and overall board strength with an cumulative board thickness of 62 mils. The RF transmission lines were designed using a Grounded co-planar waveguide with a linewidth of 15 mils and gap of 7 mils.

Figure 24. Evaluation Board Layout

Peregrine Specification 101-0345

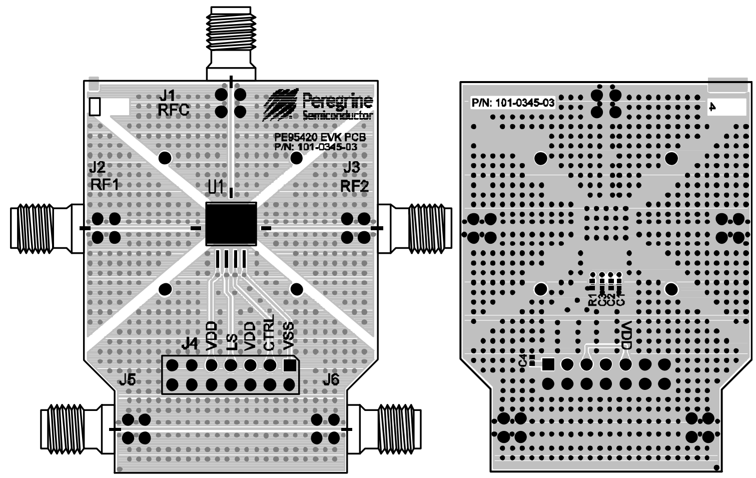


Figure 25. Evaluation Kit Schematic

Peregrine Specification 102-0417

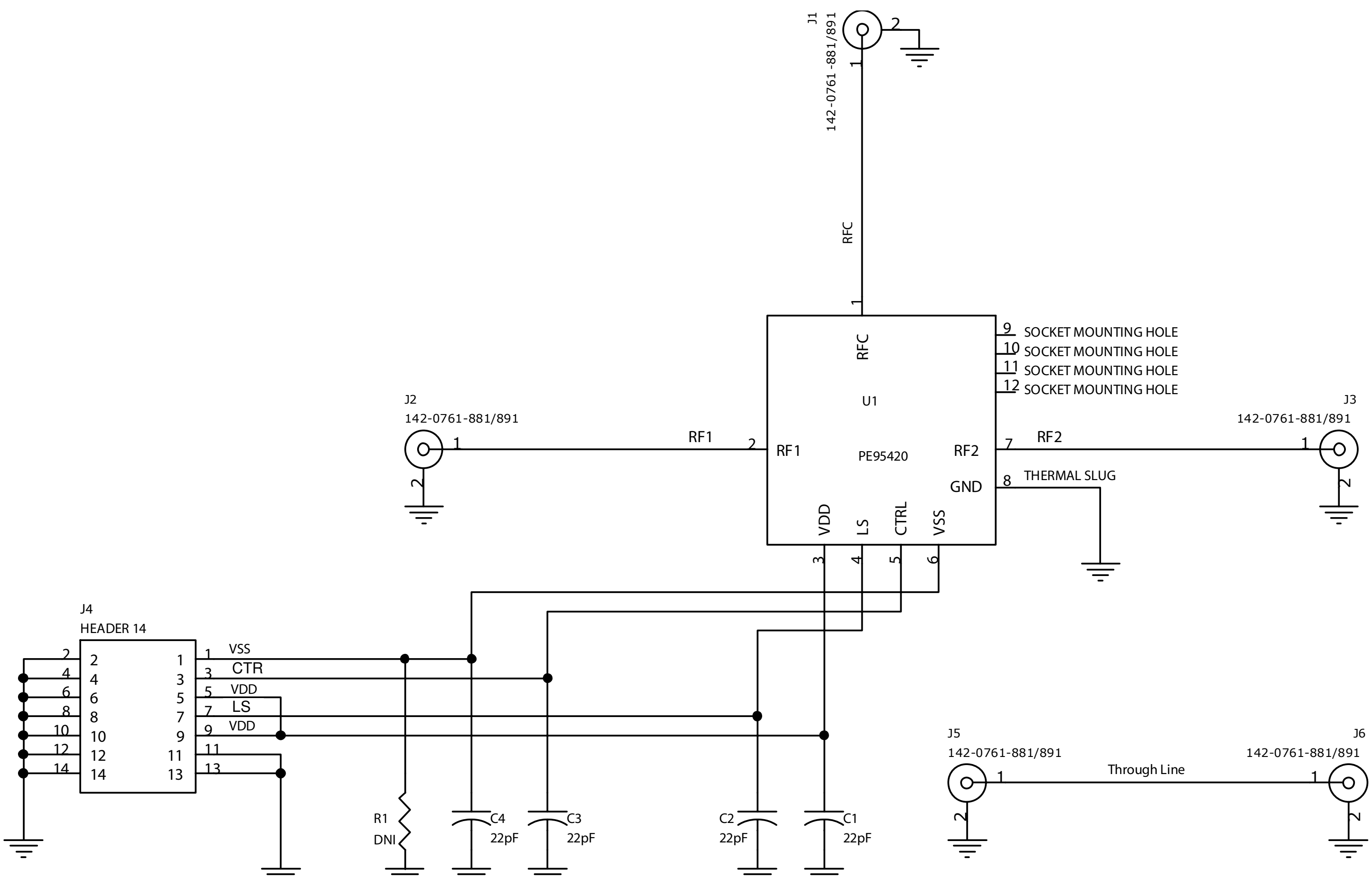
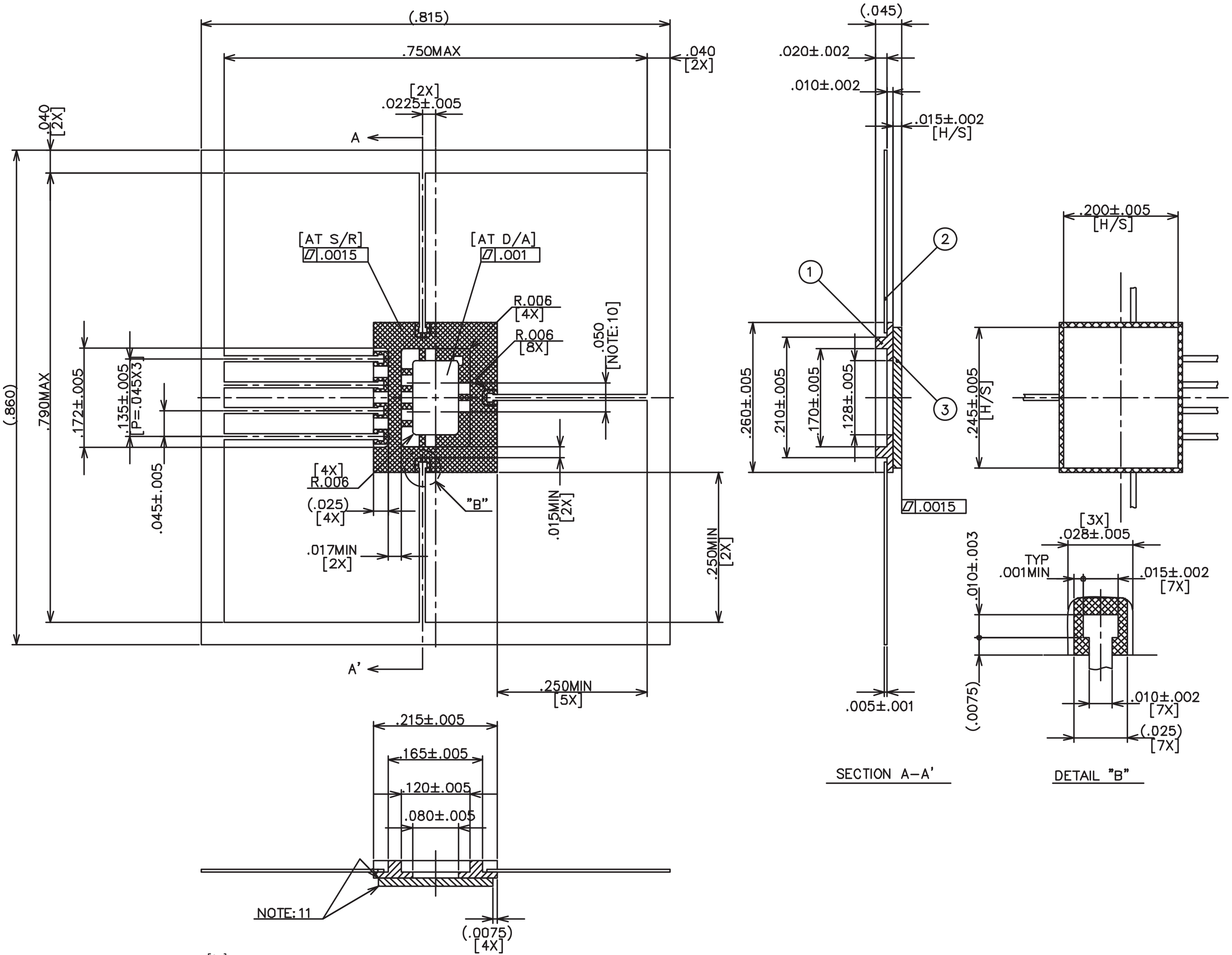
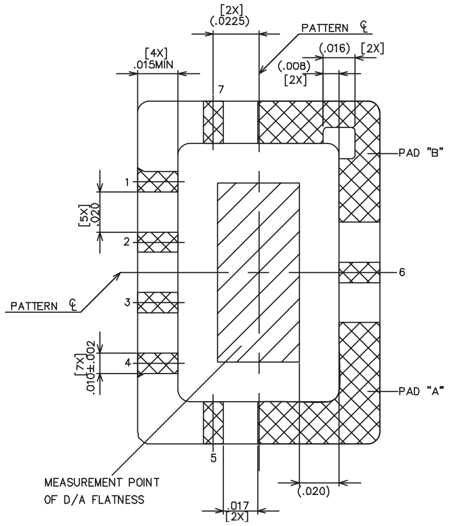


Figure 26. Package Drawing

7-lead CSOIC

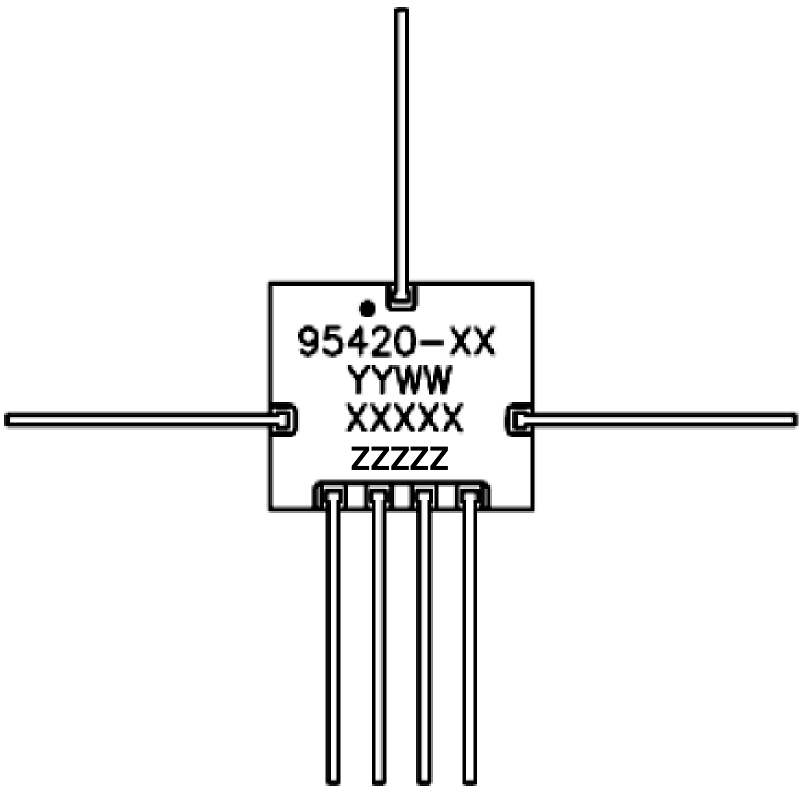




NOTES:

1. GOLD PLATE 50~225? INCHES OVER 75~225? INCHES NICKEL.(MEASUREMENT POINT AT LEAD)
2. VIAS ARE SOLID TUNGSTEN WHICH MAKE ELECTRICAL CONNECTION BETWEEN CERAMIC–1/CERAMIC–2 TOP METALLIZATION AND BASE.
3. METALLIZATION SHALL BE WITHIN A PULL–BACK OF .001 MAX AND A RUN–DOWN OF .005 MAX.
4. BRAZE FILLET MAY NOT EXTEND INTO CAVITY MORE THAN .007. .001MAX THICKNESS FILM BRAZE IS ACCEPTABLE INTO CAVITY.
5. VIA MISALIGNMENT BETWEEN CERAMIC–1 AND CERAMIC–2 SHALL BE .003 MAX.
6. A SINGLE .008MAX DIAMETER VOID IN PLATING (FROM PLATING JIG CONTACT) IS ACCEPTABLE IN DIE ATTACH CAVITY OUTSIDE OF INDICATED DIMENSION.
7. EDGE "R" IS ACCEPTABLE ON CuW BASE EDGES.
8. S/R TO BE ELECTRICALLY CONNECTED TO THE B/G "A","B" & H/S.
9. TOLERANCE TO BE NOT LESS THAN ±.005 INCH UNLESS OTHERWISE SPECIFIED OF DRAWING.
10. NTK SPECIFICATION YS–1026 SHALL APPLY.

Figure 27. Top Marking



95420-XX= Part number e.g. 95420-11
XX will be specified by the PO and/or the Assembly Instructions
YYWW= Date Code-Last 2 digits of the year and work week
XXXXX = Lot Code
ZZZZZ = Serial Number

• = Pin 1 mark

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
95420-01	95420-01	PE95420-7CSOIC-50B Engineering Samples	7-lead CSOIC	50 Count Trays
95420-11	95420-11	PE95420-7CSOIC-50B Production Units	7-lead CSOIC	50 Count Trays
95420-99		Production Die	Die	400 Units/Waffle Pack
95420-00	PE95420-EK	PE95420 Evaluation Kit	Evaluation Board	1 / Box

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For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

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