XR1008-QB

Receiver
35 - 45 GHz

Rev. V1

Features

- Sub-harmonic, Image Reject Receiver
- Integrated LNA, Image Reject Mixer, LO Doubler/ Buffer
- +2.0 dBm LO Drive Level
- 10.0 dB Conversion Gain
- 3.5 dB NF
- +5.0 dBm Input Third Order Intercept (IIP3)
- Lead-Free 7mm 28-lead SMD Package
- 100% RF and DC Testing
- RoHS* Compliant and 260°C Reflow Compatible

Description

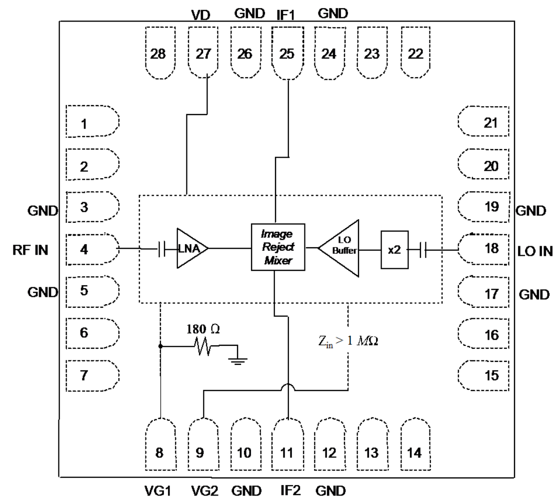
The XR1008-QB is a 35.0-45.0 GHz packaged receiver that has a noise figure of 3.5 dB and 5.0 dBm Input Third Order Intercept across the band. This device integrates a three stage LNA followed by an image reject resistive pHEMT mixer and includes an integrated LO doubler and buffer amplifier. The use of integrated LO doubler and LO buffer amplifier makes the provision of the LO easier than for fundamental mixers at these frequencies. I and Q mixer outputs are provided and an external 90 degree hybrid is required to select the desired sideband.

The device comes in a 7x7mm SMT package that is RoHS compliant. This device has been designed for use in 38/42 GHz Point-to-Point Microwave Radio applications.

Ordering Information

Part Number	Package
XR1008-QB-0N00	bulk quantity
XR1008-QB-0N0T	tape and reel
XR1008-QB-EV1	evaluation module

Functional Schematic



Pin Configuration[1]

Pin No.	Function	Pin No.	Function
3	Ground	17	Ground
4	RF Input	18	LO Input
5	Ground	19	Ground
8	VG1	24	Ground
9	VG2	25	IF1 Output
10	Ground	26	Ground
11	IF2 Output	27	Drain Bias
12	Ground	All others	Not Connected

1. The exposed pad centered on the package bottom must be connected to RF and DC ground.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

Electrical Specifications[2]: 35-45 GHz (Ambient Temperature T = 25°C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (LO)	GHz	16.0	-	24.0
Frequency Range (IF)	GHz	DC	-	4.0
Input Return Loss (S11)	dB	-	10.0	-
Conversion Gain RF/IF (S21) (LSB/USB) [IF=2 GHz]	dB	8.0/9.5	9.0/10.0	-
Conversion Gain RF/IF (S21) (LSB/USB) [IF=3.5 GHz]	dB	6.8/8.3	7.8/8.8	-
LO Input Drive (P_{LO})	dBm	0.0	+2.0	+8.0
Image Rejection [IF=2 GHz]	dBc	15.0	-	-
Image Rejection [IF=3.5 GHz]	dBc	13.0	-	-
Noise Figure (NF) (LSB/USB) [IF=2 GHz]	dB	-	3.5/3.5	4.6/4.3
Noise Figure (NF) (LSB/USB) [IF=3.5 GHz]	dB	-	4.0/4.0	5.1/4.8
Isolation LO/RF @ LOx1/LOx2	dB	-	40.0/40.0	-
Input Third Order Intercept Point (IIP3)	dBm	0.0	+5.0	-
Input 1 dB Compression (IP1dB)	dBm	-	-5.0	-
Drain Bias Voltage (Vd)	VDC	-	4.0	4.0
Gate Bias Voltage (Vg1,2)	VDC	-1.0	-0.5	-0.1
Supply Current (Id) (Vd=4.0, Vg=-0.5V Typical)	mA	-	180	240

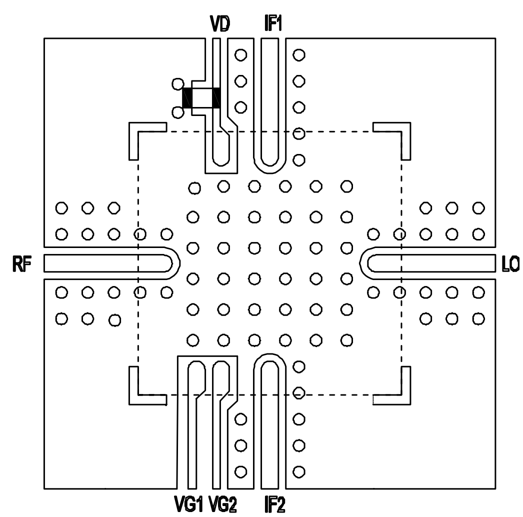
2. Performance limits guaranteed over the frequency range 37.0-40.15 GHz

Absolute Maximum Ratings [3]

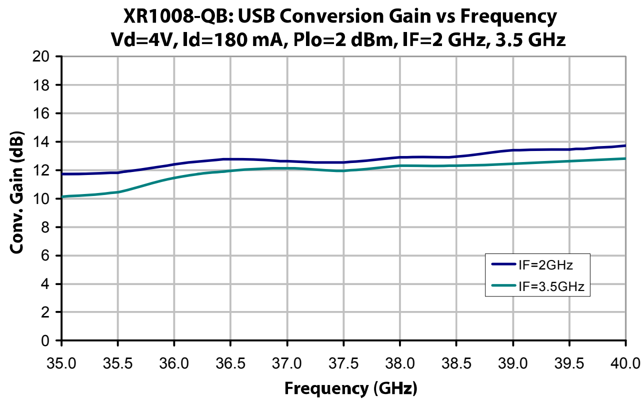
Parameter	Absolute Max.
Supply Voltage (Vd)	+4.3 VDC
Supply Current (Id)	300 mA
Gate Bias Voltage (Vg)	-1.5V < Vg < 0V
Input Power (Pin)	+5 dBm
Storage Temperature (Tstg)	-65 ºC to +165 ºC
Operating Temperature (Ta)	-55 ºC to +85 ºC
Channel Temperature (Tch)	175 ºC
ESD - Human Body Model	Class 1A
ESD - Machine Body Model	Class A
Moisture Sensitivity Level	MSL3

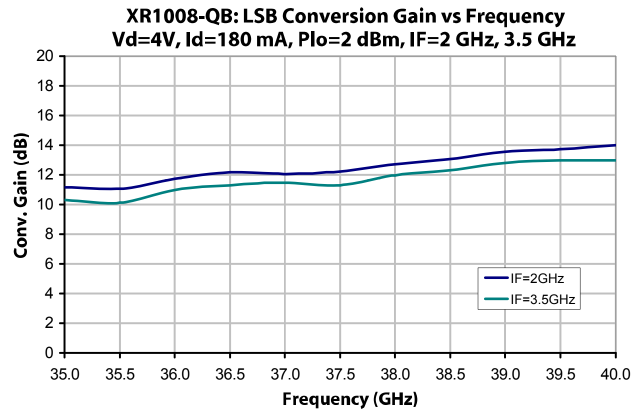
3. Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life

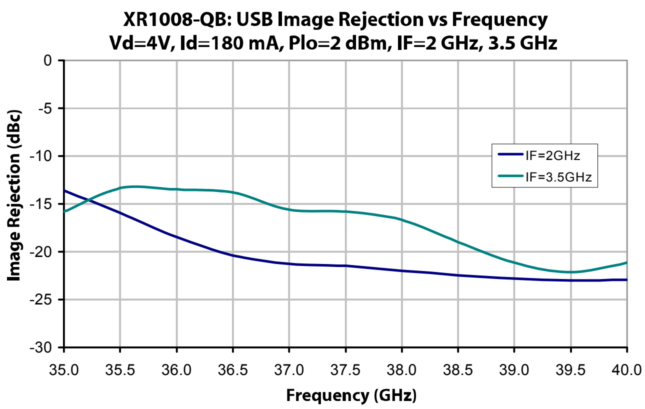
Recommended Layout

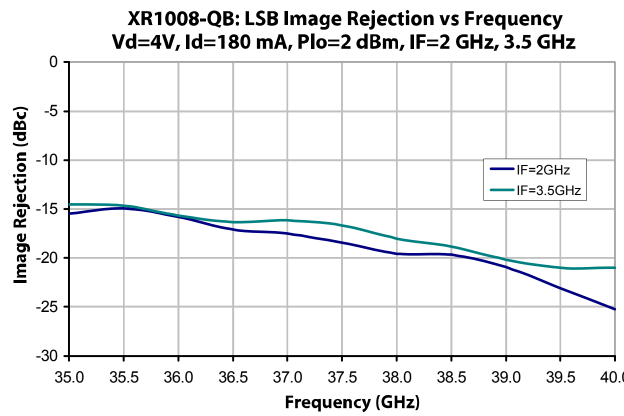


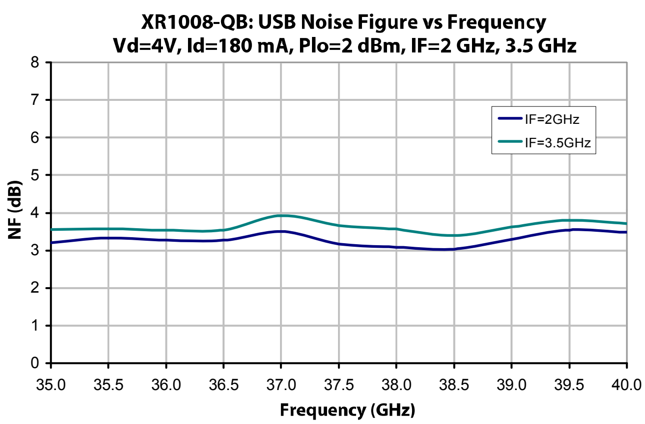
Typical Performance Curves

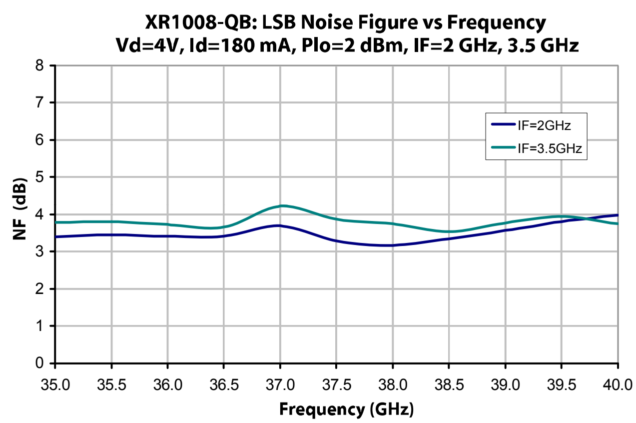




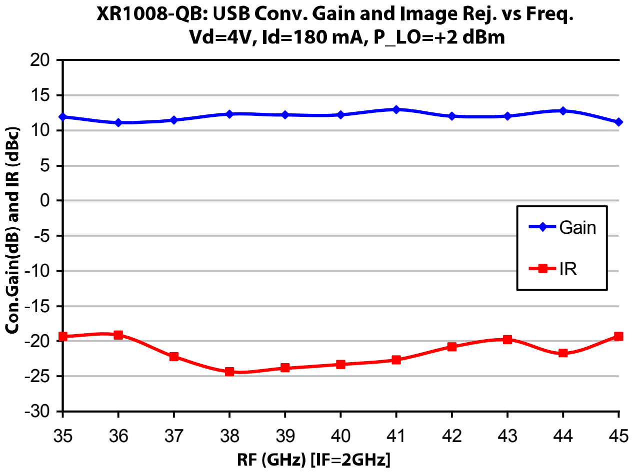


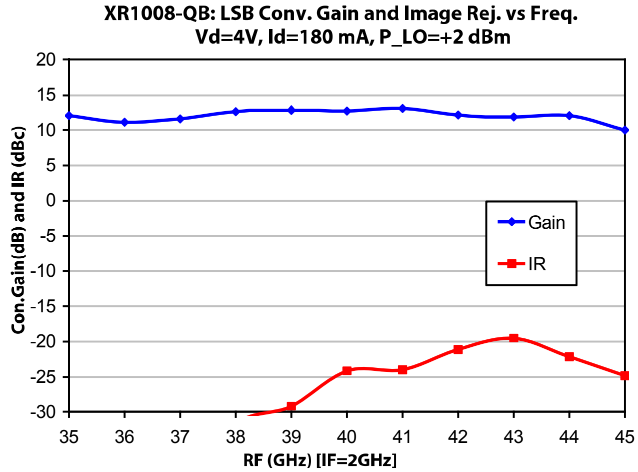






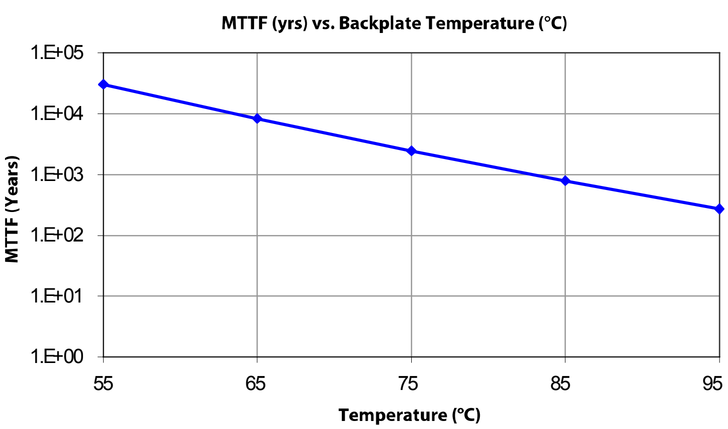
Typical Performance Curves (cont.)





MTTF

MTTF is calculated from accelerated life-time data of single devices and assumes an isothermal back-plate.

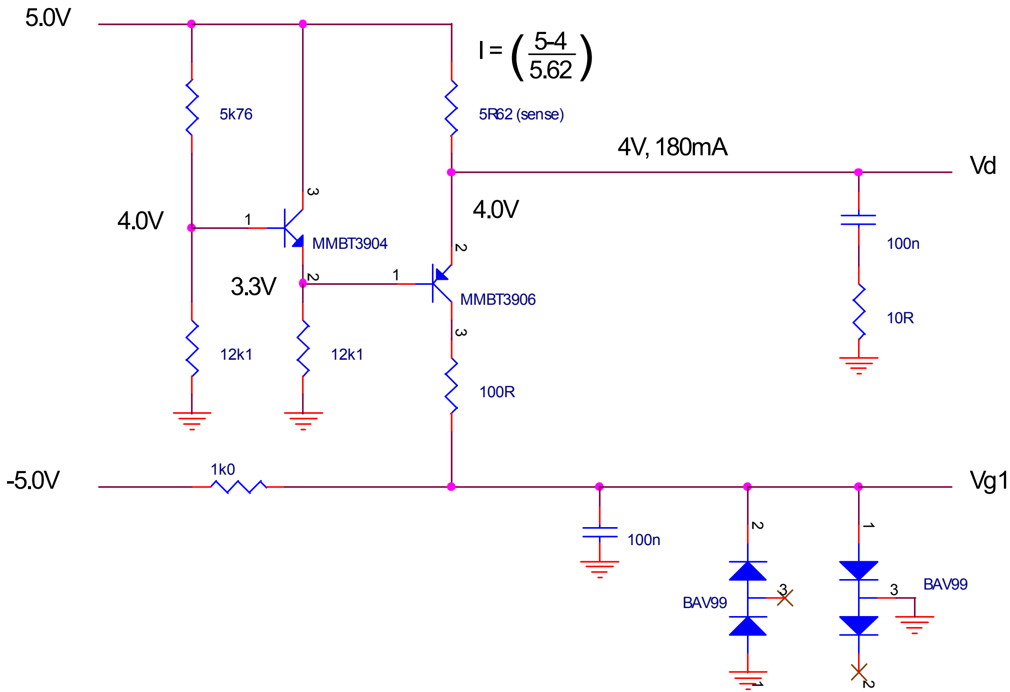


Bias Conditions: Vd=4.0V, Id=180 mA

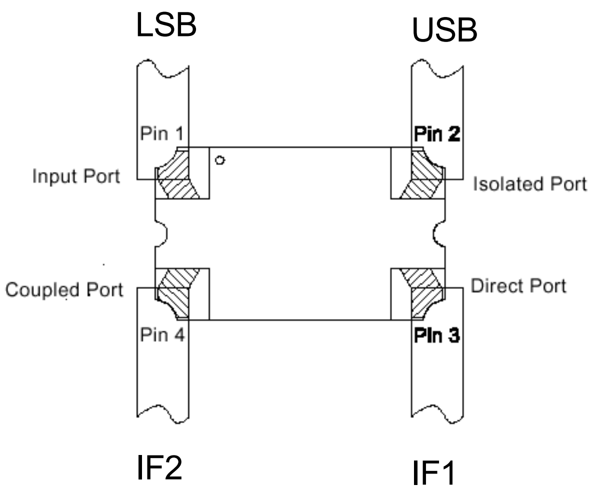
App Note [1] Biasing - Please refer to the functional block diagram and pin-out table for biasing information. The device is operated by biasing VD=4.0 V with ID=180 mA by adjusting the applied voltage on VG1. VG1 typically requires-0.5 V to result in the drain current being 180 mA. The nominal input impedance of this gate is 180 Ω, so it should be noted that the nominal gate current will be 2.7 mA.

Additionally, a fixed bias of VG2=-0.5 V is required to bias the mixer and doubler. Adjusting VG2 above or below this value can adversely affect conversion gain, image rejection and intercept point performance. It is recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. The diagram “Active Bias Circuit” demonstrates a possible method for active biasing. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

Active Bias Circuit



App Note [3] USB/LSB Selection - Please refer to the functional block diagram and pin-out table for biasing information. The device is operated by biasing VD=4.0 V with ID=180 mA by adjusting the applied voltage on VG1.



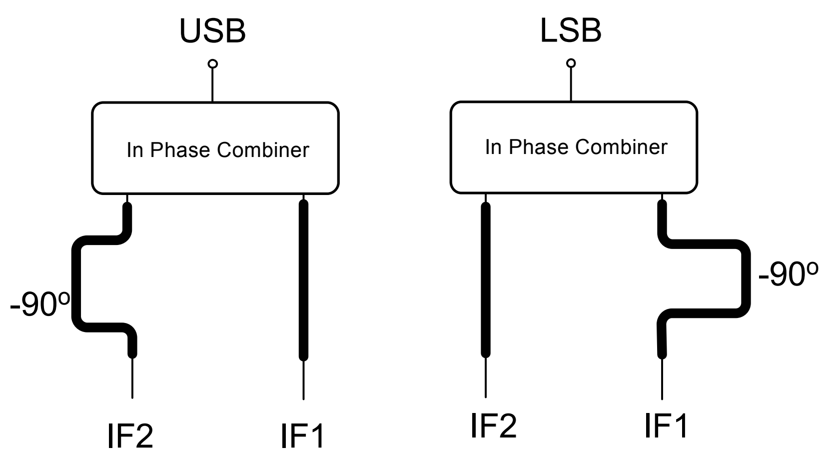
For Upper Side Band operation (USB):

With IF1 and IF2 connected to the direct port (0º) and coupled port (90º) respectively as shown in the diagram, the USB signal will reside on the isolated port. The input port must be loaded with 50 ohms.

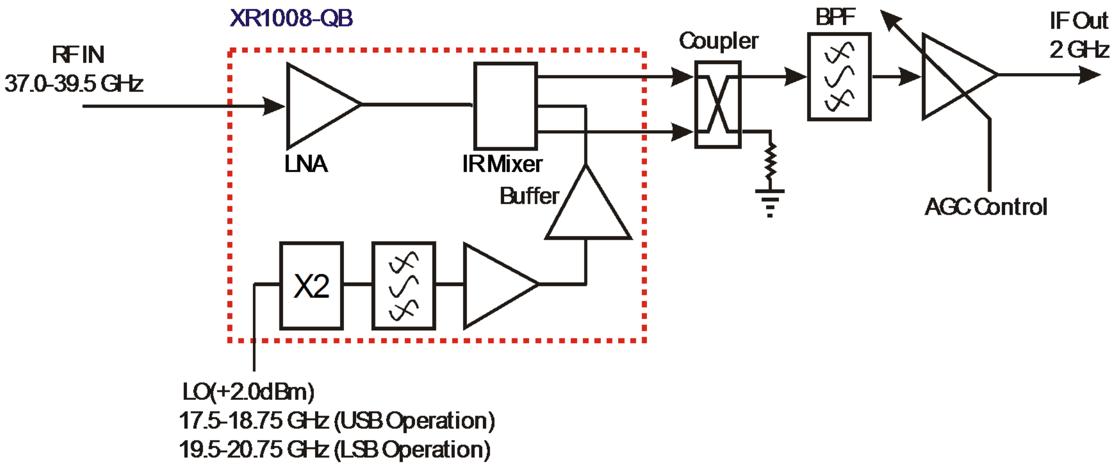
For Lower Side Band operation (LSB):

With IF1 and IF2 connected to the direct port (0º) and coupled port (90º) respectively as shown in the diagram, the LSB signal will reside on the input port. The isolated port must be loaded with 50 ohms.

An alternate method of Selection of USB or LSB:



Typical Application

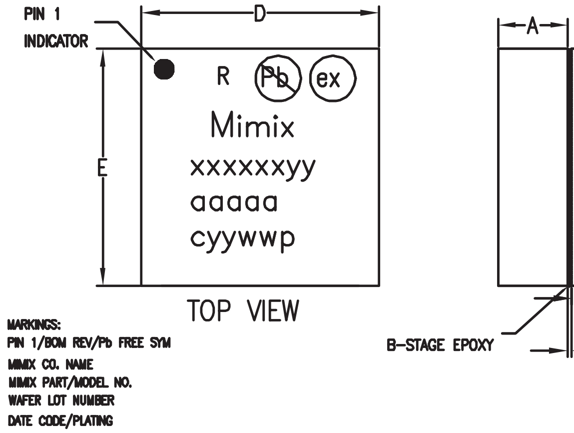


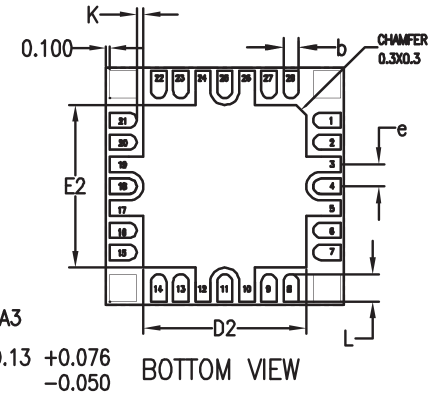
MMIC-based 35.0-45.0 GHz Receiver Block Diagram
(Changing LO and IF frequencies as required allows design to operate as high as 46 GHz)

This 30.0-46.0 GHz XR1008-QB GaAs MMIC Receiver can be used in saturated radio applications and linear modulation schemes up to 128 QAM.

Lead-Free 7 mm 28-Lead SMD†

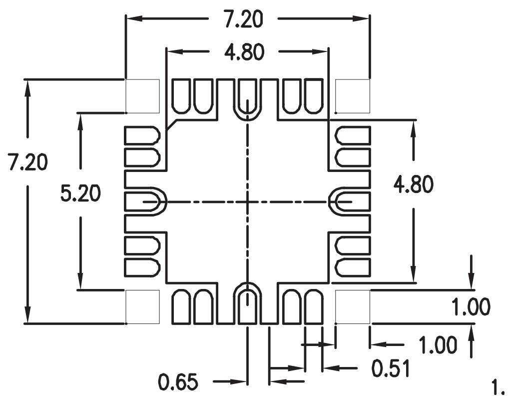
QB - MSL, Gross Leak Test Compliant





0.13 +0.076 −0.050

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTES:
1. DIMENSIONS ARE IN MM.

	MIN	TYP	MAX
A	1.20	1.25	1.30
A3	0.10 – 0.20		REF
b	0.40	0.45	0.50
K	–	0.20	–
D	7.00 BSC		
E	7.00 BSC		
e	0.65		
D2	4.75	4.80	4.85
E2	4.75	4.80	4.85
L	0.75	0.80	0.85

1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Plating is 100% matte tin over copper.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.