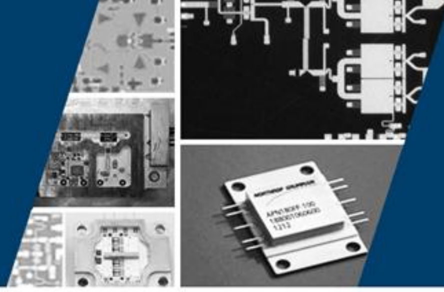
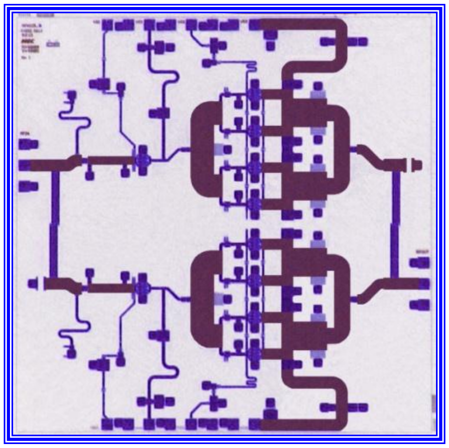
APN228
27-31 GHz
GaN Power Amplifier



NORTHROP GRUMMAN

Advance Datasheet

Revision: May 2014



X = 4.0mm Y = 4.0mm

Applications

- Point-to-Point Digital Radios
- Point-to-Multipoint Digital Radios
- SatCom Terminals

Product Description

The APN228 monolithic GaN HEMT amplifier is a broadband, two-stage power device, designed for use in SatCom Terminals and point-to-point digital radios. To ensure rugged and reliable operation, HEMT devices are fully passivated. Both bond pad and backside metallization are Au-based that is compatible with epoxy and eutectic die attach methods.

Product Features

- RF frequency: 27 to 31 GHz
- Linear Gain: 19.5 dB typ.
- Psat: 41.2 dBm typ.
- Die Size: 16 sq. mm.
- 0.2um GaN HEMT Process
- 4 mil SiC substrate
- DC Power: 28 VDC @ 1.2 A

Performance Characteristics (Ta = 25°C)

Specification	Min	Typ	Max	Unit
Frequency	27		31	GHz
Linear Gain	18	19.5		dB
Input Return Loss	17	24		dB
Output Return Loss	14	20		dB
P1db		39		dBm
Psat	40	41.2		dBm
PAE @ Psat		27		%
Vd1=Vg1a, Vd2=Vd2a		28		V
Vg1. Vg1a		-3.5		V
Vg2, Vg2a		-3.5		V
Id1+Id1a		240		mA
Id2+Id2a		960		mA

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Min	Max	Unit
Vd1=Vg1a ,Vd2=Vd2a	20	28	V
Id1+Id1a		240	mA
Id2+Id2a		960	mA
Vg1, Vg1a, Vg2, Vg2a	-5	0	V
Input drive level		TBD	dBm
Assy. Temperature (TBD seconds)		300	deg. C

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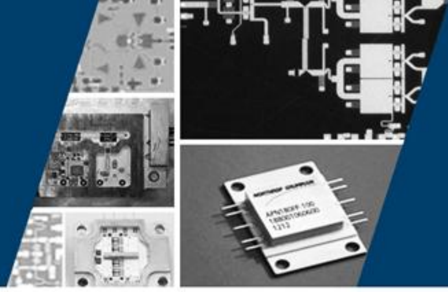
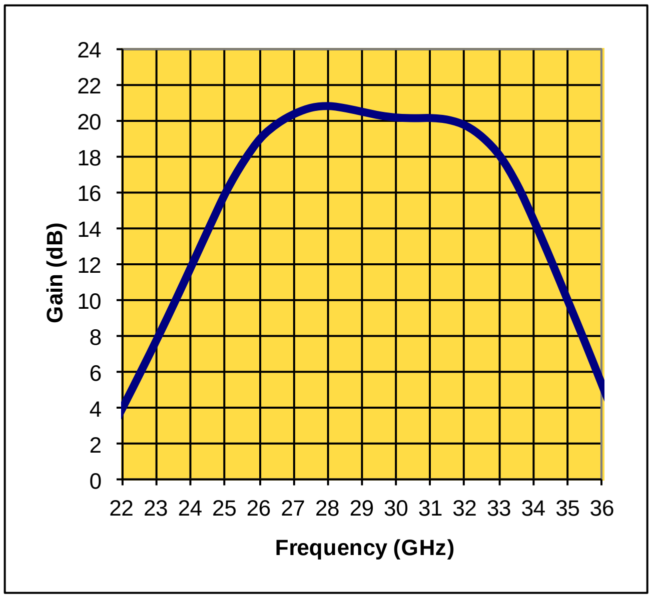
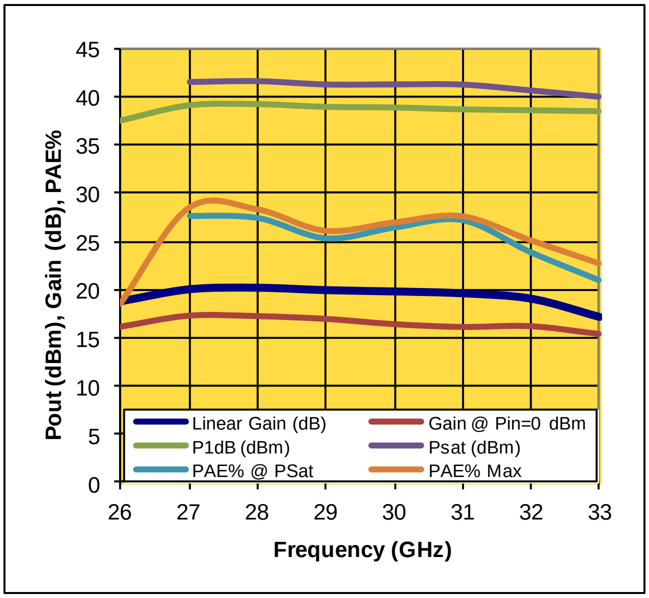


Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240 mA, Id2 + Id2a = 960 mA

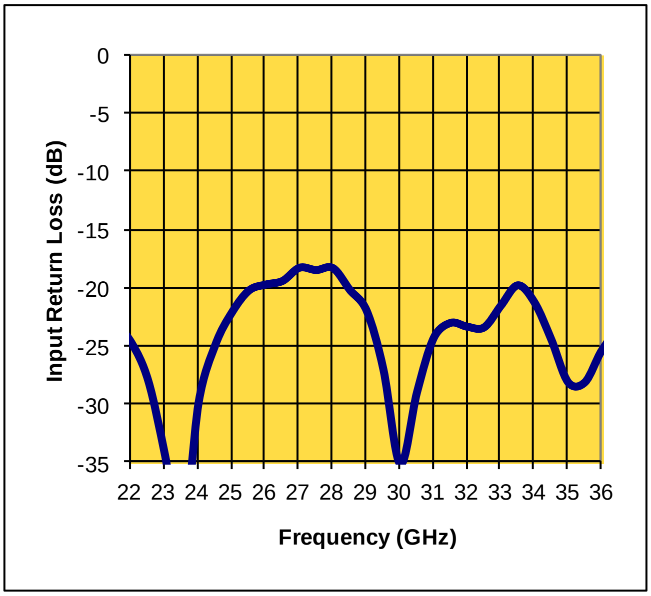
Linear Gain vs. Frequency *



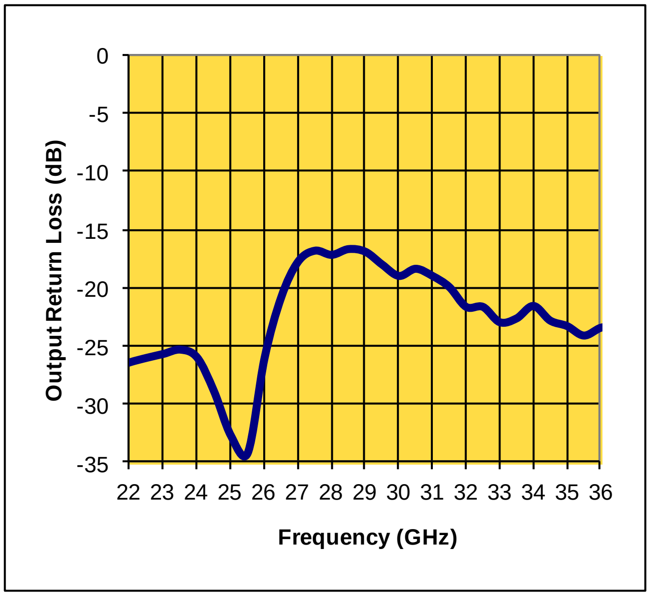
Power, Gain, PAE% vs. Frequency **



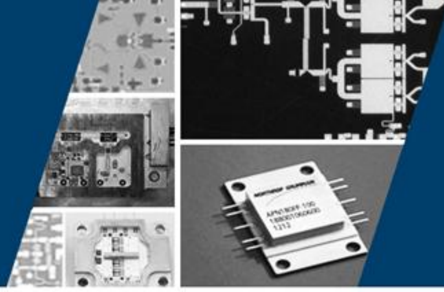
Input Return Loss vs. Frequency *



Output Return Loss vs. Frequency *



* Pulsed-Power On-Wafer , ** CW Fixtured



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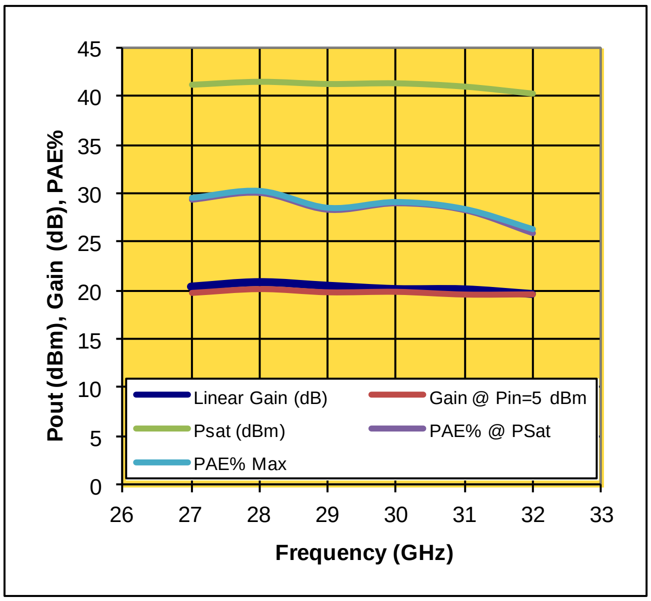
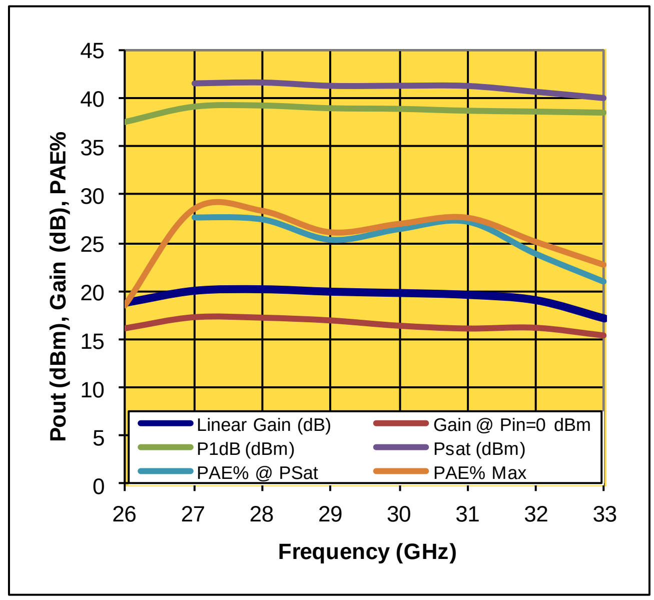
Measured Performance Characteristics (Typical Performance at 25°C)

Vd = 28.0 V, Id1 + Id1a = 240 mA, Id2 + Id2a = 960 mA

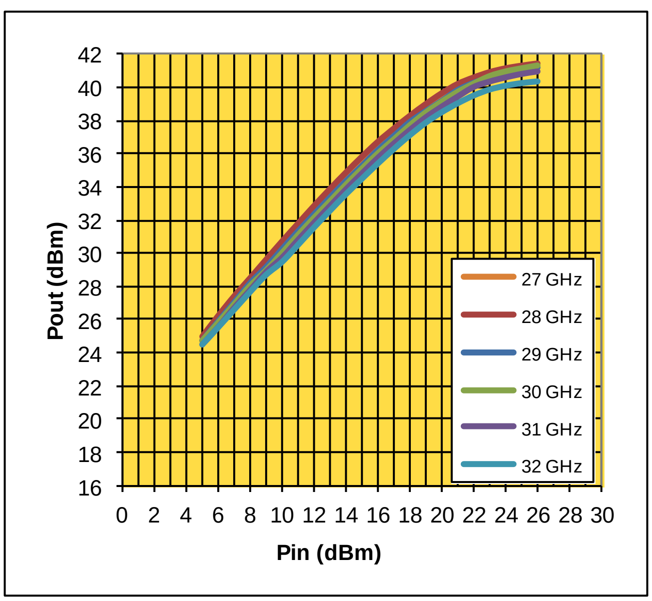
Power, Gain, PAE% vs. Frequency
Pulsed-Power On-Wafer



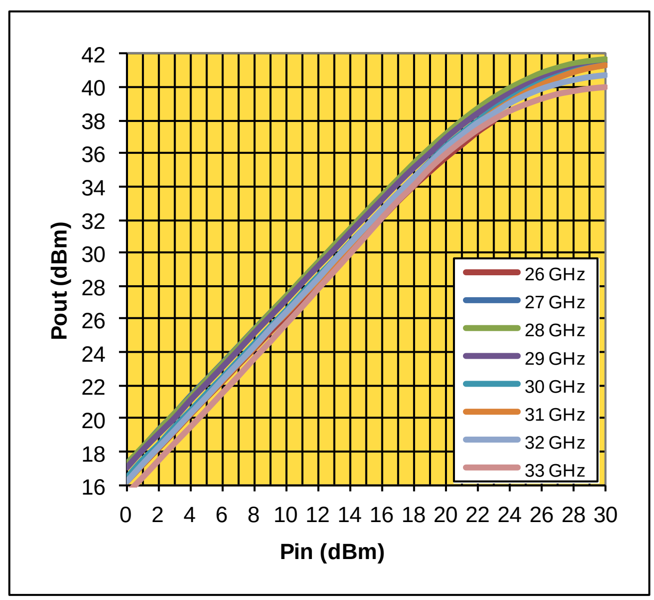
Power, Gain, PAE% vs. Frequency
CW Fixtured



Output Power vs. Input Power
Pulsed-Power On-Wafer



Output Power vs. Input Power
CW Fixtured



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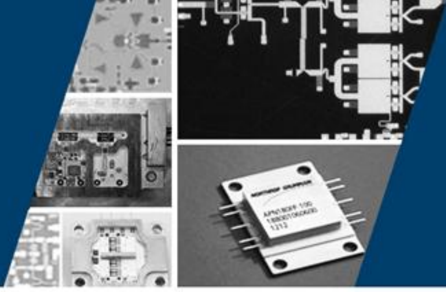
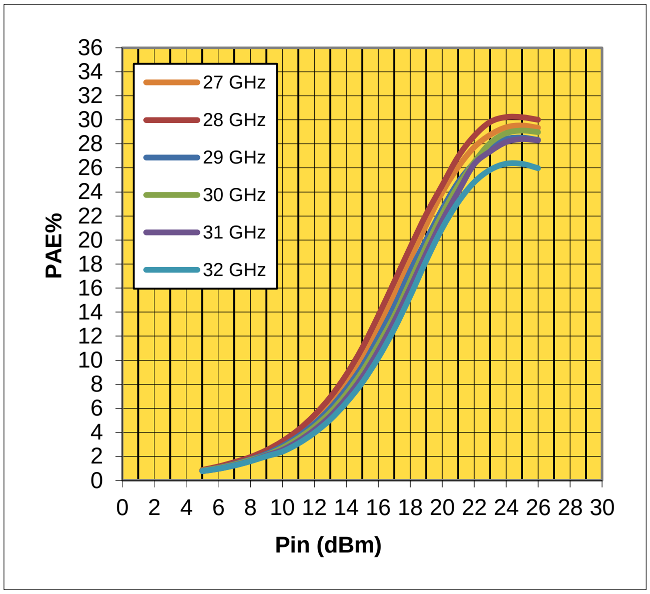
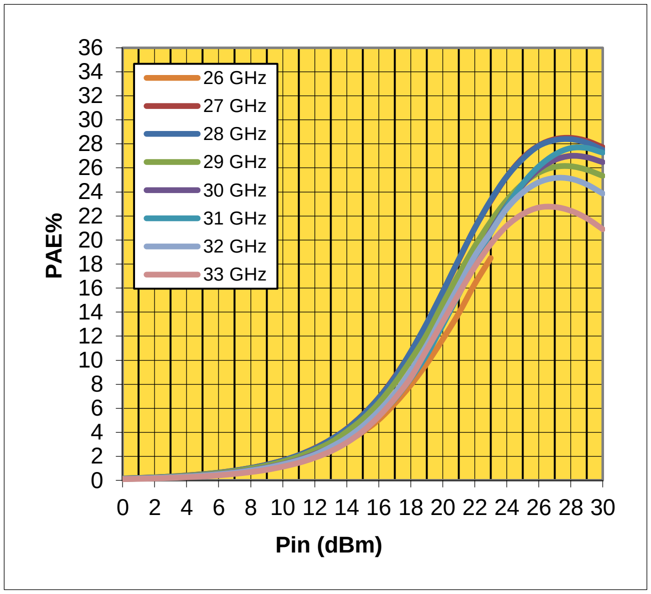


Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240 mA, Id2 + Id2a = 960 mA

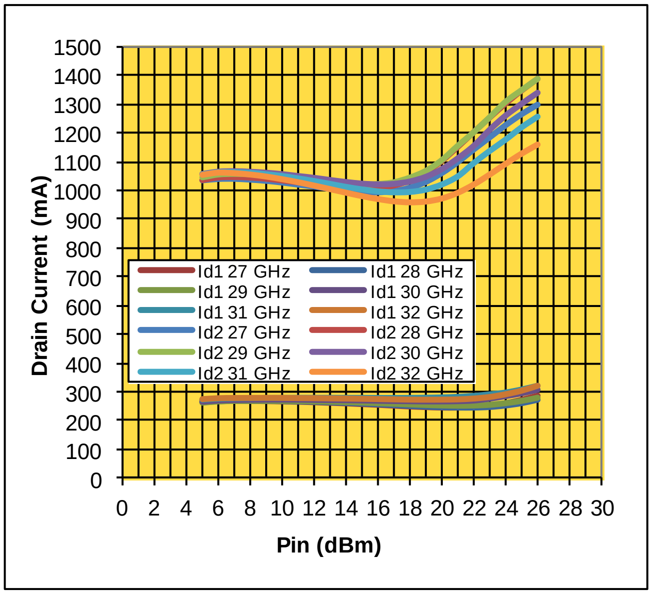
PAE% vs. Input Power
Pulsed-Power On-Wafer



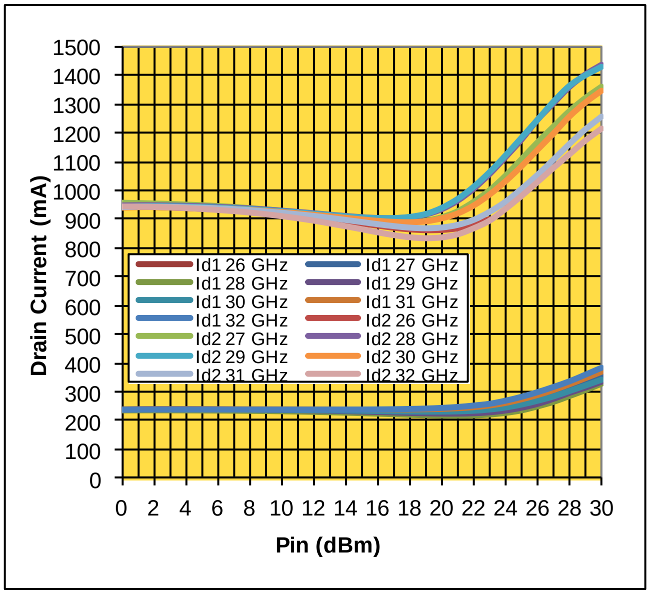
PAE% vs. Input Power
CW Fixtured



Stage Currents vs. Input Power
Pulsed-Power On-Wafer



Stage Currents vs. Input Power
CW Fixtured



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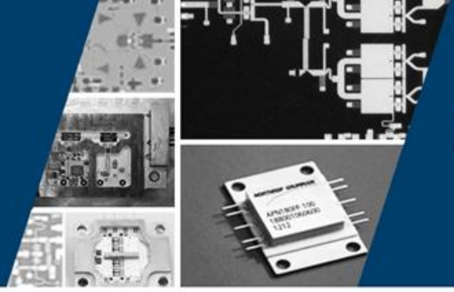
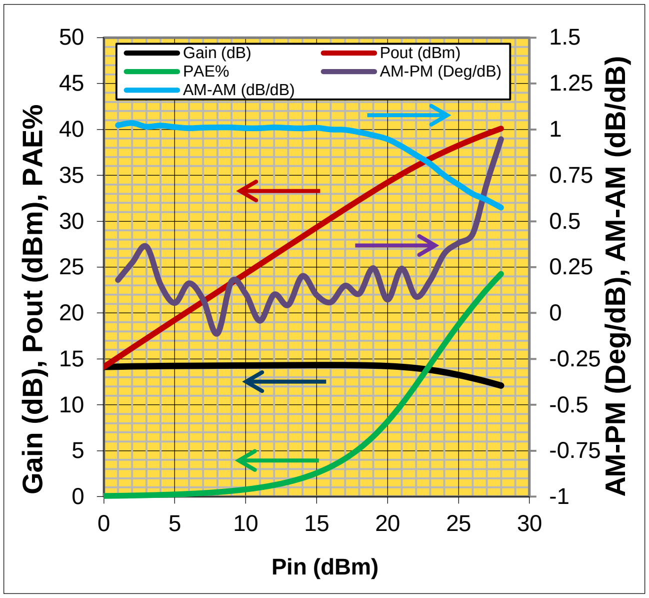
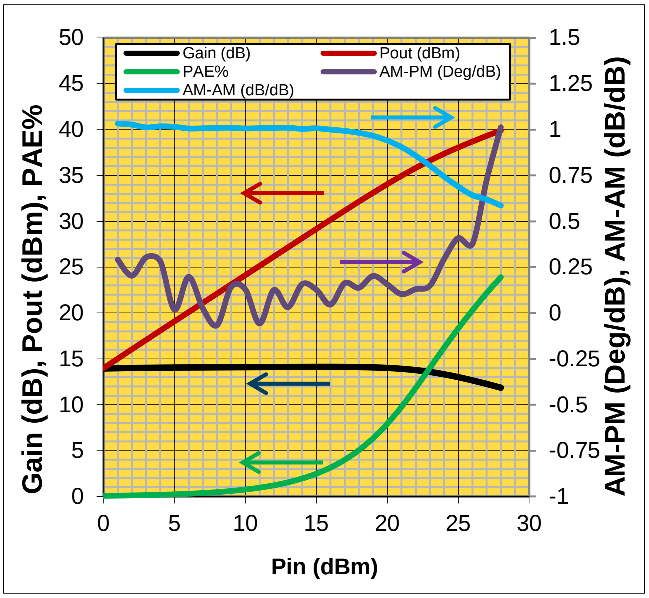


Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240 mA, Id2 + Id2a = 960 mA

CW Fixtured Gain, Pout. PAE%,
AM-AM & AM-PM vs. Pin @ 29 GHz *



CW Fixtured Gain, Pout. PAE%,
AM-AM & AM-PM vs. Pin @ 30 GHz *



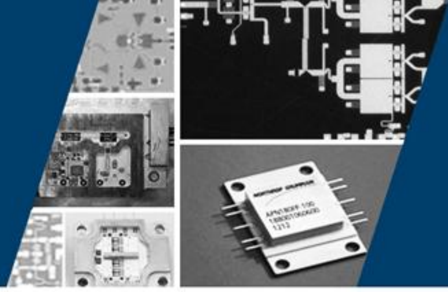
* In un-calibrated fixture with 2-tone input

Thermal Properties

Preliminary Thermal Properties with die mounted with 1mil 80/20 AuSn Eutectic to 25mil CuW Shim.

Conditions	Shim Boundary Temperature	Junction Temperature Tjc	Thermal Resistance θjc
Vd = 28V	25 ºC	180.4 ºC	4.4 ºC/W
Id1 + Id1a = 345.6 mA *	38 ºC	200.0 ºC **	4.6 ºC/W
Id2 + Id2a = 1380 mA *	50 ºC	219.2 ºC	4.8 ºC/W
Pin=28.94 dBm			
Pout=41.18 dBm			

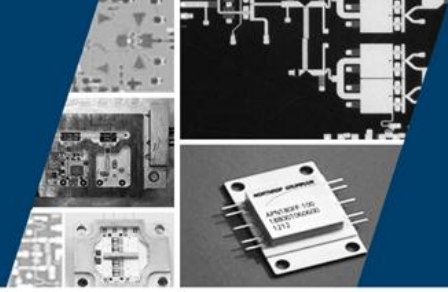
* Vd = 28.0 V, Idq1 = 240 mA, Id2q = 960 mA
** Max recommended. Pre-qualification reliability testing indicates that MTTF in excess of 10^5 hours can be achieved by ensuring Tjc is kept below 200ºC.



Measured Performance Characteristics (Typical Performance at 25°C)
Vd = 28.0 V, Id1 + Id1a = 240 mA, Id2 + Id2a = 960 mA *

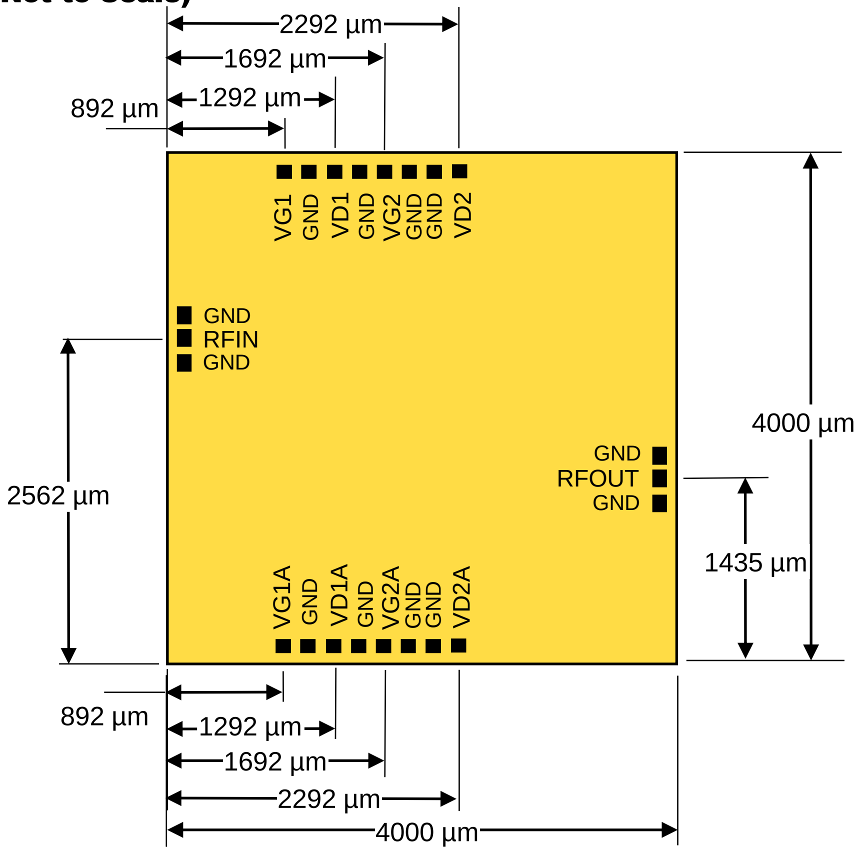
Freq GHz	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang
21.0	0.073	140.736	1.038	83.349	0.006	-178.738	0.024	-19.159
21.5	0.070	120.733	1.275	63.805	0.006	139.168	0.043	-23.300
22.0	0.047	100.323	1.537	45.035	0.009	-59.362	0.041	-42.268
22.5	0.048	93.133	1.910	24.396	0.007	-39.020	0.055	-71.525
23.0	0.033	50.584	2.396	3.260	0.010	-61.427	0.075	-92.131
23.5	0.003	118.778	2.964	-18.492	0.011	-6.034	0.070	-111.220
24.0	0.013	-117.419	3.734	-42.187	0.010	-92.575	0.066	-142.797
24.5	0.043	-120.919	4.691	-67.738	0.008	22.499	0.061	-165.432
25.0	0.053	-137.959	5.837	-95.260	0.008	-22.586	0.025	159.514
25.5	0.039	-148.517	7.069	-124.632	0.008	-32.580	0.036	-20.978
26.0	0.070	-168.507	8.368	-156.630	0.012	80.611	0.078	-58.790
26.5	0.095	174.073	9.310	170.814	0.014	73.342	0.105	-88.050
27.0	0.074	157.969	9.877	138.106	0.003	173.492	0.144	-98.724
27.5	0.098	143.460	10.165	106.596	0.012	-26.439	0.188	-131.428
28.0	0.117	125.100	10.207	75.665	0.016	-39.899	0.175	-154.443
28.5	0.089	114.311	9.999	46.202	0.016	-62.256	0.164	-175.473
29.0	0.071	98.748	9.775	17.929	0.021	-40.122	0.138	166.598
29.5	0.043	56.329	9.570	-9.187	0.016	-109.534	0.119	164.863
30.0	0.063	47.172	9.300	-36.249	0.024	-85.926	0.098	156.791
30.5	0.010	60.692	9.134	-63.091	0.002	33.569	0.100	151.182
31.0	0.012	67.196	8.975	-90.521	0.013	-74.315	0.088	136.624
31.5	0.047	171.750	9.086	-118.390	0.025	-128.080	0.045	127.158
32.0	0.019	120.205	9.016	-148.410	0.027	178.045	0.069	108.070
32.5	0.016	83.549	8.847	-179.494	0.013	71.808	0.041	125.275
33.0	0.054	-137.514	8.271	146.498	0.010	-121.660	0.056	85.961
33.5	0.074	156.014	7.349	113.022	0.017	-160.154	0.064	148.641
34.0	0.046	132.888	6.049	79.625	0.014	-106.290	0.028	112.878
34.5	0.027	55.546	4.821	49.838	0.021	120.654	0.043	33.886
35.0	0.017	146.946	3.883	20.514	0.019	101.070	0.015	-113.245
35.5	0.033	-57.825	3.075	-5.565	0.026	44.968	0.021	-57.291
36.0	0.017	62.286	2.395	-30.590	0.024	125.536	0.048	-108.437
36.5	0.057	-147.918	1.863	-55.779	0.024	-21.454	0.103	-122.307
37.0	0.035	158.791	1.425	-79.650	0.028	-55.769	0.091	-136.961

* Pulsed-Power On-Wafer



Die Size and Bond Pad Locations (Not to Scale)

X = 4000 µm ± 25 µm
Y = 4000 ± 25 µm
DC Bond Pad = 100 x 100 ± 0.5 µm
RF Bond Pad = 100 x 100 ± 0.5 µm
Chip Thickness = 101 ± 5 µm



Biasing/De-Biasing Details:

Bias for 1st stage is from top. The 2nd stages must bias up from both sides.

Listed below are some guidelines for GaN device testing and wire bonding:

a. Limit positive gate bias (G-S or G-D) to < 1V
b. Know your devices' breakdown voltages
c. Use a power supply with both voltage and current limit.
d. With the power supply off and the voltage and current levels at minimum, attach the ground lead to your test fixture.
    i. Apply negative gate voltage (-5 V) to ensure that all devices are off
    ii. Ramp up drain bias to ~10 V
    iii. Gradually increase gate bias voltage while monitoring drain current until 20% of the operating current is achieved
    iv. Ramp up drain to operating bias
    v. Gradually increase gate bias voltage while monitoring drain current until the operating current is achieved
e. To safely de-bias GaN devices, start by debiasing output amplifier stages first (if applicable):
    i. Gradually decrease drain bias to 0 V.
    ii. Gradually decrease gate bias to 0 V.
    iii. Turn off supply voltages
f. Repeat de-bias procedure for each amplifier stage

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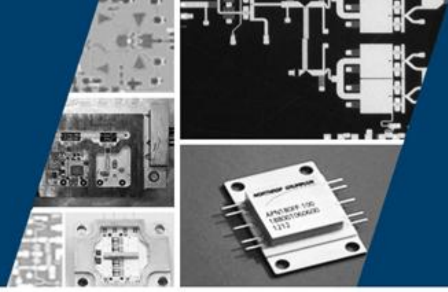

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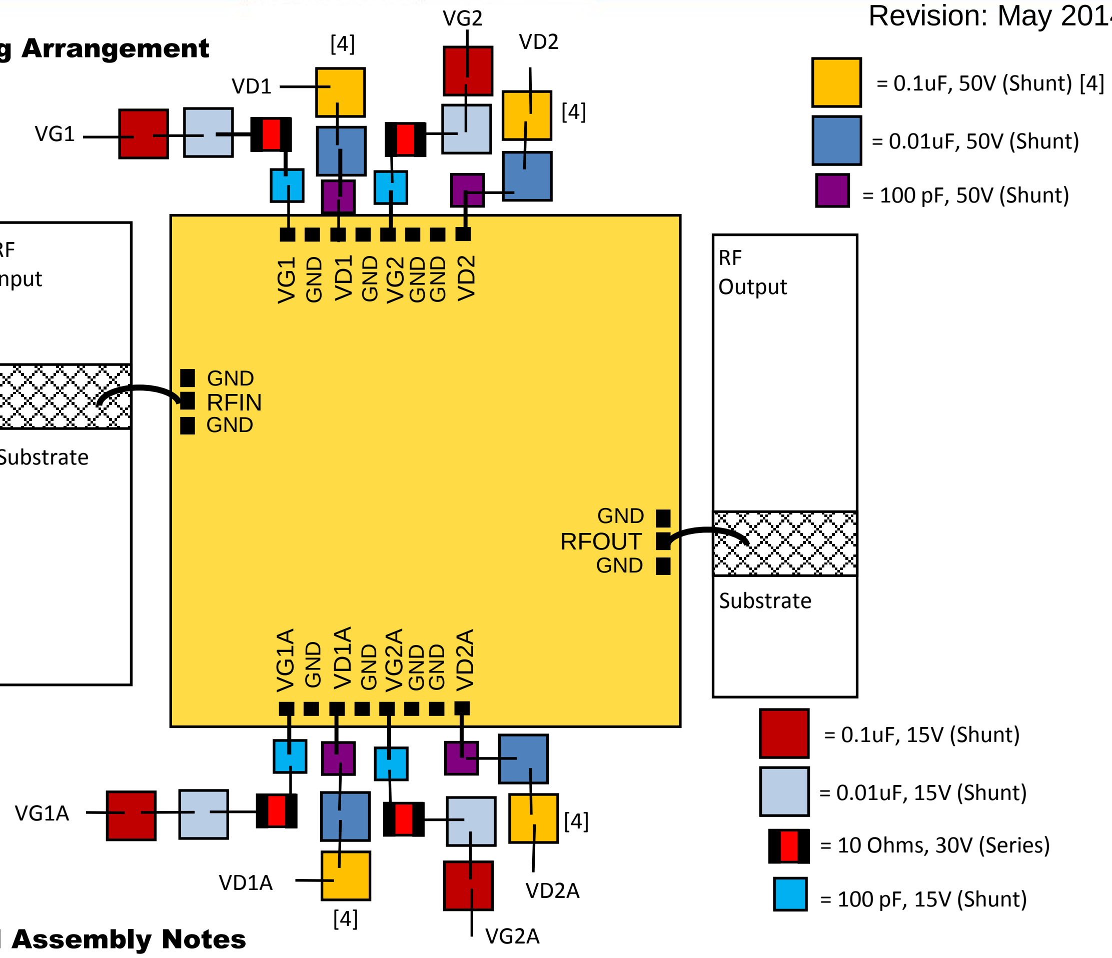
Suggested Bonding Arrangement



Recommended Assembly Notes

1. Bypass caps should be 100 pF (approximately) ceramic (single-layer) placed no farther than 30 mils from the amplifier.
2. Best performance obtained from use of <10 mil (long) by 3 by 0.5 mil ribbons on input and output.
3. Part must be biased from both sides as indicated.
4. The 0.1uF, 50V capacitors are not needed if the drain supply line is clean. If Drain Pulsing of the device is to be used, do **NOT** use the 0.1uF , 50V Capacitors.

Mounting Processes

Most NGAS GaN IC chips have a gold backing and can be mounted successfully using either a conductive epoxy or AuSn attachment. NGAS recommends the use of AuSn for high power devices to provide a good thermal path and a good RF path to ground. Maximum recommended temp during die attach is 320ºC for 30 seconds.

Note: Many of the NGAS parts do incorporate airbridges, so caution should be used when determining the pick up tool.

CAUTION: THE IMPROPER USE OF AuSn ATTACHMENT CAN CATASTROPHICALLY DAMAGE GaN CHIPS.

PLEASE ALSO REFER TO OUR "GaN Chip Handling Application Note" BEFORE HANDLING, ASSEMBLING OR BIASING THESE MMICS!