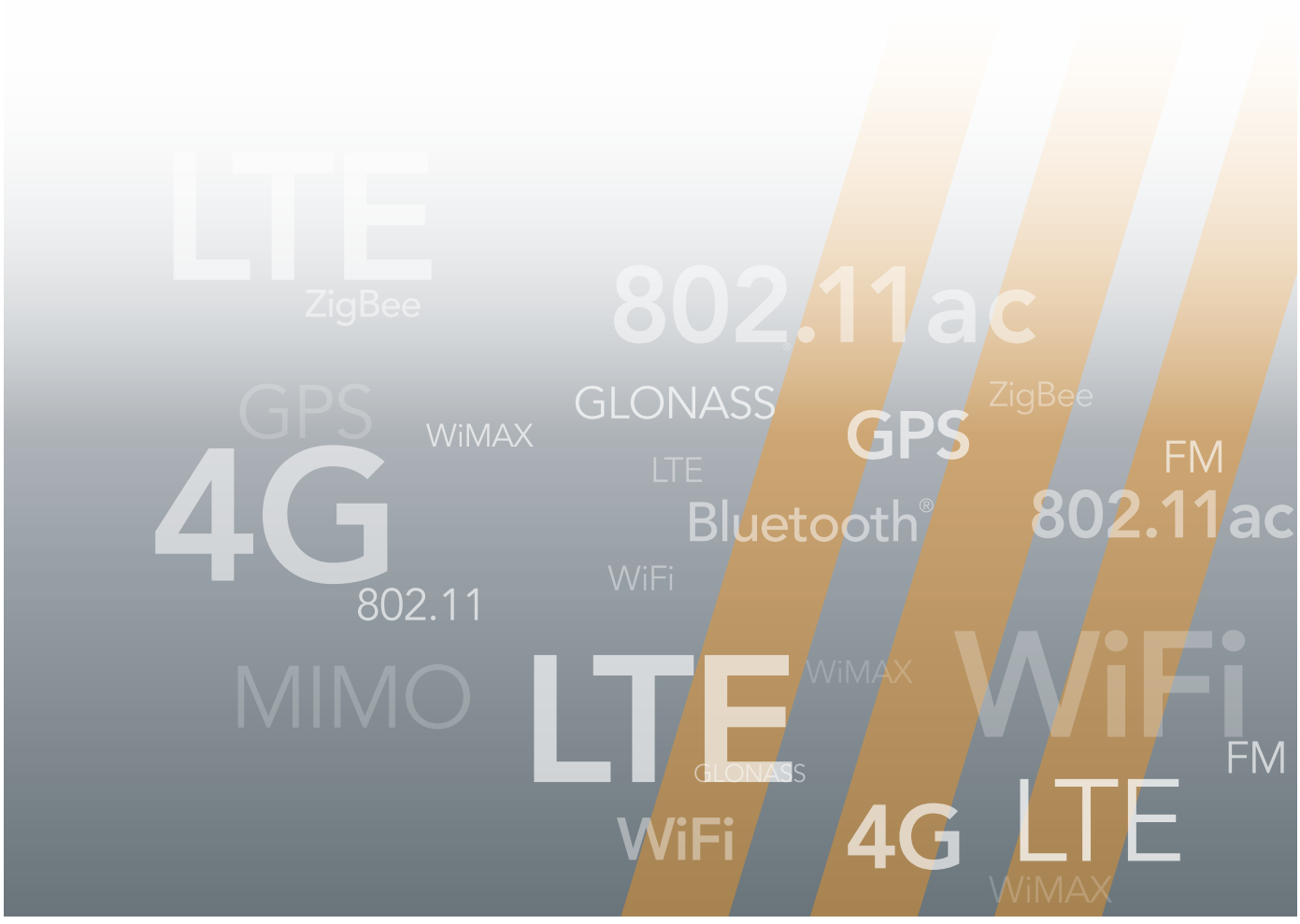
8451 SA

TECHNICAL SPECIFICATIONS

z8451
Signal Analyzer
PXI, PXIe



LITEPOINT

Port Descriptions

Front Panel

Label	Type	Description
I +,-	SMA	Differential baseband I input
Q +,-	SMA	Differential baseband Q input
EXT IN	SMA	External input for trigger or reference
EXT OUT	SMA	External output for trigger, reference or event

Inputs

I/Q Input Channels

Specification	Value
Channels	Two Differential Input Channels, I+/- and Q+/- (One I/Q)
Input Impedance Single-ended Differential	 50 Ω 100 Ω ≤ ±1% accuracy
Input VSWR DC to 250 MHz	 ≤ 1.3:1
Input Bias Current	≤ ±10 µA
Connectors	SMA

I/Q Input Voltage

Specification	Value
Absolute Maximum Input (no damage) Single-ended	 -2 V to +5 V (DC + peak AC), CAT I
Input Voltage Ranges	+10 dBm (2 Vppd) 0 dBm (0.63 Vppd) -10 dBm (0.2 Vppd) -20 dBm (0.063 Vppd)
Input Voltage Range Accuracy (1 MHz)	≤ ±0.05 dB at 25°C ambient ≤ ±0.01 dB drift per °C
Input Offset Adjustment	±1 V 4 µV resolution
Input Offset Accuracy	< ±(2 mV + 0.5% offset) at 25°C ≤ ±200 µV drift per °C

I/Q Input Dynamic Performance

Specification	Value
Analog Bandwidth -3 dB Bandwidth Stopband Rejection	 DC to 300 MHz ≥80 dB at 800 MHz
Passband Flatness (+10 dBm Range) DC to 50 MHz DC to 500 MHz DC to 1 GHz (0, -10, -20 Ranges) DC to 50 MHz DC to 500 MHz DC to 1 GHz	 +0.4/-0.2 dB +0.7/-0.2 dB +0.7/-1.0 dB +0.2/-0.2 dB +0.2/-1.2 dB +0.2/-2.0 dB
Spurious-Free Dynamic Range (excluding harmonics)	≥ 80 dBc at 10 MHz
Harmonic Distortion	≥ 75 dBc at 10 MHz
Intermodulation Distortion (2 tone, 10.6 MHz & 10.8 MHz)	≥ 80 dBc
Average Noise Density +10 dBm Range 0 dBm Range -10 dBm Range -20 dBm Range	 ≤ -145 dBm/Hz (-155 dBFS/Hz) ≤ -150 dBm/Hz (-150 dBFS/Hz) ≤ -153 dBm/Hz (-143 dBFS/Hz) ≤ -154 dBm/Hz (-134 dBFS/Hz)
Phase Noise (187.5 MHz, typical) 1 kHz offset frequency 10 kHz offset frequency 100 kHz offset frequency 1 MHz offset frequency 10 MHz offset frequency	 -110 dBc/Hz -130 dBc/Hz -132 dBc/Hz -138 dBc/Hz -140 dBc/Hz
I/Q Channel-to-Channel Match (DC to 50 MHz, same range settings)	≤ 0.2 dB magnitude ≤ 0.5° phase
I/Q Channel-to-Channel Isolation DC to 100 MHz 100 MHz to 250 MHz	 ≥ 90 dB ≥ 80 dB

Analog-to-Digital Converter (ADC) & Digital Downconverter (DDC)

Specification	Value
ADC Configuration	Simultaneous Sampling Dual ADC
ADC Vertical Resolution	14 Bits 0.0061% of full-scale range
ADC Clock Frequency	400 MS/s simultaneous sampling
ADC Clock Jitter	≤ 300 fs RMS
I/Q Data Vertical Resolution[1]	up to 32 bits 16-bit and 32-bit data formats
I/Q Data Rate (flexible data rate with fractional resampling)	123 S/s to 100 MS/s, 200 MS/s 400 MS/s (DDC Bypass) 1 Hz resolution
I/Q Data Memory	512 MiByte total
I/Q Waveform Size (matched I/Q sizes)	up to 128 MiSamples (16-bit data) up to 64 MiSamples (32-bit data)
I/Q Channel Mode (DDC input feed)	I/Q quadrature input pair I input only Q input only Independent I and Q (real mixing)
I/Q Instantaneous Bandwidth (alias-free)	162.5 MHz, 100 Hz to 81.25 MHz 1 Hz resolution
I/Q Resolution Bandwidth (RBW)	1 Hz to 3 MHz 0.1 Hz resolution
I/Q Center Frequency	0 Hz to 1 GHz 1 Hz resolution

Clock Input (front panel)

Specification	Value
Functionality	External ADC sampling clock input
Absolute Maximum Input (no damage)	±5 V (DC + peak AC), CAT I
Input Signal (operating range)	0.5 Vpp to 5 Vpp Sine or square wave
Input Impedance	50 Ω ± 2 % accuracy
Input Coupling	AC
Clock Input Frequency[2]	400 MHz, 800 MHz, 1.2 GHz, 1.6 GHz, or 2 GHz
Connector	SMA

[1] DDC filtering of quantization noise adds to vertical resolution by 10*log10(OSR), where OSR is the oversampling

[2] The ADC clock must be 400 MHz. The external clock may be an integer multiple (N) of 400 MHz, where N=1 to 5

Timebase Reference

Specification	Value
Timebase Reference	10 MHz or 100 MHz
Timebase Reference Source	Internal TCXO, External Input, Backplane
Internal TCXO Timebase	±2.5 ppm accuracy
Timebase Output	External Output

Trigger

Specification	Value
Trigger Source	I, Q, I/Q Envelope, External Input, Pattern, Software, Immediate (no trigger), TTL Trigger 0-7, Star Trigger
Trigger Slope/Polarity	Positive or Negative
Trigger Position	Pre-Trigger & Post-Trigger
Trigger Jitter	≤ 2.5 ns peak-to-peak

External Input (front panel)

Specification	Value
Functionality	Trigger Input, Timebase Reference Input
Absolute Maximum Input (no damage)	≤ ± 5 V (DC + peak AC), CAT I
Input Trigger Level Adjustment	-2 V to +2 V 0.5 mV resolution ≤ 20 mV accuracy 20 mV overdrive (input hysteresis)
Input Bandwidth (-3 dB)	≥ 250 MHz
Input Impedance	1 MΩ ‖ 30 pF or 50 Ω ≤ ±2% accuracy
Connector	SMB

External Ouput (front panel)

Specification	Value
Functionality	Trigger Output, Timebase Reference Output, Event Output, Programmable Clock Output, Programmable Pulse Output, Constant Level
Output Event Source	Trigger Event, Capture Complete Event, Operation Complete Event, Master Summary Status Event
Polarity	High or Low Truth
Programmable Event Pulse Width	50 ns to 163 ms
Programmable Clock	Period: 26.667 ns to 100 seconds 13.333 ns resolution 50% Duty Cycle
Programmable Pulse Pulse Repetition Interval Pulse Width	 26.667 ns to 100 seconds, 13.333 ns resolution 26.667 ns
Probe Compensation	10 kHz Clock which can be used to compensate probe
Limit Test Successful	Event pulse after each capture upon limit or mask test success
Output Level	TTL Compatible into ≥ 200 Ω ≥ ±24 mA Output Drive
Output Enable	Tri-State Output Capability
Connector	SMB

Backplane Triggers

Specification	Value
Functionality	Multi-Instrument Synchronization Trigger, Event Output Signals
Triggers	TTL Trigger 0-7
Direction	Input or Output
Source	Trigger Event, Capture Complete Event, Operation Complete Event, Master Summary Status Event, Constant Level
Polarity	High or Low Truth
Programmable Event Pulse Width	50 ns to 163 ms

Traces

Specification	Value
Trace Channels	Quantity 8
Trace Size	Up to 512 KiSample 32-bit floating point data
Trace Feed (source)	Input Channels or Reference Channels
Trace Type	Write (Live), Average, Max Hold, Min Hold (Reference Feeds use Write Type only)
Trace Average Count	2 to 65535
Trace Data Format	Linear Magnitude, Logarithmic Magnitude, Phase, Real, Imaginary, 32-bit floating point data

Reference Waveforms

Specification	Value
Reference Channels	Quantity 4
Reference Storage	Non-volatile memory storage
Reference Data	32 KiSample maximum waveform size 32-bit floating point data
Reference Data Format	Linear Magnitude, Logarithmic Magnitude, Phase, Real, Imaginary, 32-bit floating point data

Markers

Specification	Value
Marker Channels	Quantity 2
Marker Functionality	Waveform Trace Magnitude and Frequency Markers
Marker Source	Trace 1-8
Marker Peak Search Search Methods Selectable Search Options	 Maximum, Next Maximum by Amplitude, Next Maximum Left, Next Maximum Right Absolute Threshold, Relative Excursion

Data Processing & Download

Specification	Value
Self-Calibration	Automatic internal calibration: Input DC Offset Zero, Input DC Offset Adjust
Waveform Data Formats	16-bit or 32-bit signed integer (I/Q time-domain data) 32-bit floating point (Trace or Reference data) Intel or Motorola Byte Order

Instrument Stored States

Specification	Value
Functionality	Non-volatile storage of instrument setup configuration
Stored States	30 State 0 is Reset State Power-On State programmable

LED Indicators

Specification	Value
RDY (Ready)	OFF: Hardware Failure ON: Unit has passed power-up self-diagnostics TOGGLE: Unit has an error pending in error queue
TRG (Trigger)	OFF: Trigger event not detected ON/PULSE: Trigger complete event detected TOGGLE: Device identify enabled

PXI Interface

Specification	Value
PXI Slot Compatibility	PXI Standard Slot and PXIe Hybrid Slot Compatible
PXI Timing & Triggering Signals (XJ4 Connector)	PXI_TRIG[0:7] input/output PXI_STAR input PXI_CLK10 input

PXIe Interface

Specification	Value
PXIe Slot Compatibility	PXI Standard Slot and PXIe Hybrid Slot Compatible
PXI Timing & Triggering Signals (XJ4 Connector)	PXI_TRIG[0:7] input/output PXI_STAR input PXI_CLK10 input
PXIe Timing & Triggering Signals (XJ3 Connector)	PXI_DSTARA input (unused PXI_STAR input PXI_CLK10 input

Status Reporting

Specification	Value
IEEE-488.2 Device Status	Reporting Structure including Status Byte, Standard Event Registers, Questionable Registers, Operation Registers and Self-Test Status Registers

Power & Cooling

Power Supplies

Model	Platform	Voltage	Typical Current	Maximum Current
z8451	PXI	+3.3 VDC +5 VDC +12 VDC -12 VDC	4.88 A 1.14 A 0.02 A 0.00 A	6.03 A 1.30 A 0.03 A 0.00 A
	PXIe	+3.3 VDC +5 VDC	1.68 A 1.74 A	1.76 A 1.92 A

Total Cooling & Power Consumption

Model	Platform	Typical Cooling & Power	Maximum Cooling & Power
z8451	PXI	22.0 W	26.8 W
	PXIe	26.4 W	28.8 W

Physical & Environmental

Size & Weight

Specification	Value
Physical Size	Single-Wide 3U PXI/PXIe Instrument 8.25" x 0.79" x 5.25" (L x W x H) 20.96 cm x 2.01 cm x 13.34 cm (L x W x H)
Weight	11.1 oz or 315 g

Temperature Range

Specification	Value
Operating	0°C to +50°C ambient (MIL-PRF28800F Class 3)
Storage	-40°C to +75°C (MIL-PRF28800F Class 3)
Over-Temperature	Automatic shutdown if internal temperature exceeds +65°C
Calibration Range	+20°C to +30°C ambient, after a 20 minute warm-up period, to meet all calibration specification accuracies

Relative Humidity

Specification	Value
Operating or Storage Up to +30 °C +30 °C to +40 °C above +40 °C	 5 to 95% ± 5% non-condensing 5 to 75% ± 5% non-condensing 5 to 45% ± 5% non-condensing

Altitude

Specification	Value
Operating	Up to 5 km
Storage	Up to 15 km

Terminology

Numeric Prefixes

When referring to numeric values, this document will use SI (International System of Units) and IEC (International Electrotechnical Commission) standard prefixes. Prefix definitions are in the following table.

Prefix	Multiplier
n (nano)	1/(1000x1000x1000)
µ (micro)	1/(1000x1000)
m (milli)	1/1000
k/K (kilo)	1000
M (Mega)	1000x1000
G (Giga)	1000x1000x1000
Ki (Kibi)	1024
Mi (Mebi)	1024x1024
Gi (Gibi)	1024x1024x1024

Differential Outputs

Single-Ended is used to refer to the output on either the + or – output pin

Differential is used to refer to the output between the + and- output pins

Vd indicates Volts differential

Vppd indicates Volts peak-to-peak differential

Safety

This product is designed to meet the requirements of the following standard of safety for electrical equipment for measurement, control and laboratory use: EN 61010-1

Electromagnetic Compatibility

CE Marking EN 61326-1:1997 with A1:1998 and A2:2001 Compliant

FCC Part 15 (Class A) Compliant

Emissions

EN 55011	Radiated Emissions, ISM Group 1, Class A, distance 10 m, emissions < 1 GHz
EN 55011	Conducted Emissions, Class A, emissions < 30 MHz Immunity
EN 61000-4-2	Electrostatic Discharge (ESD), 4 kV by Contact, 8 kV by Air
EN 61000-4-3	RF Radiated Susceptibility, 10 V/m
EN 61000-4-4	Electrical Fast Transient Burst (EFTB), 2 kV AC Power Lines
EN 61000-4-5	Surge
EN 61000-4-6	Conducted Immunity
EN 61000-4-8	Power Frequency Magnetic Field, 30 A/m
EN 61000-4-11	Voltage Dips and Interrupts

CE Compliance

This product meets the necessary requirements of applicable European Directives for CE Marking as follows:

73/23/EEC Low Voltage Directive (Safety)
89/336/EEC Electromagnetic Compatibility Directive (EMC)

See Declaration of Conformity for this product for additional regulatory compliance information.

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