Product Specification

PE42660 DIE

SP6T UltraCMOS™ 2.75 V Switch 100 – 3000 MHz

Figure 1. Functional Diagram

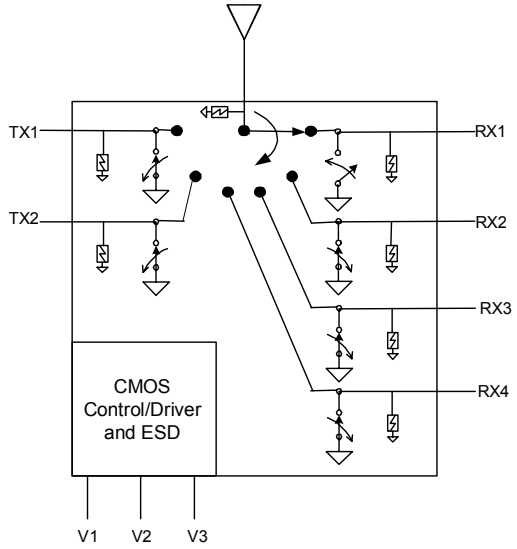
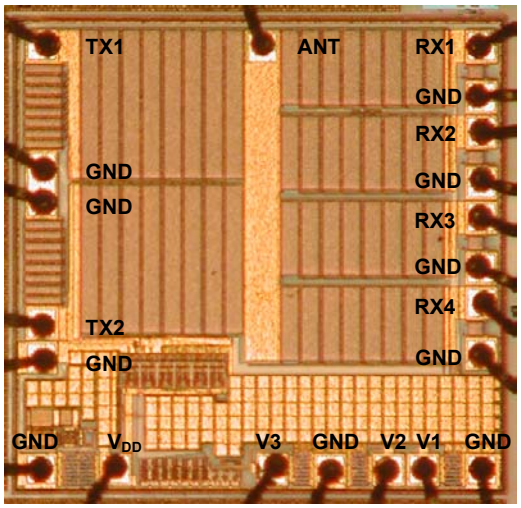


Figure 2. Die Top View



Features

- Three pin CMOS logic control with integral decoder/driver
- Exceptional harmonics performance: $2f_o$ = -85 dBc and $3f_o$ = -83 dBc
- Low TX insertion loss: 0.55 dB at 900 MHz, 0.65 dB at 1900 MHz
- TX – RX Isolation of 48 dB at 900 MHz, 40 dB at 1900 MHz
- 1500 V HBM ESD tolerance all ports
- 41 dBm P1dB
- No blocking capacitors required

Product Description

The PE42660 is a HaRP™-enhanced SP6T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market. On-chip CMOS decode logic facilitates three-pin low voltage CMOS control, while high ESD tolerance of 1500 V at all ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Table 1. Electrical Specifications @ +25 °C, V_{DD} = 2.75 V (Z_S = Z_L = 50 Ω)

Parameter	Conditions	Typical	Units
Operational Frequency		100-3000	MHz
Insertion Loss	ANT - TX - 850 / 900 MHz ANT - TX - 1800 / 1900 MHz ANT - RX - 850 / 900 MHz ANT - RX - 1800 / 1900 MHz	0.55 0.65 0.90 1.00	dB dB dB dB
Isolation	TX - RX - 850 / 900 MHz TX - RX - 1800 / 1900 MHz TX - TX - 850 / 900 MHz TX - TX - 1800 / 1900 MHz	48 40 29 25	dB dB dB dB
Return Loss	850 / 900 MHz 1800 / 1900 MHz	22 23	dB
2nd Harmonic[1]	35 dBm TX Input - 850 / 900 MHz 33 dBm TX Input - 1800 / 1900 MHz	-85 -84	dBc
3rd Harmonic[1]	35 dBm TX Input - 850 / 900 MHz 33 dBm TX Input - 1800 / 1900 MHz	-83 -82	dBc
Switching Time	(10-90%) (90-10%) RF	2	µs

Notes: 1. Pulsed RF input duty cycle of 50% and 4620 µs, measured per 3GPP TS 45.005

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T_{OP}	-40		+85	°C
V_{DD} Supply Voltage	V_{DD}	2.65	2.75	2.85	V
I_{DD} Power Supply Current (V_{DD} = 2.75 V)	I_{DD}		13	50	µA
TX input power[2] (VSWR ≤ 3:1) 824-915 MHz	P_{IN}			+35	dBm
TX input power[2] (VSWR ≤ 3:1) 1710-1910 MHz				+33	
RX input power[2] (VSWR ≤1:1)	P_{IN}			+20	dBm
Control Voltage High	V_{IH}	0.7 x V_{DD}			V
Control Voltage Low	V_{IL}			0.3 x V_{DD}	V

Note: 2. Assumes RF input period of 4620 µs and duty cycle of 50%.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
P_{IN}(50 Ω)	TX input power (50 Ω) [3,4] 824-915 MHz		+38	dBm
	TX input power (50 Ω) [3,4] 1710-1910 MHz		+36	
	RX input power (50 Ω) [3,4]		+23	
P_{IN} (∞:1)	TX input power (VSWR = (∞:1)[3,4] 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1)[3,4] 1710-1910 MHz		+33	
V_{ESD}	ESD Voltage (HBM, MIL_STD 883 Method 3015.7)		1500	V

Note: 3. Assumes RF input period of 4620 µs and duty cycle of 50%.
4. V_{DD} within operating range specified in Table 2.

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	ANT[6]	RF Common – Antenna
2	TX1[6]	RF I/O - TX1
3	GND[5]	Ground (Requires two bond wires)
4	TX2[6]	RF I/O – TX2
5	GND[5]	Ground
6	GND[5]	Ground
7	V_{DD}	Supply
8	V3	Switch control input, CMOS logic level
9	GND[5]	Ground
10	V2	Switch control input, CMOS logic level
11	V1	Switch control input, CMOS logic level
12	GND[5]	Ground
13	GND[5]	Ground
14	RX4[6]	RF I/O – RX4
15	GND[5]	Ground
16	RX3[6]	RF I/O – RX3
17	GND[5]	Ground
18	RX2[6]	RF I/O – RX2
19	GND[5]	Ground
20	RX1[6]	RF I/O – RX1

Notes: 5. Bond wires should be physically short and connected to ground plane for best performance.

6. Blocking capacitors needed only when non-zero DC voltage present.

Figure 3. Pin Configuration (Top View)

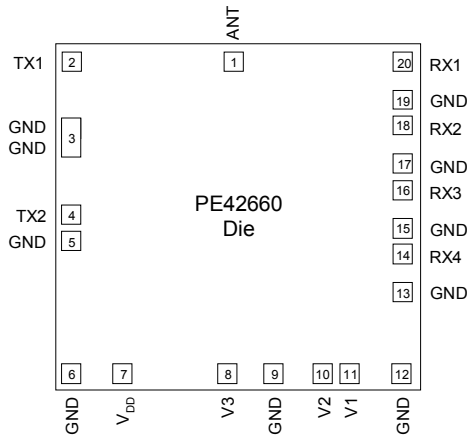


Table 5. Truth Table

Path	V3	V2	V1
ANT – RX1	0	0	0
ANT – RX2	0	0	1
ANT – RX3	0	1	0
ANT – RX4	0	1	1
ANT - TX1	1	0	x
ANT - TX2	1	1	x

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Die ID	Description	Package	Shipping Method
42660-90	C9807_01	PE42660-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
42660-99	C9807_01	PE42660-DIE-400G	Waffle Pack	400 Dice / Waffle Pack
42660-00	C9807_01	PE42660-DIE-1H	Evaluation Kit	1/ box

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Data Sheet Identification

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Preliminary Specification

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Product Specification

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