

PRODUCT SUMMARY

The Holworth HSM Series RF Synthesizer Module is a stand alone, CW source. This high frequency source is designed for ease of system integration where LO performance is critical. With >200kHr MTBF, Holworth synthesizers provide the best in industry stability. When integrated as multiple units, the result is true phase coherency with industry leading channel-to-channel stability. Compare the HSM Series to competitive designs and discover the most compact form factor available in its overall performance class.



The core architecture of the HSM Series modules is derived from Holworth's proprietary NON-PLL design to provide the ultimate in phase / frequency stability. This direct-digital/direct-analog hybrid design was originally developed as a key building block for our phase noise analysis products. The hybrid architecture provides frequency agility & resolution, phase continuous switching and predictable performance without compromising on spurious or phase noise performance.

HSM EXTENDED FREQUENCY OPTIONS:

Model No.	Frequency Range	Phase Noise Performance
HSM12001B	10MHz to 12.5GHz	-110 dBc/Hz at 12GHz (10kHz offset)
HSM18001B	10MHz to >20GHz	-106 dBc/Hz at 18GHz (10kHz offset)

Note: Holworth's "Ultra Low Phase Noise" statement is real. We make no assumptions. 100% of all RF synthesizers manufactured by Holworth Instrumentation are subjected to full phase noise evaluation. (This critical parameter cannot be accepted as being "OK" based on spectrum analysis or an alternate test.)

The versatile HSM Series Synthesizer Module can be controlled directly via the SPI bus, the Holworth GUI, a preloaded lookup table, LabVIEW™, MATLAB™, C++, C#, etc. Some systems integrators have preferred the supported Linux platform over a Windows based PC.

The attractive performance-to-price ratios available with the Holworth HSM Series offers optimal solutions for electronics design, manufacturing test applications, as well as OEM systems integration.

Finally, with MTBFs greater than 200,000 hours, the HSM Series synthesizer module has been designed to exceed the most stringent reliability requirements.

HSM DESIGN HIGHLIGHTS

- 100% Phase Coherent Channel-Channel
- Onboard Precision 100MHz OCXO (free running)
- 100MHz Reference Out: -165dBc/Hz^{1/2} (10kHz OS)
- Reference Input: 10MHz or 100MHz
- SPI, USB or Ethernet Communications Interface
- Internal Temperature Monitor Output
- External Pulse Modulation

ELECTRICAL SPECIFICATIONS - FREQUENCY

The specified parameters for the HSM Series RF Synthesizer Modules are fully verified at final performance test and 100% guaranteed for the warranted life of the product. Performance specifications listed on this page are specific to Frequency.

FREQUENCY PERFORMANCE¹

PARAMETER	MIN	TYPICAL	MAX	COMMENTS
Frequency Range Model HSM12001B Model HSM18001B	10 MHz 10 MHz		12 GHz 18 GHz	VHF through X Band (settable to 12.5GHz) VHF through Ku Band (settable to 22.5GHz)
Frequency Step Size		0.001 Hz		
Phase Offset	0 deg		+360 deg	
Switching Speed (Frequency) SPI Mode (ASCII) SPI Mode (Binary)			300us 100us	
Internal Time Base Reference (Oscillator Aging Rate)		± 1 ppm/yr		1 st year. ±0.5 ppm/yr each subsequent year
Temperature Effects		± 1 ppm		0 to 55 °C
Line Voltage Effects (12V)		± 0.1 ppm		±5%
Reference Output Frequency Amplitude Impedance	+2 dBm	100 MHz 50 Ω	+6 dBm	Nominal Nominal
External Reference Input Input Frequency 10MHz Lock Range 10MHz External Amplitude 100MHz External Amplitude Impedance Waveform	0 dBm +2 dBm	10 / 100 ± 4 ppm 50 Ω	± 1 ppm +10 dBm +6 dBm	Software Select 10MHz, 100MHz or No Ext. Ref. 20Hz Locking BW, Internal OCXO remains on 20Hz Locking BW, Internal OCXO remains on Internal OCXO shuts off 50 Ω (nom) Sine

¹ Specifications are subject to change per the discretion of Holworth Instrumentation, Inc

ELECTRICAL SPECIFICATIONS - AMPLITUDE

The specified parameters for the HSM Series RF Synthesizer Modules are fully verified at final performance test and 100% guaranteed for the warranted life of the product. Performance specifications listed on this page are specific to Amplitude.

AMPLITUDE PERFORMANCE¹

PARAMETER	MIN ²	TYPICAL ³	MAX ²	COMMENTS
Output Power (Calibrated) 10 MHz to 12 GHz 12 GHz - 18 GHz	-10 dBm -10 dBm		+18 dBm +16 dBm	Settable -20 to +23 dBm
Resolution		0.01 dB		
Connector		50 Ω		SMA
SWR (S₁₁) 10 MHz < f $\leq$ 6 GHz 6 GHz < f $\leq$ 18 GHz		1.33 (-17.0 dB) 1.43 (-15.0 dB)		
Maximum Reverse Power Max DC Voltage > 100 kHz	25 V _{DC} maximum by design. *** Some applications may require reverse power protection. 16 dBm max by design.			
Switching Speed (Amplitude)			100us	Settling to within 0.1dB
Absolute Level Accuracy 10 MHz - 6 GHz 6 GHz - 12 GHz -10 dBm to 5 dBm 5 dBm to 18 dBm 12 GHz - 18 GHz -10 dBm to 5 dBm 5 dBm to 16 dBm		± 0.5 dB ± 0.5 dB ± 1 dB ± 0.6 dB ± 1.1 dB		25C to 35C (case temperature)
SSB Phase Noise 2.0 GHz, 10 kHz offset 4.0 GHz, 10 kHz offset 8.0 GHz, 10 kHz offset 12.0 GHz, 10 kHz offset 18.0 GHz, 10 kHz offset		≤ -128 dBc/Hz ≤ -122 dBc/Hz ≤ -114 dBc/Hz ≤ -110 dBc/Hz ≤ -106 dBc/Hz		
Harmonics (CW mode)		-30 dBc		
Non-Harmonics (CW mode) 10 MHz to 8 GHz 8 GHz to 18 GHz		-60 dBc -50 dBc		
Sub-Harmonics (CW mode) 10 MHz to 8 GHz 8 GHz to 18 GHz		-60 dBc -50 dBc		
Jitter (RMS) at 18 GHz		55 fs		5 kHz < BW < 20 MHz

¹ Specifications are subject to change per the discretion of Holworth Instrumentation, Inc.

² All MIN/ MAX (Minimum/ Maximum) performance parameters are guaranteed and 100% verified during final performance test.

³ Typical performance is "by design" and consistent with field performance data.

ELECTRICAL SPECIFICATIONS - AMPLITUDE (continued)

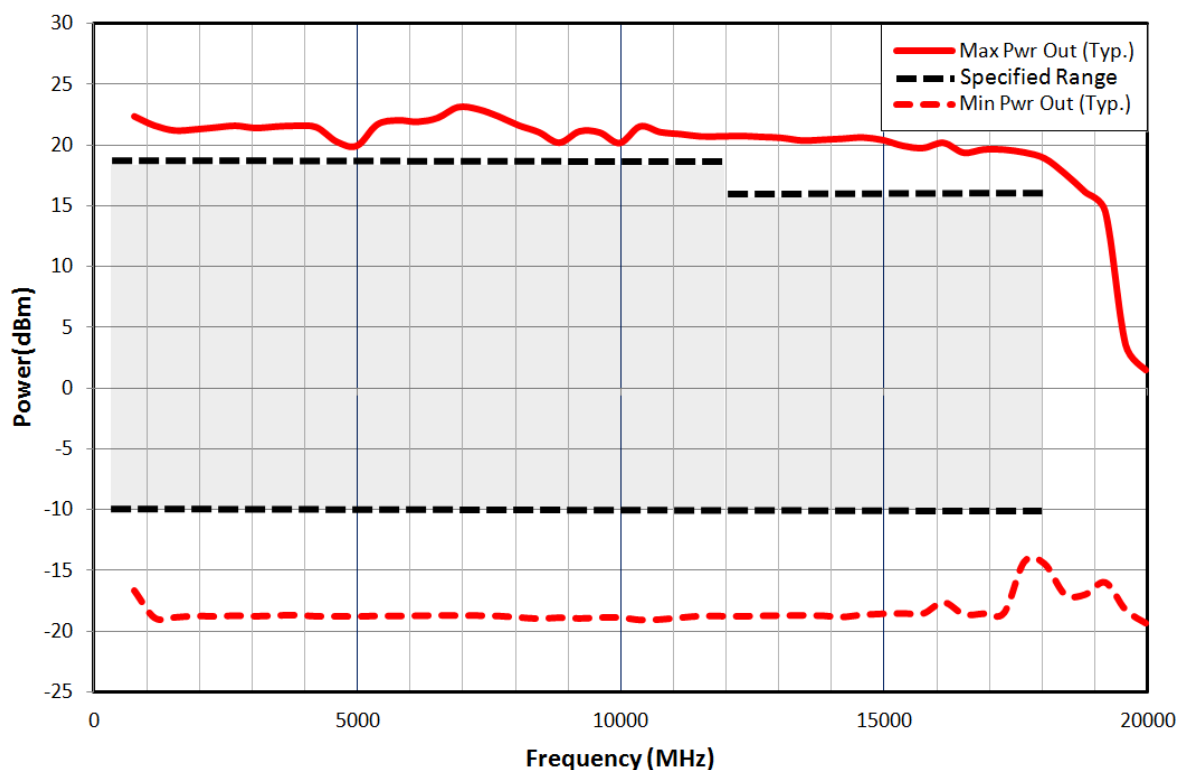


Figure 1: Maximum and Minimum Amplitude Threshold

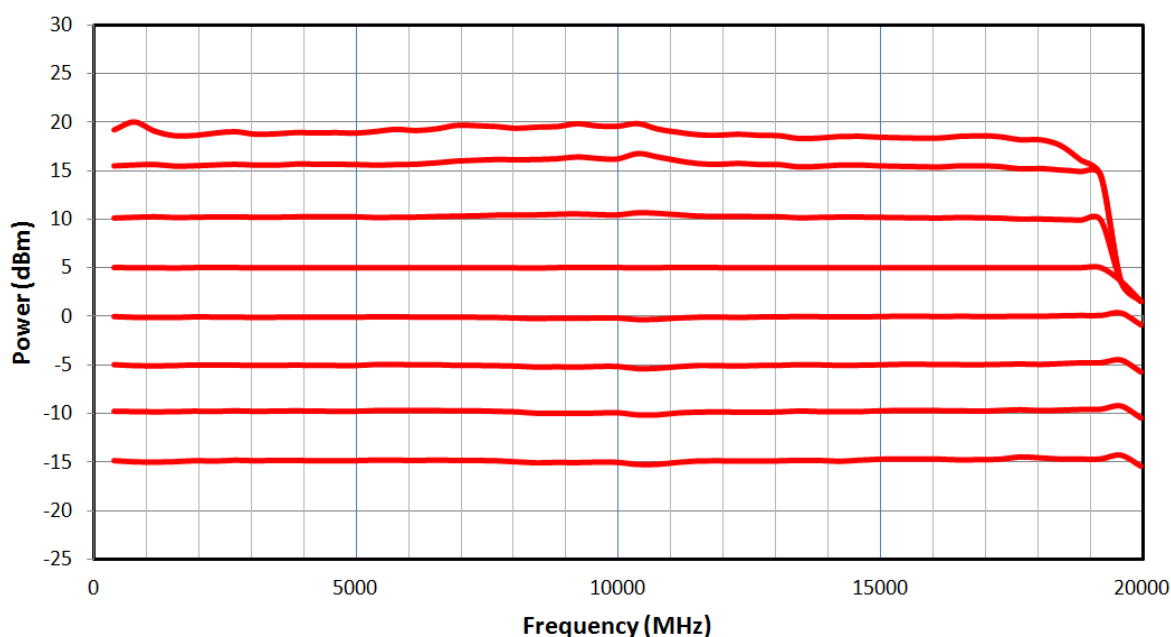


Figure 2: Calibrated Output Power Accuracy vs. Frequency

ELECTRICAL SPECIFICATIONS - MODULATION (External Stimulus)

The modulation parameters listed here are based on modulation functions as related to the use of an external modulation stimulus.

PARAMETER	PERFORMANCE	COMMENTS
PULSE MODULATION¹ (Analog)		
Risetime (T_r)	<20 ns	
Falltime (T_f)	<20 ns	
On/Off Ratio 10MHz to 2GHz 2GHz to 5GHz 5GHz to 12GHz	> 60dB > 50dB > 90dB	
Minimum Pulse Width	50 ns	
ALC Loop Deviation (ALC disabled)	1dB difference from ALC enabled	

¹ Specifications are subject to change per the discretion of Holworth Instrumentation, Inc

PARAMETER	PERFORMANCE	COMMENTS
External Trigger Threshold	+1V	±5% into 50Ω

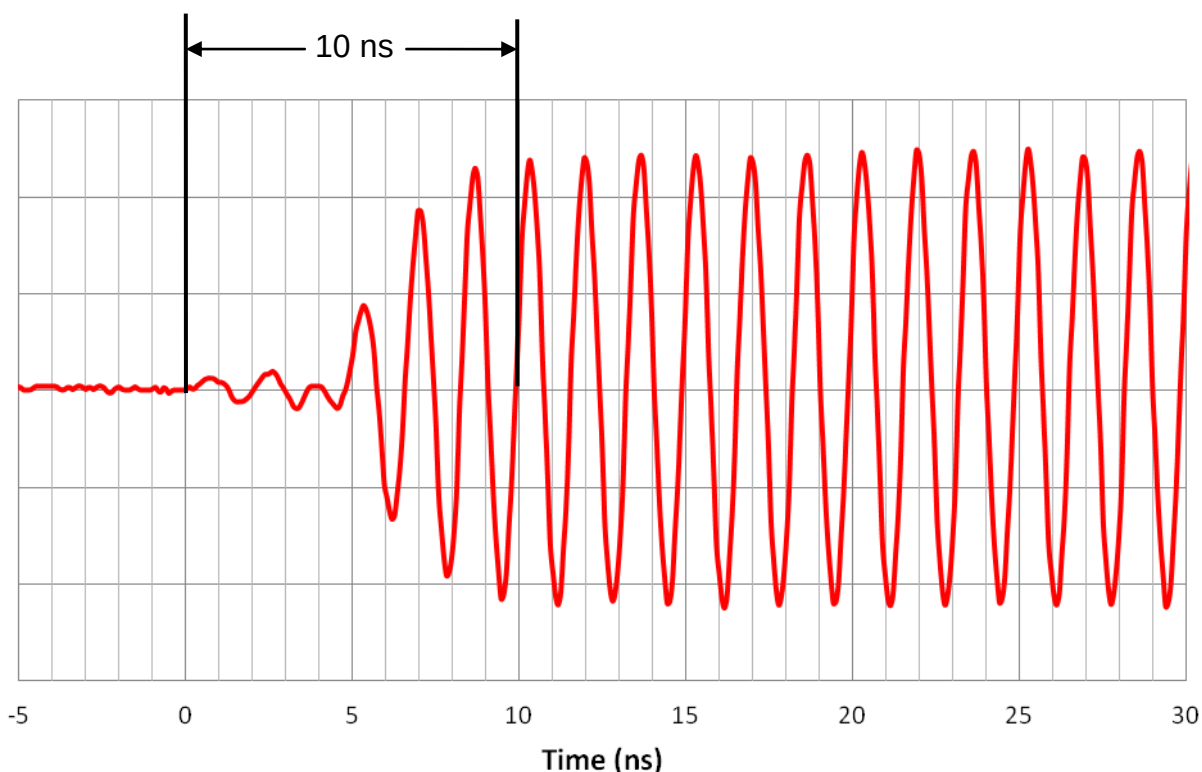


Figure 3: External Pulse Modulation Rise Time (seconds)

ENVIRONMENTAL SPECIFICATIONS ¹

Environmental specifications are based on component margins, thermal verification testing and current draw tests.

PARAMETER	MIN	TYPICAL	MAX	COMMENTS
Operating Temperature Standard Models Option: OPT-SYS3 ²	0 C -40C		+55 C +75C	Performance tests at: +20C ±5C Performance tests at: -40, +20, +75C ±2C
Temperature Monitor Range	-40 C		+85 C	Absolute
Power Consumption ³ Standard Models Option: OPT-SYS3		15 W 15 W	18 W 18 W	18W during warm-up (OCXO) 18W during warm-up (OCXO)

¹ Specifications are subject to change per the discretion of Holworth Instrumentation, Inc

² Extended temperature testing conducted using an external 100MHz reference.

³ See PINOUT CONFIGURATION table on page 10 for volt/amp ratings per pin.

PHASE NOISE DATA - Standard OCXO

The raw data displayed in Figure 2 is of SSB Phase Noise vs. Frequency Offset as measured for the HSM Series RF Synthesizer Modules. All data was collected at an output power setting of +10dBm.

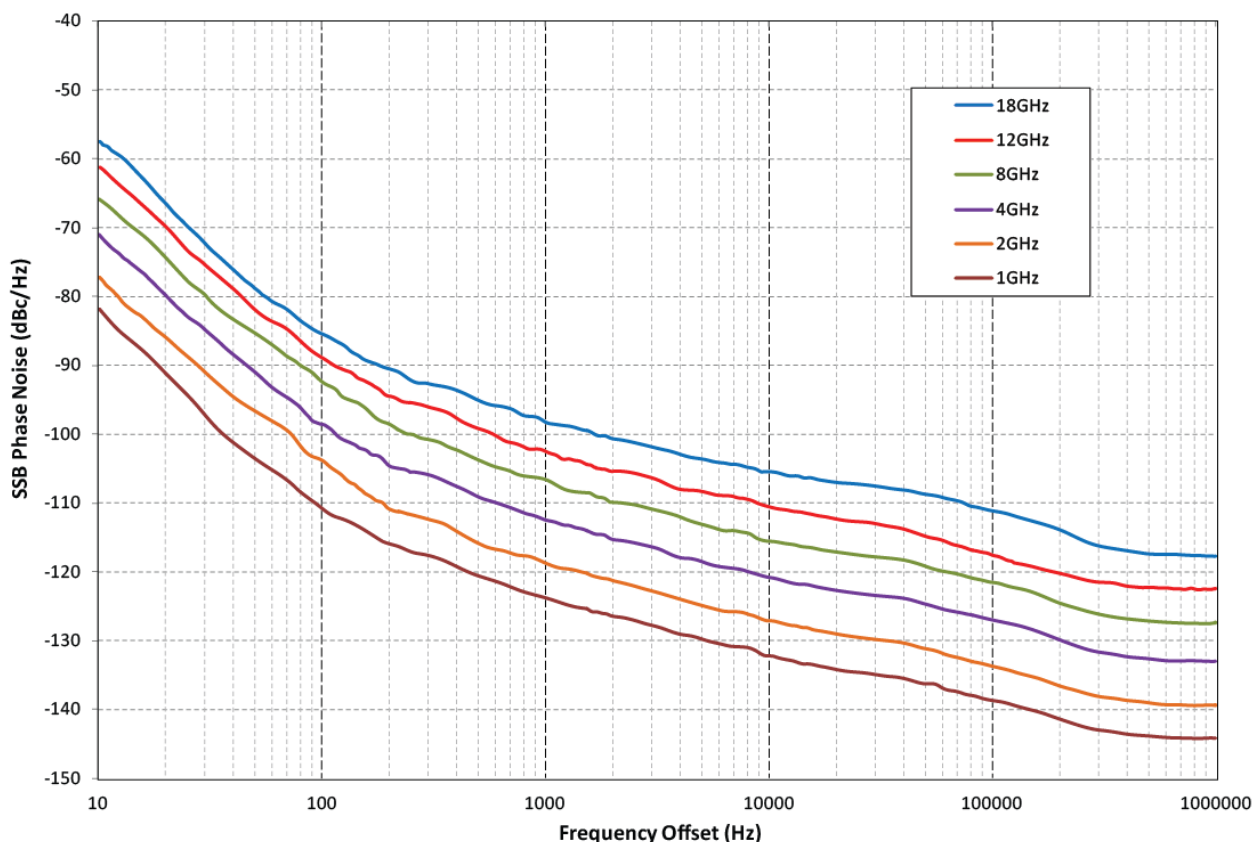


Figure 4: SSB Phase Noise ($P_{OUT}=+10dBm$)

PHASE NOISE DATA - Optional OCXO

The HSM Series RF Synthesizer Modules can be equipped with an optional, high performance OCXO. Option OPT-OCXO provides an approximate 10dB improvement in the phase noise at close to the carrier (10Hz offset). The example plots contained in this section show the phase noise improvement with OPT-OCXO versus that with a standard OCXO installed.

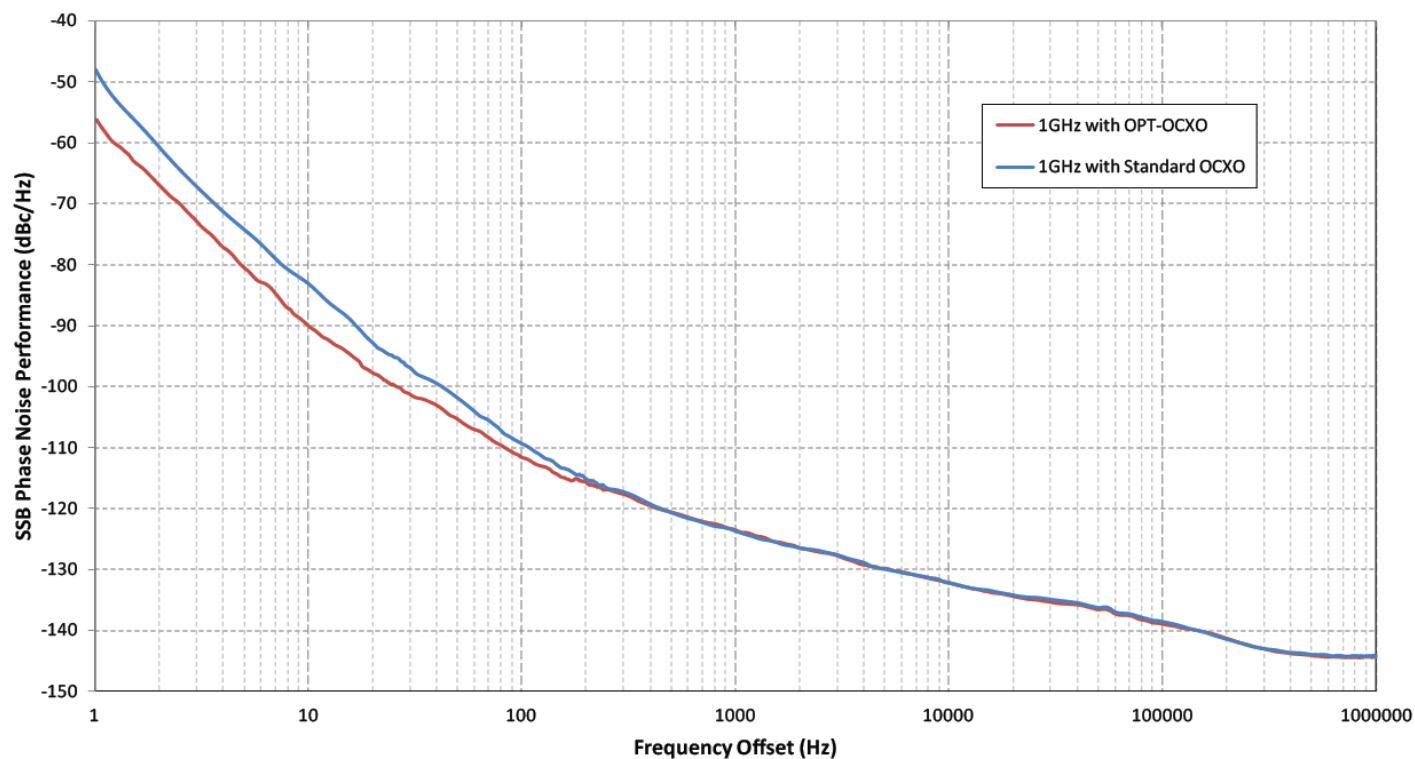


Figure 5: SSB Phase Noise OPT-OCXO Comparison ($P_{OUT}=+10\text{dBm}$)

SPECTRAL PURITY DATA

The data contained in this section demonstrates the spectral purity performance of the HSM Series designs. Spectrum analyzer test settings: 300kHz Resolution BW, 30kHz Video BW.

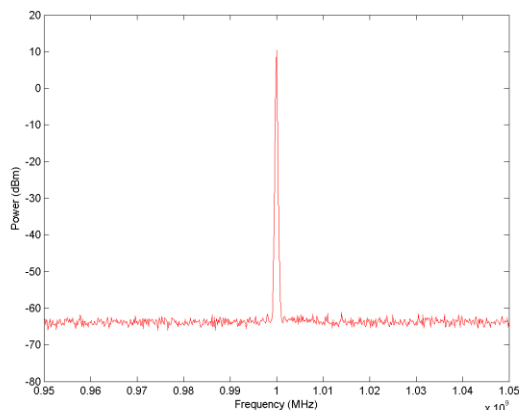


Figure 6a: 1GHz Narrow Band Spectrum

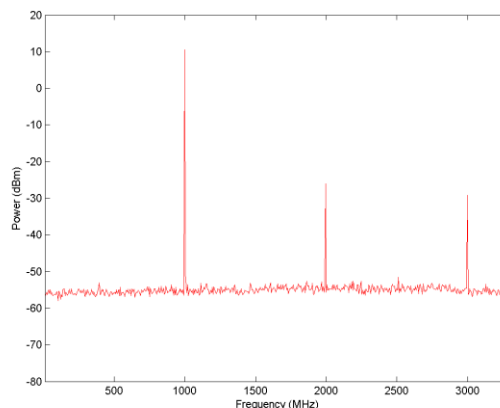


Figure 6b: 1GHz Broad Band Spectrum

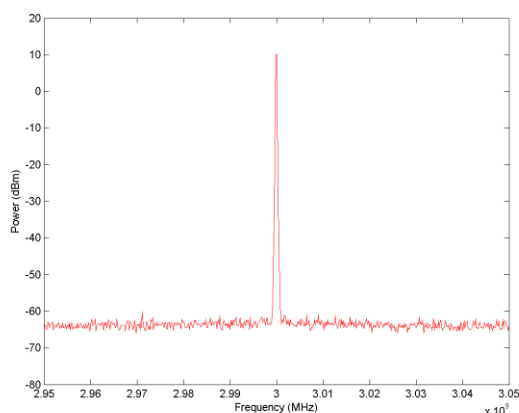


Figure 7a: 3GHz Narrow Band Spectrum

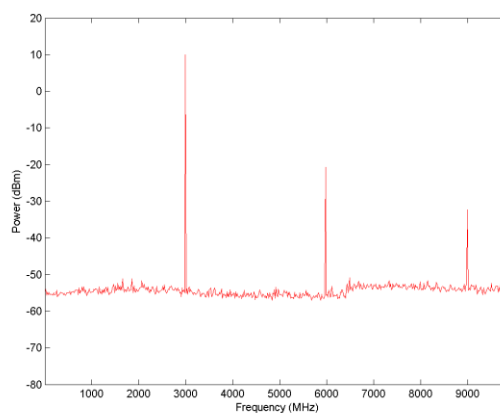


Figure 7b: 3GHz Broad Band Spectrum

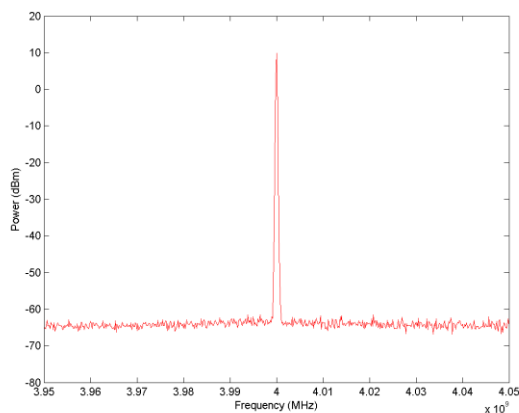


Figure 8a: 4GHz Narrow Band Spectrum

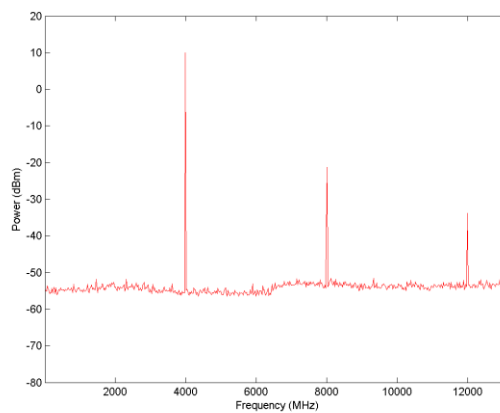


Figure 8b: 4GHz Broad Band Spectrum

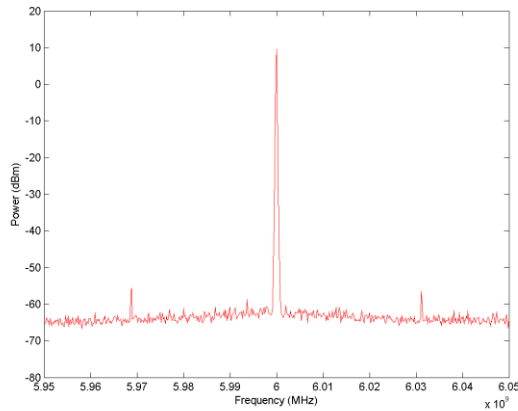


Figure 9a: 6GHz Narrow Band Spectrum

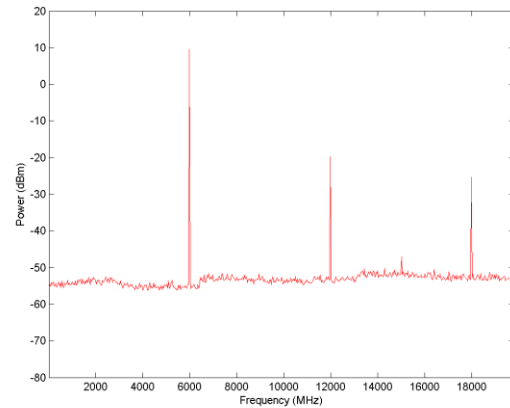


Figure 9b: 6GHz Broad Band Spectrum

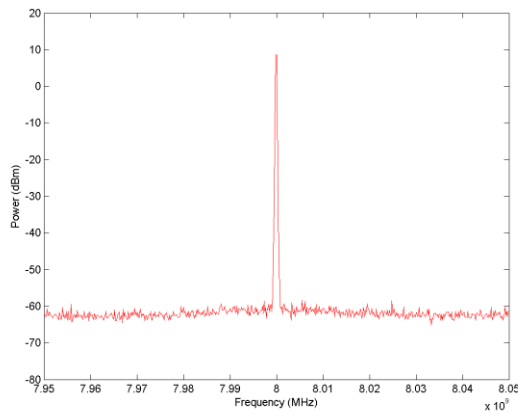


Figure 10a: 8GHz Narrow Band Spectrum

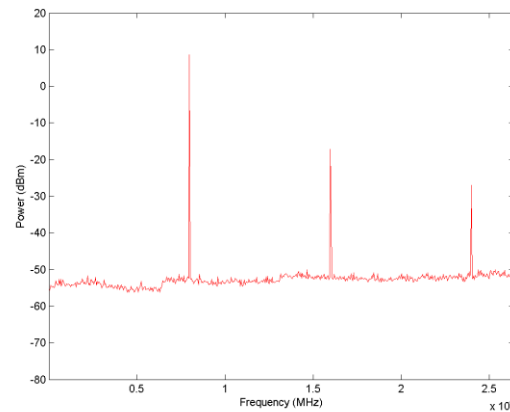


Figure 10b: 8GHz Broad Band Spectrum

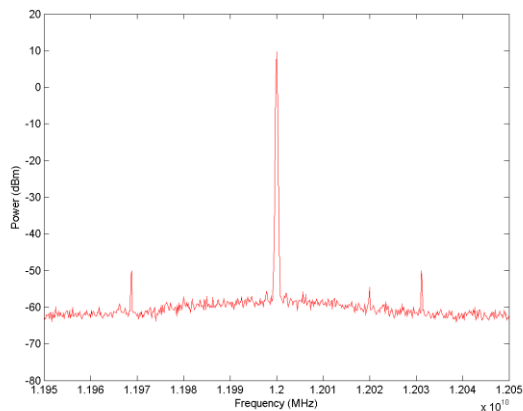


Figure 11a: 12GHz Narrow Band Spectrum

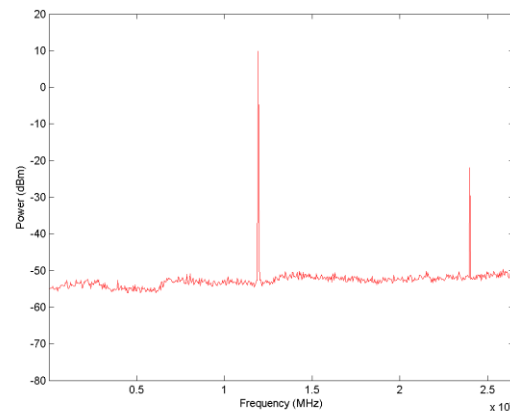


Figure 11b: 12GHz Broad Band Spectrum

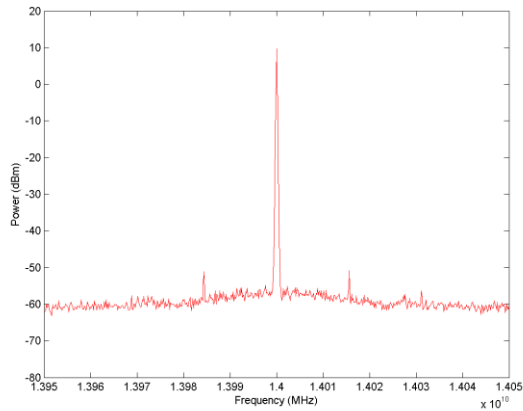


Figure 12a: 14GHz Narrow Band Spectrum

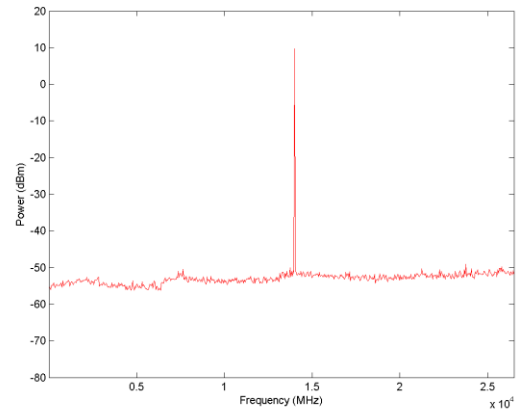


Figure 12b: 14GHz Broad Band Spectrum

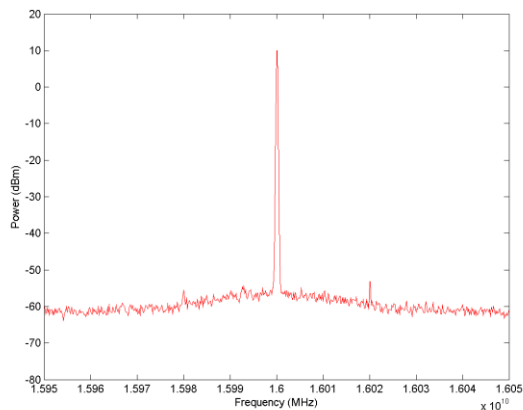


Figure 13a: 16GHz Narrow Band Spectrum

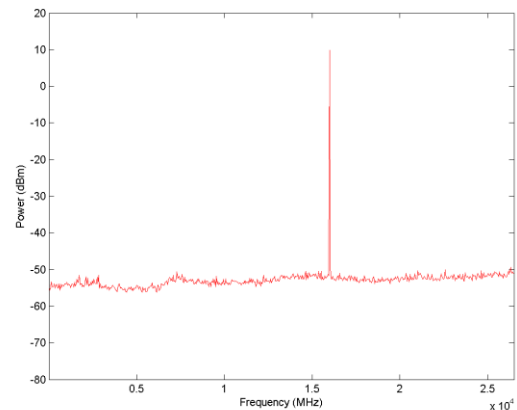


Figure 13b: 16GHz Broad Band Spectrum

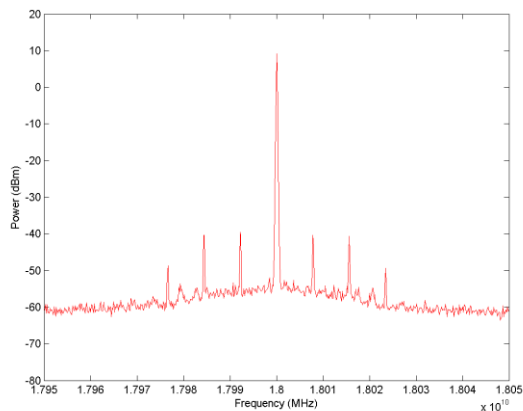


Figure 14a: 18GHz Narrow Band Spectrum

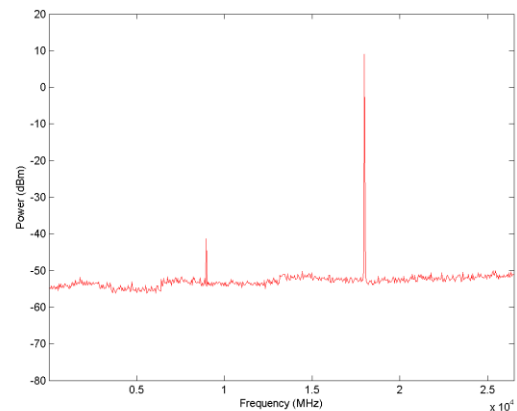
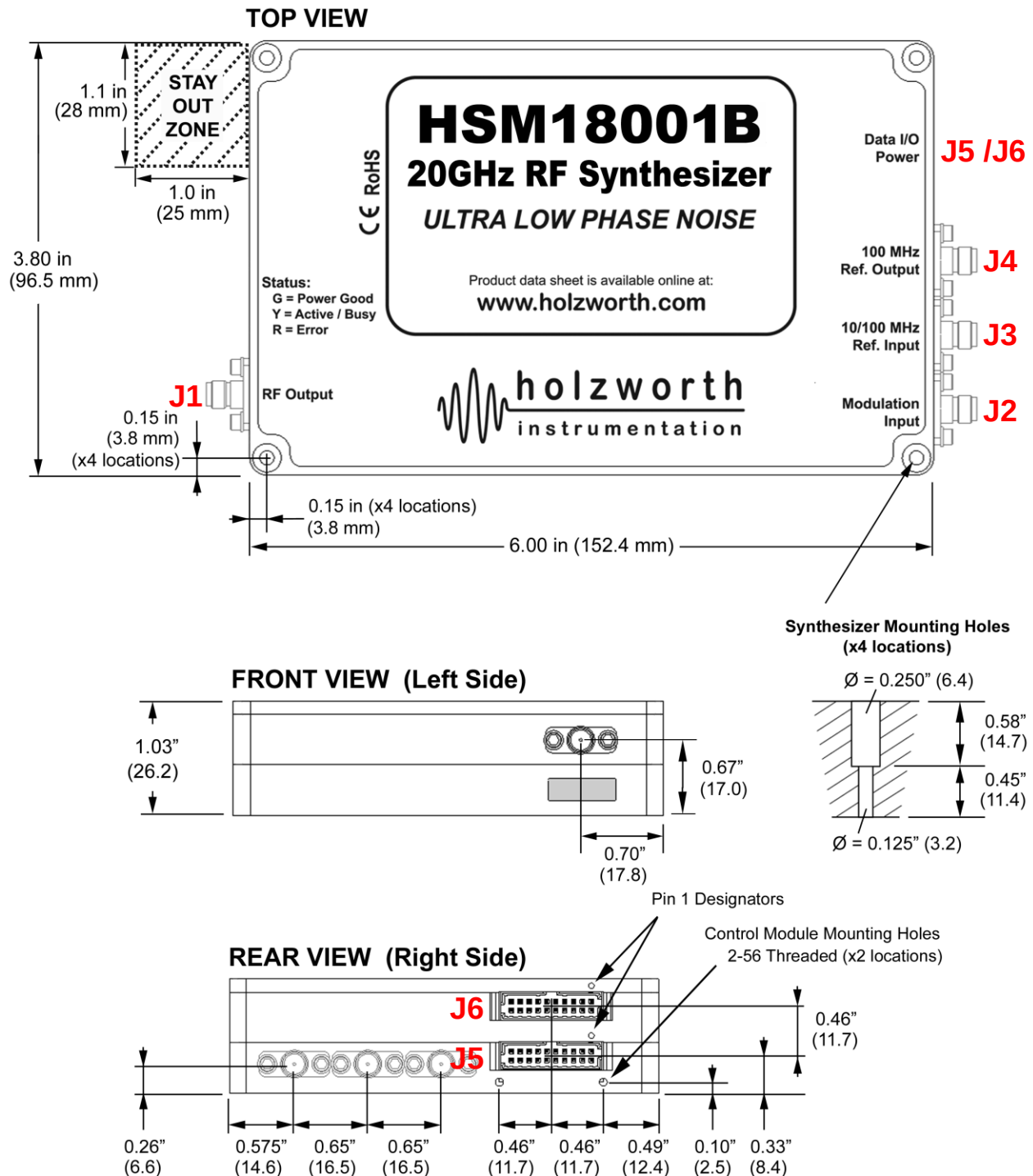


Figure 14b: 18GHz Broad Band Spectrum

Data at additional frequencies available upon request.

INTERFACE DEFINITIONS

Mechanical details are in both inches and millimeters (listed inside parenthesis). Allow for dimensional tolerances of up to ± 0.010 inches.



INTERFACE DEFINITIONS

The interfaces defined within this section are cross referenced to the mechanical configuration included in this document. Ports are labeled on the synthesizer modules, but numbers are not physically printed on the module.

J-PORT DEFINITIONS

PORT	LABEL	DESCRIPTION
J1	RF Output	SMA Jack
J2	Modulation Input	SMA Jack, Multiplexed, 50ohm Input Trigger/Pulse mod: 1.2 V Threshold
J3	10/100 MHz Ref. Input	SMA Jack: 10MHz/100MHz Reference Input (software selectable) 10MHz: 0dBm to +10dBm Input (PLL Lock Range: ± 1ppm) 100MHz: +4 dBm out, ± 2 dB Input (Internal OCXO is shut off)
J4	100MHz Ref. Output	SMA Jack: 100MHz Reference Output 100MHz: +4 dBm out, ± 2 dB (nom)
J5	HSM ¹ Data I/O - Power	2mm, 20pin (2x10) Milli-grid Shrouded Pin Header (detent type) Contains Power, Ground, SPI and Status Indicators
J6	HSE ¹ Data I/O - Power	2mm, 20pin (2x10) Milli-grid Shrouded Pin Header (detent type) Contains Power, Ground, SPI and Status Indicators
Display	Status	Tri-color LED Indicator Panel: GREEN = Power Good YELLOW = Communication Active / Busy / Not Ready RED = ERROR (i.e. no 10MHz PLL lock, Unleveled, etc.)

J5/J6 (SPI) MATING CONNECTOR PART NUMBERS

APPLICATION	MOLEX PART NUMER	DESCRIPTION
IDC Ribbon	Molex 87568-2093	2mm Milli-Grid, 20pin (2x10) Female, Polarization and Ramp Locking
Vertical PCB Thru Hole	Molex 79107-7009	2mm Milli-Grid, 20pin (2x10) Female, NO Polarization or Ramp Locking
Vertical PCB SMT	Molex 79109-1009	2mm Milli-Grid, 20pin (2x10) Female, NO Polarization or Ramp Locking

¹ HSM refers to the lower section of the synthesizer, while HSE refers to the high-frequency upconversion section. Each has a 20-pin connector.

J5 PINOUT CONFIGURATION

PIN No.	Label	PIN No.	Label
1	GND	2	GND
3	+5V, (1.5A Max)	4	+5V tied to pin 3
5	+12V, (600mA Max)	6	N.C. (reserved)
7	NC	8	N.C. (reserved)
9	/RESET (/RESET47k PU)	10	N.C. (reserved)
11	/CS (Module Select - 47k PU)	12	N.C. (reserved)
13	SDO (Synthesizer Data Output)	14	Power Good (OC – 47k PU to 3.3V)
15	SDI (Synthesizer Data Input)	16	/ERROR (OC – 47k PU to 3.3V)
17	SCLK (Synthesizer Clock Input)	18	/BUSY (OC – 47k PU to 3.3V)
19	GND	20	GND

J5 PIN LABEL DEFINITIONS

PIN Label	DEFINITION
+5V	Nominally pulls 1.2A from the +5V Rail. Initially at power on the draw will be 100mA then increase as subsystems power-on. Tolerance +8% to -1%. 4.95V to 5.4V.
+12V [or +15V]	Nominally 300mA draw from this pin (T=25C). 600mA draw at startup for at least 5 mins for OCXO power on. +15V O.K.. but increases power dissipation.
NC	No Connect. Voltage supply pin. Not currently used.
/RESET	Active low on this pin put the module in reset, releasing it returns to reset operation. Module is ready 2-3 seconds after /RESET is released. 47K pullup to 3.3V in parallel to 0.01uF cap to ground.
/CS	Communications chip select, active low. 47K pullup on this line. /CS must be low for any communication to occur. Allows for multiple synthesizer modules on 1 SPI bus. 3.3V logic levels, 5V tolerant.
SDO	Synthesizer (module/slave) Data Output. Connects to Master Serial Data Input (Active when chip select is low. High-Z when /CS is high. 47K pulldown. 3.3V logic levels, 5V tolerant.
SDI	Synthesizer (module/slave) Data Input. Connects to Master Serial Data Output (High-Z input on module. 3.3V logic levels, 5V tolerant. 47K pulldown.
SCLK	SPI Clock (slave clock input). Idle Low, Active High. Data is transitioned into the module on a rising low to high transition. Data is transitioned out on the same edge and is valid on the falling edge of SCLK. 3.3V logic levels, 5V tolerant. 47K pulldown.
Power Good	Open collector output, 47k pullup to 3.3V. When high, power is healthy. When low, either voltages or currents are problematic. Module may not operate correctly. There is a 0.5 second delay from when power is applied to a valid PowerGood. Actual PowerGood may take up to 2 seconds to go high due to some very stable internal references that are settling. This may be multiplexed with other HSM6001 synthesizers.
/ERROR	Open collector output, 47k pullup to 3.3V. Nominally high. If an error condition occurs, such as a PLL unlock or un-leveled condition, this will go active low. This can be multiplexed with other HSM6001 synthesizers.
READY or /BUSY	Open collector output, 47k pullup to 3.3V. Nominally high. After an SPI communication, if a command has been issued, then the /BUSY will go active low until that command is finished. During this time no communication may occur and SPI bus will be asleep.

J6 PINOUT CONFIGURATION

PIN No.	Label	PIN No.	Label
1	GND	2	GND
3	+ 5V (2A Max)	4	+5V tied to pin 3
5	+12V (700mA Max)	6	N.C. (reserved)
7	-12V (50mA Max)	8	N.C. (reserved)
9	/RESET (10k PU)	10	N.C. (reserved)
11	/CS (Module Select - 47k PU) *	12	N.C. (reserved)
13	SDO (Synthesizer Data Output)	14	Power Good (OC – 47k PU to 3.3V)
15	SDI (Synthesizer Data Input)	16	/ERROR (OC – 47k PU to 3.3V)
17	SCLK (Synthesizer Clock Input)	18	/BUSY (OC – 47k PU to 3.3V)
19	GND	20	GND

J6 PIN LABEL DEFINITIONS

PIN Label	DEFINITION
+5V	Nominally pulls 1.5A from the +5V Rail. Initially at power on the draw will be 100mA then increase as subsystems power-on. Tolerance +8% to -1%. 4.95V to 5.4V. The value supplied to the module can be checked via software.
+12V [or +15V]	±5%. Nominally 500mA from this pin (T=25C). The value supplied to the module can be checked via software.
-12V	±5%. Nominally 30mA from this pin (T=25C).
/RESET	Active low on this pin puts the module in reset, releasing it returns to reset operation. Module is ready 2-3 seconds after /RESET is released. 10K pullup to 3.3V in parallel to 10uF cap to ground.
/CS	Communications chip select, active low. 47K pullup on this line. /CS must be low for any communication to occur. Allows for multiple synthesizer modules on 1 spi bus. 3.3V logic levels, 5V tolerant.
SDO	Master Serial Data Input (synthesizer module/slave data out). Active when chip select is low. High-Z when /CS is high. 47K pulldown. 3.3V logic levels, 5V tolerant.
SDI	Master Serial Data Output (synthesizer module/slave data in). High-Z input on module. 3.3V logic levels, 5V tolerant. 47K pulldown.
SCLK	SPI Clock (slave clock input). Idle Low, Active High. Data is transitioned into the module on a rising low to high transition. Data is transitioned out on the same edge and is valid on the falling edge of SCLK. 3.3V logic levels, 5V tolerant. 47K pulldown.
Power Good	Open collector output, 47k pullup to 3.3V. When high, power is healthy. When low, either voltages or currents are problematic. Module may not operate correctly. There is a 0.5 second delay from when power is applied to a valid PowerGood. Actual PowerGood may take up to 2 seconds to go high due to some very stable internal references that are settling. This may be multiplexed with other HSM series synthesizers.
/ERROR	Open collector output, 47k pullup to 3.3V. Nominally high. If an error condition occurs, such as a PLL unlock or un-leveled condition, this will go active low. This can be multiplexed with other HSM series synthesizers.
READY or /BUSY	Open collector output, 47k pullup to 3.3V. Nominally high. After an SPI communication, if a command has been issued, then the /BUSY will go active low until that command is finished. During this time no communication may occur and SPI bus will be asleep.
N.C.	These are reserved lines for use in our communications module. They should be left floating.

SPI COMMUNICATIONS

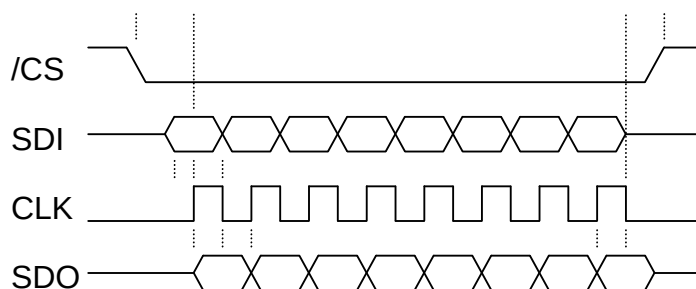
BUS OVERVIEW

The SPI bus is a byte oriented bus, sending 8bits at a time. Any number of bytes may be sent, from 1 byte to 64 bytes while chip select is low. Bytes sent beyond 64 bytes will be ignored. The data is held in a buffer until chip select goes high, initiating the parsing of the data and execution of the commands. The maximum speed of the bus is 10Mbps/s. Data may be written to the module and data may be received from the module. After a command is sent requesting data, the next transfer sends this data out on SDO. During the read, a new command may be send and will be parsed when chip select goes high. A read is always followed by a write with a read request.

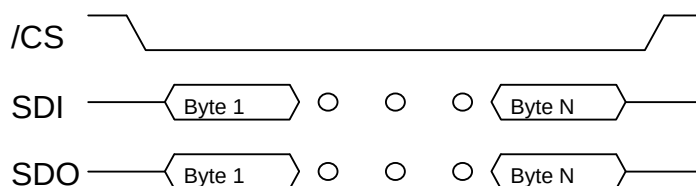
BUS HARDWARE PROTOCOL

Data is clocked into the module on the rising edge of sclk. Data is clocked out of the module on this same edge. Data output is valid on the falling edge of sclk. Data is only transferred when chip select is low. When chip select goes high, this initiates the parsing and execution of data.

SPI TIMING



The figure above demonstrates bit level timing where data is sampled into and out of the module on the rising edge of SCLK (Slave Clock). Data out is valid on the falling edge of SCLK.



The above figure displays how byte level communications occurs. Any number of bytes may be sent. After /CS goes high, the data is parsed and executed. If no data is sent, the SPI communications module simply resets itself and no parsing or execution of data occurs. If /CS goes high in the middle of a byte transfer (1-7 bits are sent instead of 8) this byte is ignored.

WARRANTY

All Holzworth synthesizers come with a standard 2 year 100% product warranty covering manufacturing defects. All product repairs and maintenance must be performed by Holzworth Instrumentation. Holzworth reserves the right to invalidate the warranty for any products that have been tampered with or used improperly. Refer to Holzworth Terms & Conditions of Sales for more details.

OPTIONS

Holzworth HSM series RF synthesizers have options to assist with better meeting specific systems requirements.

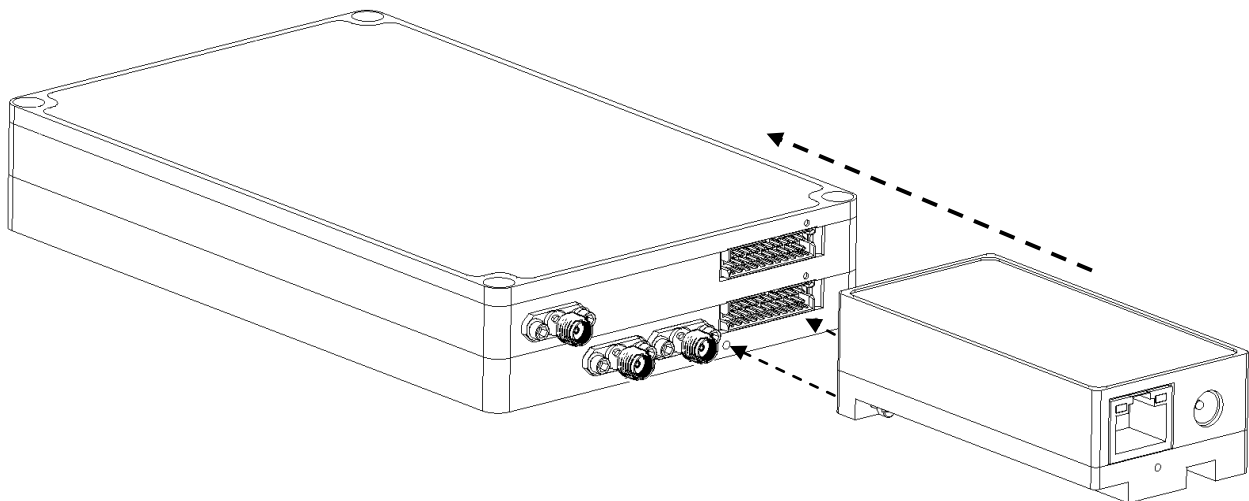
OPT-OCXO	10dB Improved Close to the Carrier Phase Noise
OPT-SYS3	Includes internal OCXO. Tested over extended temperature range with external 100MHz reference.

Communications modules are also made available for ease of integration or simply to match legacy laboratory communications requirements. USB and Ethernet communication modules can be purchased from Holzworth directly.

HCM6	USB Communications Module with power supply
HCM7	Ethernet Communications Module with power supply

HCM Communications Module Installation

The HCM Communication Module is an SPI to USB (or Ethernet) adapter that also includes a power supply adapter allowing the user to connect the RF synthesizer to standard AC power. The selected HCM Module creates a USB (or Ethernet) connection to a PC so that the Holzworth GUI, LabVIEW™, MATLAB™, etc. can be utilized to control the source. No drivers are required to run the Holzworth GUI.



Each variation of the HCM Communications Module securely fastens to the synthesizer and comes complete with an AC power supply and the appropriate cable. HCM modules are a recommended accessory as the first step in integrating the HSM series synthesizers via the SPI bus. More information is available upon request.

TECHNICAL SUPPORT

Email: support@holzworth.com

Phone: +1.303.325.3473 (option 2)



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