DC to 6 GHz, 45 dB TruPwr™ Detector with Envelope Threshold Detection

Preliminary Technical Data

ADL5904

FEATURES

RMS and Envelope Threshold Detection
Broad Input Frequency Range: DC to 6 GHz
RF Input Range: 45 dB (-30 dBm to +15 dBm)
RMS Linear-in-dB output, scaled 33 mV/dB
Input Envelope Threshold Detection and Latching
Programmable Threshold and Latch Reset Function
Fast Response Time: 20 ns from RFIN to Q/QBAR Latch
Operates at 3 V and 5 V from −55°C to +125°C
Low power: 3 mA at 3.0 V supply
Power-down capability to <100 µA
16-pin, 3mm x 3mm LFCSP package

APPLICATIONS

Transmitter Signal Strength Indication (TSSI)
Wireless Power Amplifier Input and Output Protection
Wireless Receiver Input Protection

FUNCTIONAL BLOCK DIAGRAM

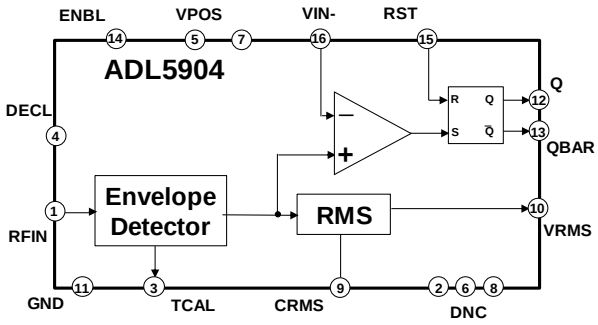

Figure 1. ADL5904 Block Diagram

GENERAL DESCRIPTION

The ADL5904 is a dual function RF detector that operates from DC to 6 GHz. It provides RMS power measurement along with a programmable envelope threshold detection function.

The RMS power measurement function has a 45 dB detection range, nominally from -30 dBm to +15 dBm*. It features low power consumption and an intrinsically ripple-free error transfer function.

The envelope threshold detection function compares the voltage from an internal envelope detector with a user-defined input voltage. When the voltage from the envelope detector exceeds the user-defined threshold voltage, an internal comparator captures and latches the event to an S-R flip flop.

The response time from the RF input signal exceeding the user-programmed threshold to the output latching is 20 ns. The latched event is held on the flip-flop until a reset pulse is applied.

The RF Input of ADL5904 is dc-coupled, allowing for operation down to arbitrarily low ac frequencies. It operates on either a 3V or 5V supply and consumes 3 mA. A disable mode reduces this current to 100 µA when a logic low is applied to the ENBL pin.

The ADL5904 is supplied in a 3 mm × 3 mm, 16-lead LFCSP for operation over the wide temperature range of −55°C to +125°C.

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SPECIFICATIONS

V_{POS} = 5 V, T_A = 25°C, Z_O = 50 Ω, C_{RMS} = 0.1 µF.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range			DC to 6000		MHz
RF INPUT INTERFACE	Pin RFIN				
Nominal Input Impedance	Single-ended drive, External shunt matching resistor		50		Ω
RMS Power Measurement	Pin RFIN, VRMS				
200 MHz – 6000 MHz					
±1.0 dB Dynamic Range	CW input, T_A = +25°C		45		dB
Maximum Input Level, ±1.0 dB*	Calibration at −25 dBm, −10 dBm, and 10 dBm		15		dBm
Minimum Input Level, ±1.0 dB	Calibration at −25 dBm, −10 dBm, and 10 dBm		-30		dBm
Deviation vs. Temperature	Deviation from output at 25°C				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		±0.5		dB
	−40°C < T_A < +85°C; P_{IN} = −20 dBm		±0.5		dB
Logarithmic Slope	−45 dBm < P_{IN} < 0 dBm; calibration at −30 dBm and -10 dBm		33		mV/dB
Logarithmic Intercept	−45 dBm < P_{IN} < 0 dBm; calibration at −30 dBm and -10 dBm		-40		dBm
Output Voltage	Pin = +10 dBm		1.6		V
	Pin = -20 dBm		0.6		V
VRMS Source/Sink Capability			TBD		mA
THRESHOLD DETECT and LATCH	Pin Q, QBAR, VIN-, RST				
Peak Envelope Power, Threshold Detection Range	PEP(dBm)=P_{RMS}(dBm)+Pk-to-Average Ratio(dB)		-30 to +15		dBm
Output Response Time	Transition time from RFIN exceeding VIN- threshold to Q and Qbar settled (VIN- = TBD V, Threshold overdrive = TBD dB, P_{IN} = −TBD dBm)		20		ns
Reset Time	Transition time from RST high to Q and Qbar settled		TBD		ns
Q, Qbar Source/Sink Current			TBD/TBD		mA
COMPARATOR INTERFACE	Pin VIN-				
VIN- Input Range			0 to 2		V
VIN- Input Bias Current			TBD		uA
FLIP FLOP RESET INTERFACE	Pin RST				
Logic High Level		TBD		VPOS	V
Logic Low Level		0		TBD	V
Input Bias Current			TBD		
POWER-UP INTERFACE	Pin ENBL				
Voltage Level to Enable		TBD		VPOS	V
Voltage Level to Disable		0		TBD	V
Input Bias Current			TBD		

Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY INTERFACE	Pin VPOS				
Supply Voltage		3.0		5.0	V
Quiescent Current	T_A = 25°C, No signal at RFIN, VPOS=5V		3		mA
	T_A = 25°C, No signal at RFIN, VPOS=3V		3		mA
	T_A = 125°C, No signal at RFIN, VPOS =5V		TBD		mA
Power-Down Current	ENBL = LOW, VPOS = 3V		100		µA
	ENBL = LOW, VPOS = 5V		100		µA

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

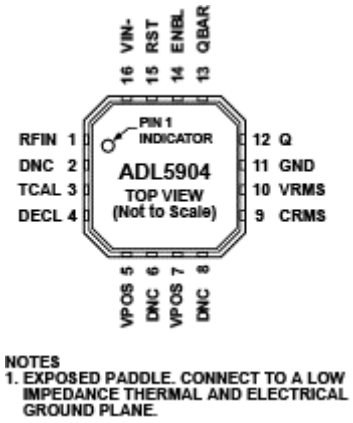


Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	The ADL5904's RFIN pin is dc-coupled and is not internally matched. A broadband 50 ohm match is achieved using an external 82.5 ohm shunt resistor with a 0.47uF ac-coupling capacitor placed between the shunt resistor and the RF input. Smaller ac-coupling capacitor values can be used if low frequency operation is not required.
2,6,8	DNC	No Connect.
3	TCAL	Threshold calibration. The voltage on this pin is used to determine the correct threshold voltage that should be applied to Pin 16 (VIN-) to set a particular RF power threshold. This is a two-step process. First measure the output voltage on TCAL with no RF signal applied to RFIN (this voltage will be approximately 750 mV). Next apply the RF input power to RFIN which should cause the circuit to trip and again measure the voltage on the TCAL pin. The difference between these two voltages is equal to the threshold voltage that should be applied to VIN- during operation.
4	DECL	Internal Decoupling. Bypass this pin to ground using a 4 Ohm resistor connected in series with a 100 nF capacitor.
5,7	VPOS	Supply Voltage range is 3V to 5V. Decoupling capacitors should be placed on Pin 5. There is no requirement for power supply decoupling capacitors on Pin 7
9	CRMS	RMS Averaging Capacitor. Connect a capacitor between DECL pin and CRMS pin to set the appropriate level of RMS averaging. The value of the rms averaging capacitor should be set based on the peak-to-average ratio and bandwidth of the input signal and based on the desired output response time and residual output noise.
10	VRMS	RMS Detector Output. The output from the VRMS pin is proportional to the logarithm of the rms value at the input level.
11	GND	Device Ground. Connect GND pin to system ground using a low impedance path. This pin should connect to the same ground as the exposed pad.
12,13	Q, Qbar	Differential digital outputs of threshold detect flip flop. Q latches high when the output of the internal envelope detector exceeds the threshold voltage on the internal comparator's VIN- input.
14	ENBL	Device Enable. Connect the ENBL pin to logic high to enable the device.
15	RST	Flip flop reset. Taking RST high clears the latched flip flop output, setting outputs Q and Qbar to low and high respectively.
16	VIN-	Inverting input to threshold detect comparator. The voltage on this pin is compared to the output voltage of the internal envelope detector which is driven by the RF input level. If the output voltage of the envelope detector exceeds the voltage on VIN-, the flip flop will latch the Q output to high and the Qbar output to low. VIN- should be taken low when Enable is low to avoid ESD diode turn-on. If

		VIN- is left floating, the pin will be pulled high internally which will disable the PA protection function. This will reduce the operating current by TBD mA.
	EPAD	Exposed Pad. Since most ground current flows through the EPAD, it's essential to have good thermal and electrical connection to the pcb ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

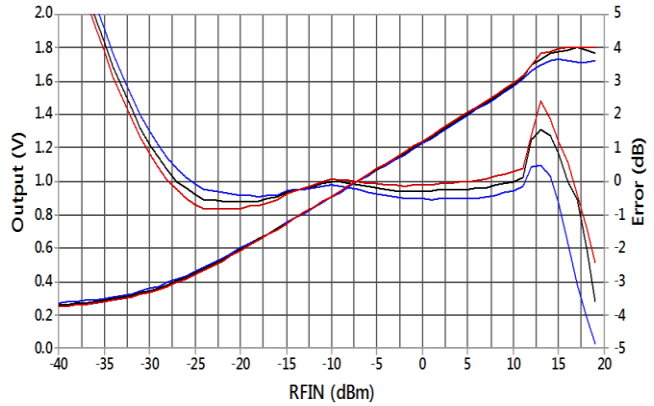


Figure 2. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 10 MHz

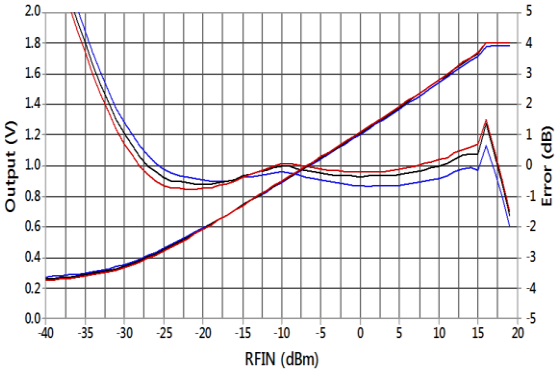


Figure 3 V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 900 MHz

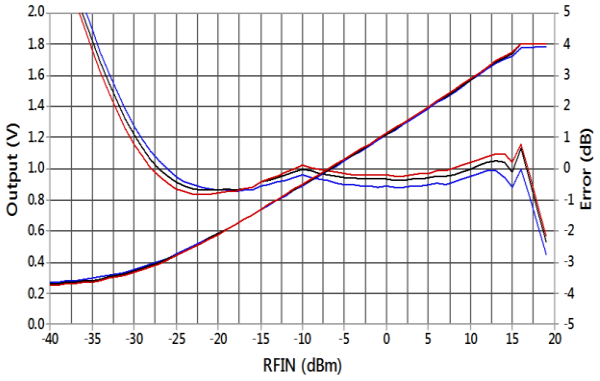


Figure 4. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 1.9 GHz

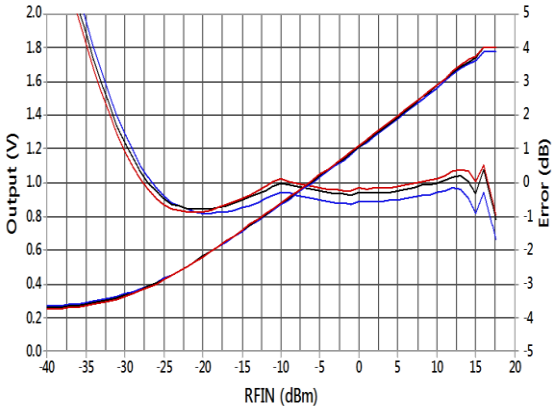


Figure 5 V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 2.6 GHz

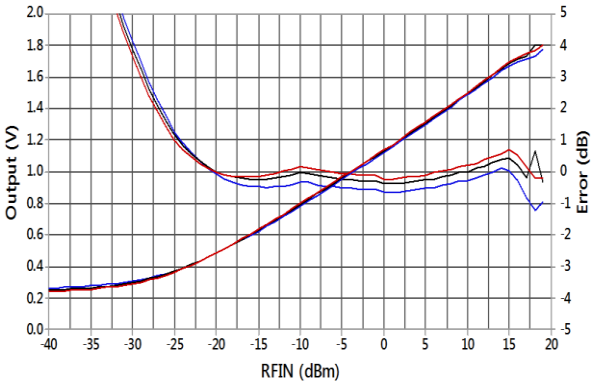


Figure 6. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 3.5 GHz

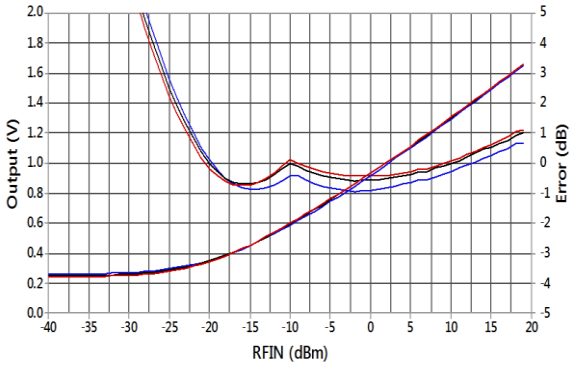


Figure 7. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 5.8 GHz

EVALUATION BOARD

The ADL5904-EVALZ is a fully populated, 4-layer, FR4-based evaluation board. A power supply of either 3V or 5V should be applied to the VPOS and GND test loops. To exercise the RMS detector portion of the circuit, the RF signal to be measured should be applied to the RFIN SMA connector. The corresponding RMS output voltage is then available on the VRMS SMA connector and on the TP1 test point. To operate the Threshold Detect circuitry, the RF signal that is being monitored should again be applied to the RFIN SMA connector. The dc threshold voltage that should cause the circuit to trip should be applied to the VIN_N SMA connector or to the TPVIN_N yellow test point. The internal S/R flip-flop should be reset by pressing the RST button.

Detailed configuration options for the evaluation board are listed in Table 3.

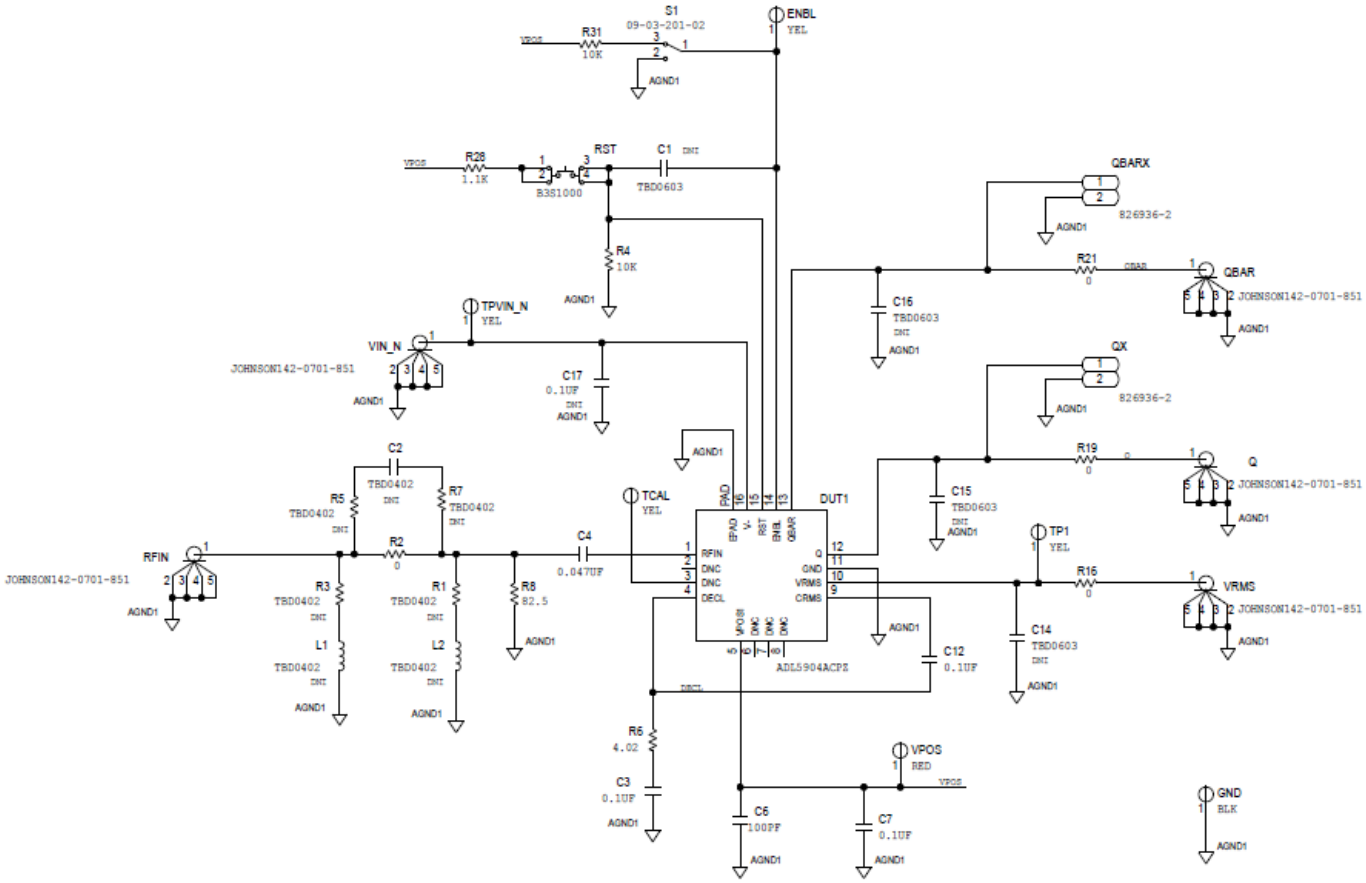
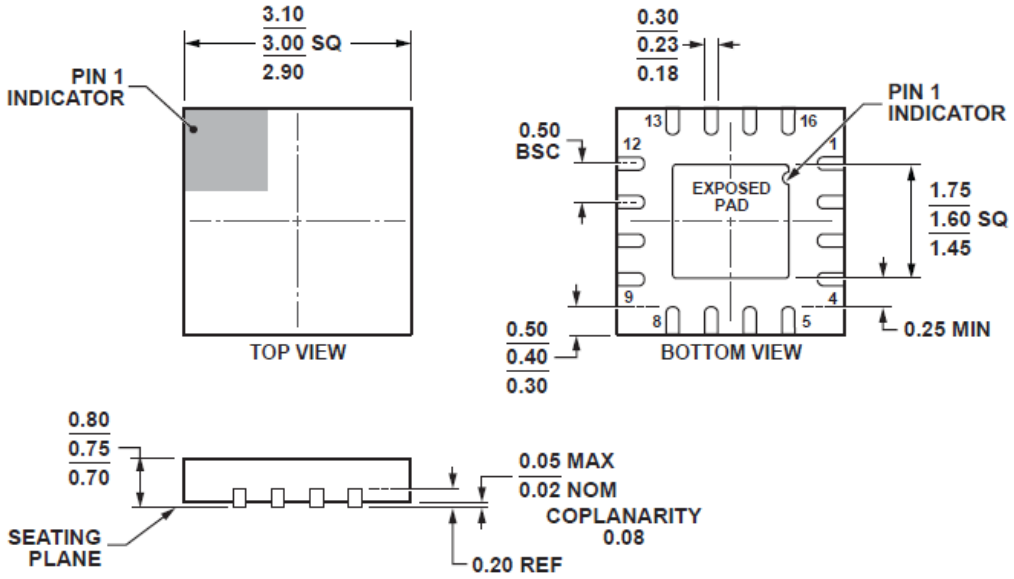


Figure 2. Evaluation Board Schematic

Table 3. Evaluation Board Configuration Options

Component	Function/Notes	Default Values
RFIN, R1, R2, R3, R5, R7, R8, L1, L2, C2, C4	**RF Input:** The RF input signal to the ADL5904 should be applied to the SMA connector labelled RFIN. The ADL5904's RFIN pin (Pin 1) is dc-coupled and is not internally matched. A broadband 50 ohm match is achieved using an external 82.5 ohm shunt resistor with a 0.47uF ac-coupling capacitor placed between the shunt resistor and the RF input. An external pre-emphasis network can be built to improve flatness vs frequency using the components between R8 and the RFIN SMA connector.	C4= 0.47uF (0402) R8 = 82.5 Ω (0402) R2 = 0 Ω (0402) R1,R3,R5,R7 = open (0402) L1,L2 = open (0402) C2 = open (0402)
TCAL, VIN_N, TPVIN_N, C17,	**TCAL:** The output voltage from the Threshold Calibration pin (TCAL, Pin 3) is available on the yellow TCAL clip lead. The voltage on this pin is used to determine the correct threshold voltage that should be applied to Pin 16 (VIN-) to set a particular RF power threshold This is a two-step process. First measure the output voltage on the TCAL yellow clip lead with no RF signal applied to RFIN (this voltage will be approximately 750 mV). Next apply the RF input power to RFIN which should cause the circuit to trip and again measure the voltage on the TCAL yellow clip lead. The difference between these two voltages is equal to the voltage that should be applied to VIN- during operation. This voltage can be either applied to the VIN_N SMA connector or to the TPVIN_N yellow clip lead. C17 can be used to provide noise decoupling of the applied input voltage.	C17 = open (0603)
R6, C3	**DECL Internal Decoupling Node:** A resistor in series with a capacitor to ground should be connected to the ADL5904's DECL pin (Pin 4).	C3 = 100 nF (0402) R6 = 4.02 Ω (0402)
VPOS, GND, C7, C6	**Power Supply Interface:** Apply the power supply for the evaluation board to the VPOS (red) and GND (black) test loops. The nominal supply decoupling consists of a 100 pF capacitor and a 0.1 µF capacitor, with the 100pF capacitor placed closest to the VPOS pin (pin 5).	C7 = 0.1 µF (0402), C6 = 100 pF (0402)
VRMS, TP1, R16, C14	**Output Interface:** The rms output voltage is available on the VRMS SMA connector or on the TP1 yellow clip lead.	R16 = 0 Ω (0402) C14 = open (0603)
C12	**RMS Averaging Capacitor:** The value of the rms averaging capacitor should be set based on the peak-to-average ratio and bandwidth of the input signal and based on the desired output response time and residual output noise.	C12 = 0.1 µF (0402)
Q, QBAR, QX, QBARX, R19, R21 C15, C16	**Threshold Detect Output (Q and Qbar):** The threshold detect flip-flop outputs (Q and Qbar) are available on the SMA connectors labelled Q and QBAR and on the 2-pin headers labelled QX and QBARX. To test the response time of Q and QBAR, remove R19 and R21 and probe QX and QBARX with low capacitance FET probes.	C15 = C16= open (0603) R19, R21 = 0 Ω (0603)
ENBL, S1, R31	**Enable Interface:** The ADL5904 can be enabled by applying 3-5V to the ENBL SMA connector or using the S1 switch. The enable voltage should equal to but not greater than the supply voltage (3V to 5V).	R31 = 10 KΩ (0603)
RST push-button Switch R4, C1, R28	**Threshold Detect Reset:** The Threshold Detect flip-flop is reset using the RST push-button switch. The RST switch is connected the VPOS supply voltage through a 1.1K resistor (R28). A 100K pull-down resistor (R4) is connected to the ADL5904's RST pin. This pulls RST low in the absence of any other stimulus. The ADL5904 will normally power up with the Q and QBAR outputs high and low respectively. A reset-on-power-up circuit can be implemented by installing a capacitor on C1. When the VPOS supply is turned on, this will cause RST to go high momentarily before being pulled low by R4.	R4 = 10 KΩ (0603) R28 = 1.1 KΩ (0603) C1 = open (0603)
VIN_N, TPVIN_N, C17	**Threshold Detect Level Set:** The voltage applied to the VIN_N SMA connector or to the TPVIN_N yellow test loop drives the inverting input of the threshold detect comparator (V_{IN}-) and thereby defines the RF power level that will trip the threshold detect comparator and flip-flop. The threshold detect voltage can be optionally decoupled using C17.	C17 = open (0603)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 x 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

Figure 4. Package Drawing

PR13838-0-5/16(PrF)