Freescale Semiconductor
Technical Data

Document Number: AFT27S006N
Rev. 3, 11/2014

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 28.8 dBm RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 728 to 3600 MHz.

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 65 mA, P_{out} = 28.8 dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

700 MHz

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
728 MHz	24.3	20.2	9.9	-45.6	-19
748 MHz	24.4	19.9	9.9	-45.9	-17
768 MHz	24.2	19.4	9.8	-46.2	-13

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 70 mA, P_{out} = 28.8 dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.(1)

2100 MHz

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	22.2	18.3	9.2	-42.3	-14
2140 MHz	22.8	19.8	9.5	-44.6	-17
2170 MHz	22.5	20.2	9.3	-46.0	-13

2300 MHz

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2300 MHz	22.9	20.9	9.8	-41.0	-10
2350 MHz	23.5	21.5	9.4	-40.8	-24
2400 MHz	23.0	22.4	8.9	-41.0	-11

2600 MHz

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2500 MHz	20.4	19.4	9.5	-44.0	-7
2600 MHz	22.0	21.2	9.1	-42.5	-16
2700 MHz	20.9	20.3	8.5	-40.9	-7

3500 MHz

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
3400 MHz	16.1	14.3	9.0	-44.1	-9
3500 MHz	17.9	16.4	9.1	-46.2	-13
3600 MHz	16.0	16.7	8.7	-44.4	-4

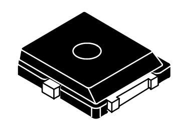
1. All data measured in fixture with device soldered to heatsink.

Features

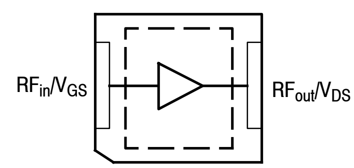
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Universal Broadband Driver
- In Tape and Reel. T1 Suffix = 1000 Units, 16 mm Tape Width, 7-inch Reel.

AFT27S006NT1

728-3600 MHz, 28.8 dBm AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



PLD-1.5W PLASTIC



(Top View)

Note: The center pad on the backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 0.76 W CW, 28 Vdc, I_{DQ} = 70 mA, 2140 MHz	$R_{\theta JC}$	3.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Machine Model (per EIA/JESD22-A115)	A
Charge Device Model (per JESD22-C101)	III

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

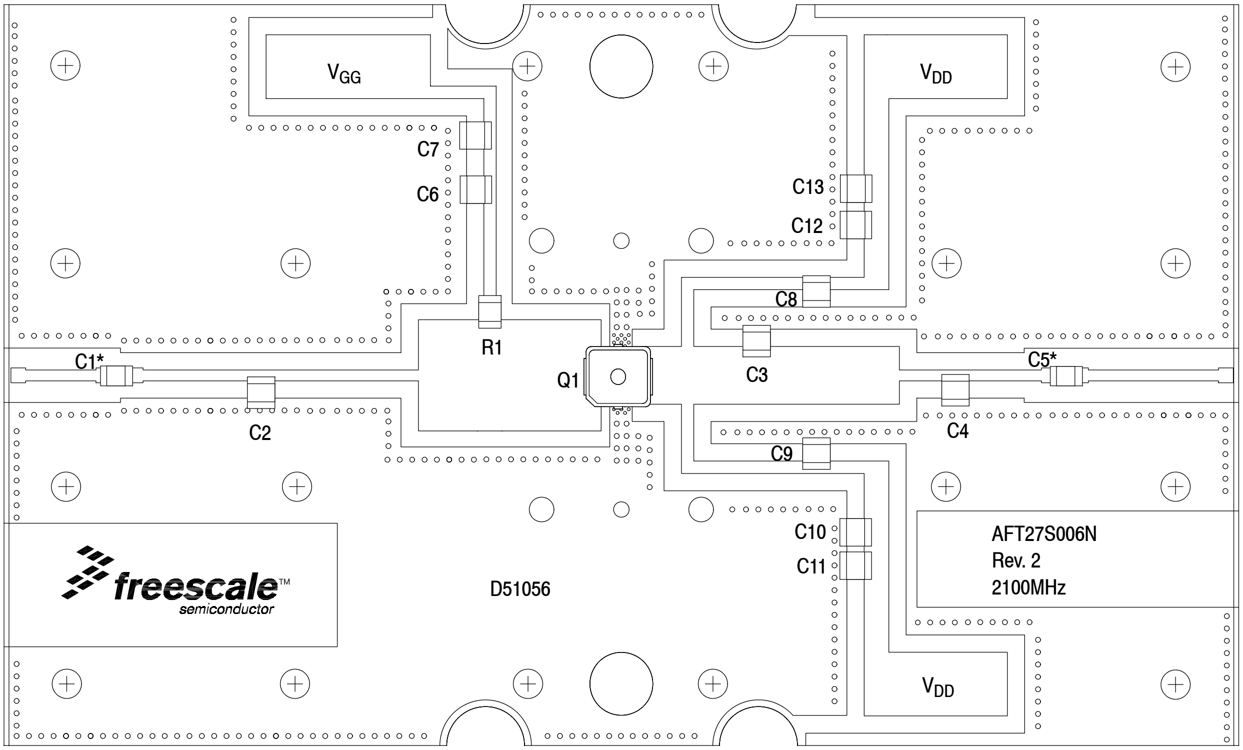
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 7.7 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 70 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 6 Vdc, I_D = 77 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 70 mA, P_{out} = 28.8 dBm Avg., f = 2170 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	21.0	22.0	24.5	dB
Drain Efficiency	η_D	17.0	20.0	—	%
Adjacent Channel Power Ratio	ACPR	—	-44.0	-38.5	dBc
Input Return Loss	IRL	—	-16	-10	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 70 mA, f = 2140 MHz					
VSWR 5:1 at 32 Vdc, 8.1 W CW Output Power (3 dB Input Overdrive from 6 W CW Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 70 mA, 2110-2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	6	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110-2170 MHz frequency range.)	Φ	—	-10.2	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	80	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 28.8 dBm Avg.	G_F	—	0.053	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.004	—	dB/°C



*C1 and C5 are mounted vertically.
NOTE: All data measured in fixture with device soldered to heatsink.

Figure 2. AFT27S006NT1 Test Circuit Component Layout — 2110-2170 MHz

Table 6. AFT27S006NT1 Test Circuit Component Designations and Values — 2110-2170 MHz

Part	Description	Part Number	Manufacturer
C1, C5, C6, C8, C9	9.1 pF Chip Capacitors	ATC100B39R1JT500XT	ATC
C2	1.2 pF Chip Capacitor	ATC100B1R2JT500XT	ATC
C3	2.7 pF Chip Capacitor	ATC100B2R7JT500XT	ATC
C4	1.5 pF Chip Capacitor	ATC100B1R5JT500XT	ATC
C7, C10, C11, C12, C13	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
Q1	RF Power LDMOS Transistor	AFT27S006NT1	Freescale
R1	4.75 Ω, 1/4 W Chip Resistor	CRCW12064R75FNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D51056	MTL

TYPICAL CHARACTERISTICS — 2110-2170 MHz

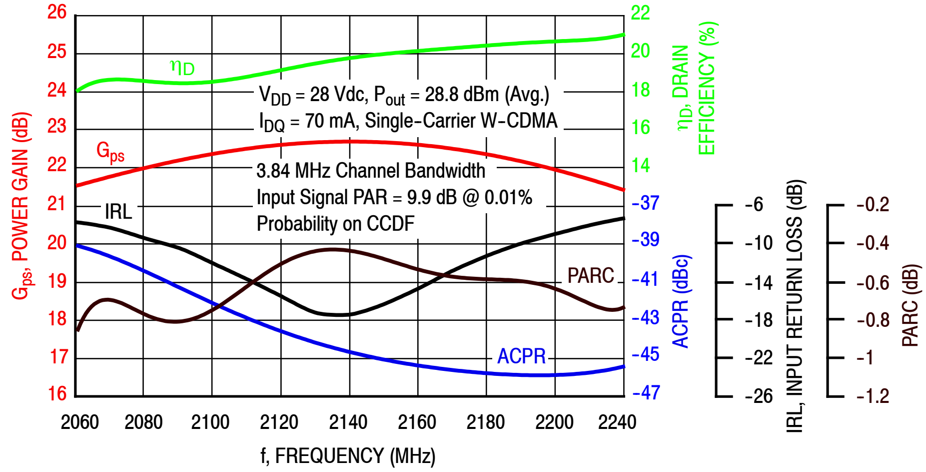


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28.8 dBm Avg.

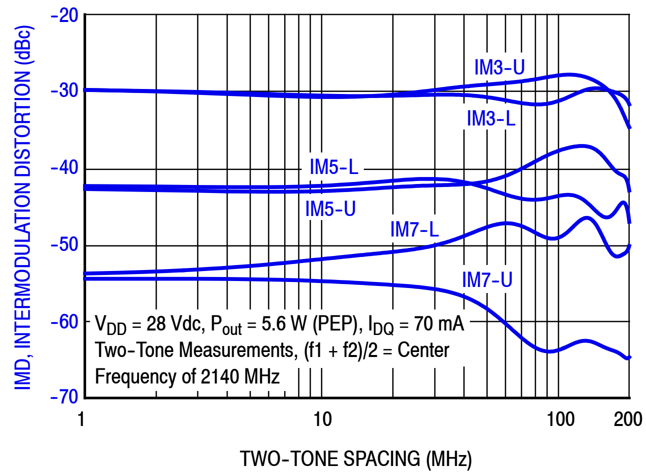


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

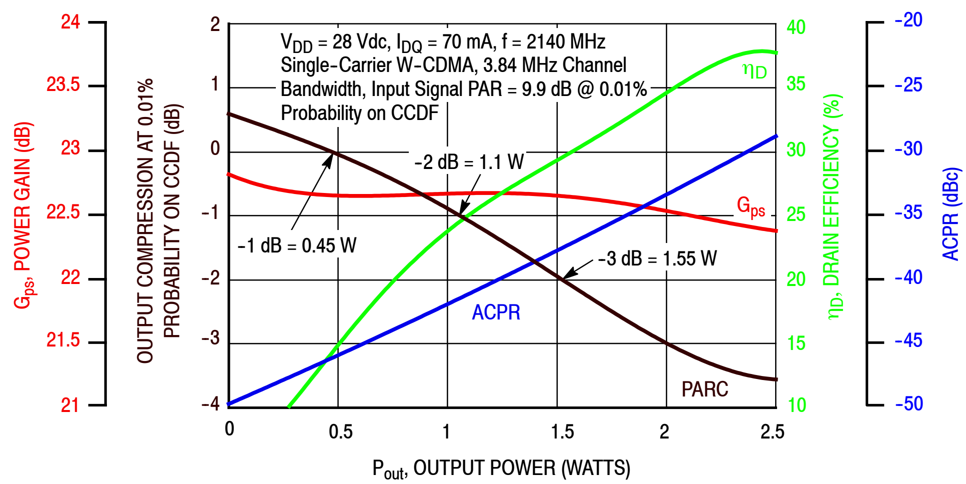


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

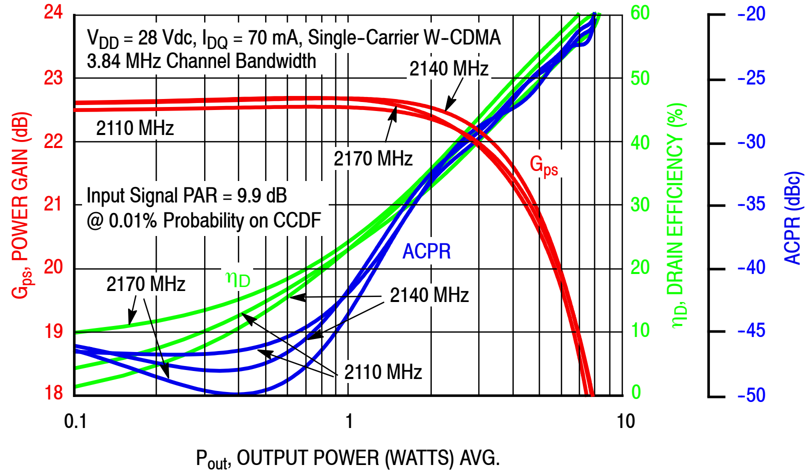


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

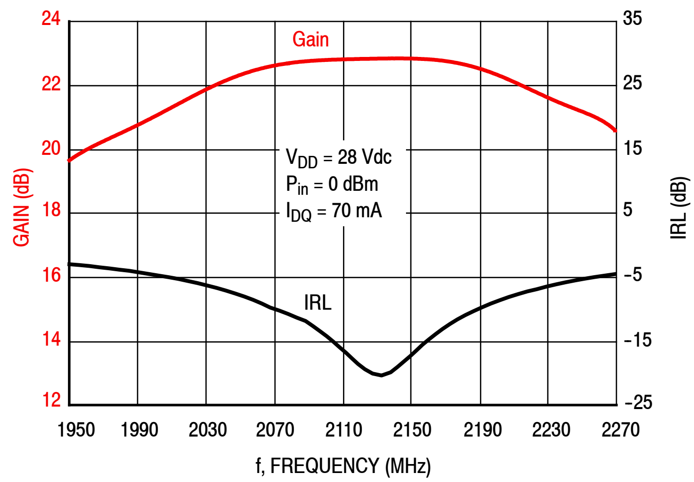


Figure 7. Broadband Frequency Response

Table 7. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 67 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.63 + j1.52	0.727 – j1.20	8.26 + j8.38	22.0	39.4	9	60.6	–12
2140	1.08 + j1.13	0.795 – j1.16	9.17 + j8.20	21.9	39.4	9	59.9	–15
2170	1.12 + j0.824	0.833 – j1.23	8.84 + j7.80	21.8	39.6	9	60.7	–15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.63 + j1.52	0.648 – j1.04	10.1 + j7.90	19.7	40.2	11	60.6	–17
2140	1.08 + j1.13	0.73 – j0.977	10.4 + j7.71	19.6	40.2	11	59.7	–22
2170	1.12 + j0.824	0.815 – j0.997	10.4 + j7.39	19.6	40.3	11	60.5	–21

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

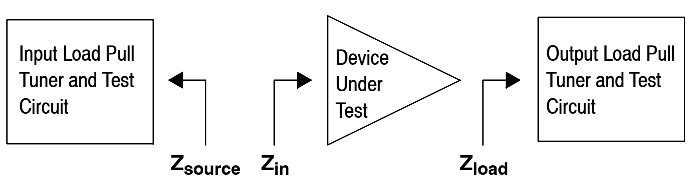
Table 8. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 67 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.63 + j1.52	0.602 – j1.19	4.69 + j12.4	24.1	37.5	6	69.4	–19
2140	1.08 + j1.13	0.677 – j1.15	5.12 + j11.9	24.0	37.9	6	68.4	–23
2170	1.12 + j0.824	0.708 – j1.17	4.92 + j11.7	24.0	37.8	6	69.4	–24

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	1.63 + j1.52	0.562 – j1.04	5.40 + j12.0	21.8	38.6	7	69.8	–26
2140	1.08 + j1.13	0.635 – j0.985	5.45 + j11.6	21.8	38.7	7	68.1	–32
2170	1.12 + j0.824	0.716 – j0.996	5.75 + j11.3	21.6	38.9	8	68.6	–30

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

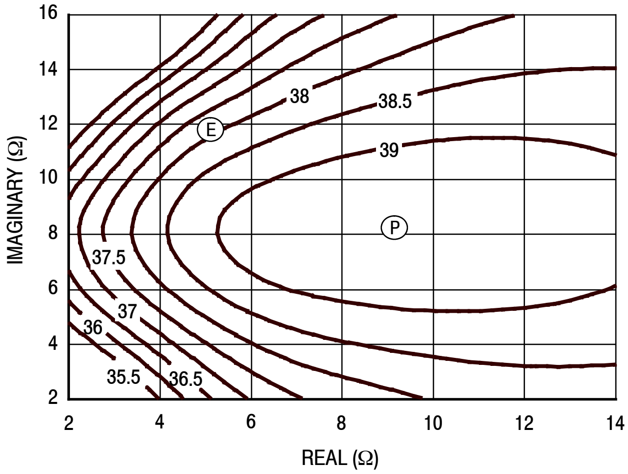


Figure 8. P1dB Load Pull Output Power Contours (dBm)

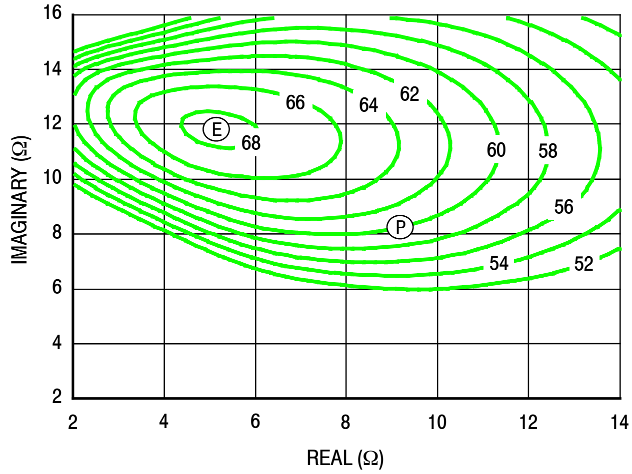


Figure 9. P1dB Load Pull Efficiency Contours (%)

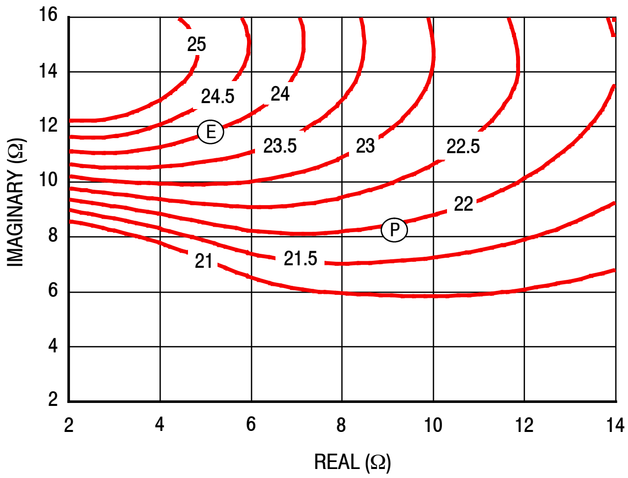


Figure 10. P1dB Load Pull Gain Contours (dB)

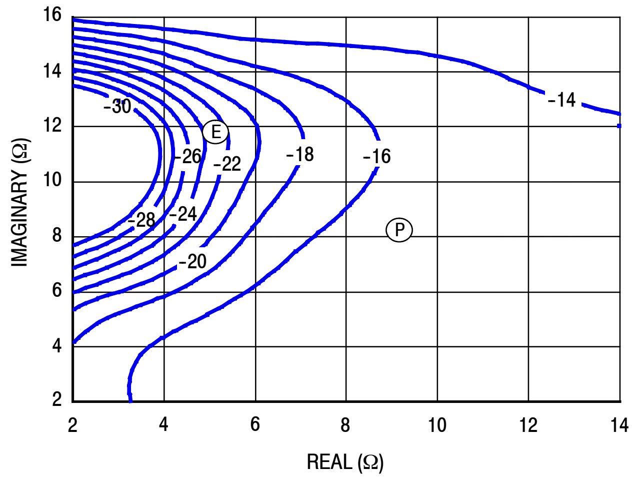


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power

E = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

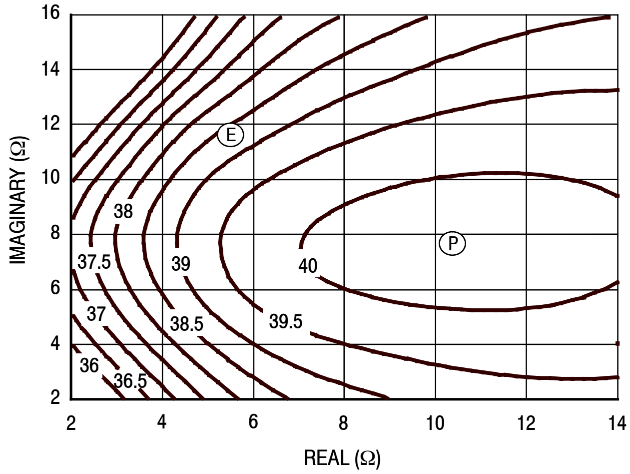


Figure 12. P3dB Load Pull Output Power Contours (dBm)

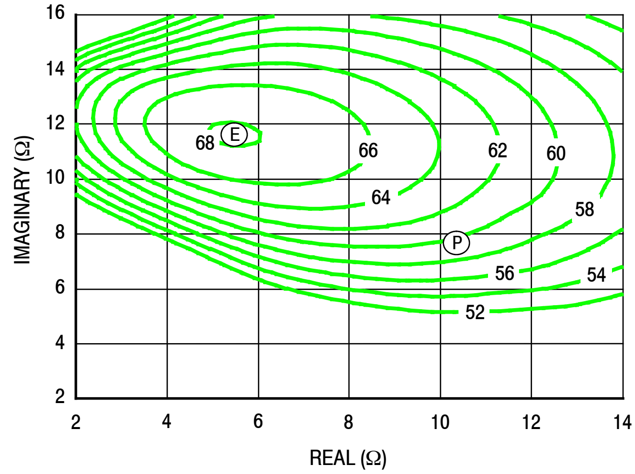


Figure 13. P3dB Load Pull Efficiency Contours (%)

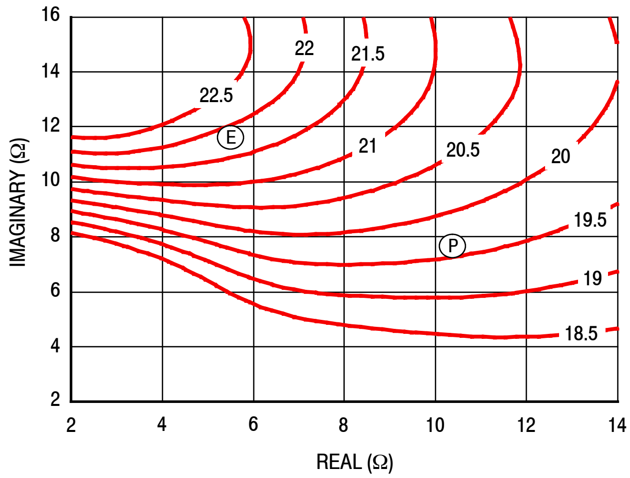


Figure 14. P3dB Load Pull Gain Contours (dB)

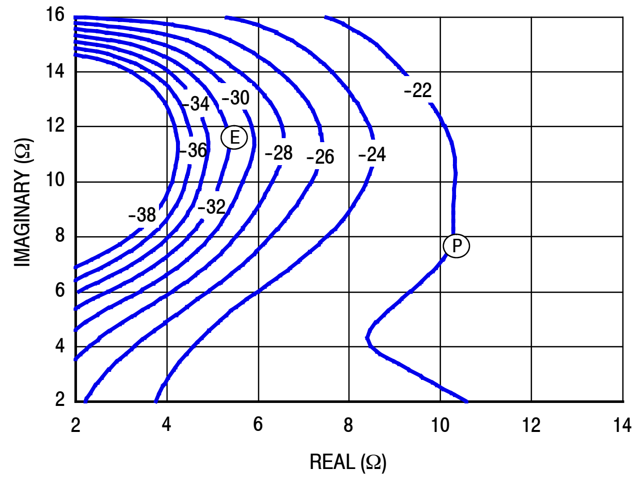


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

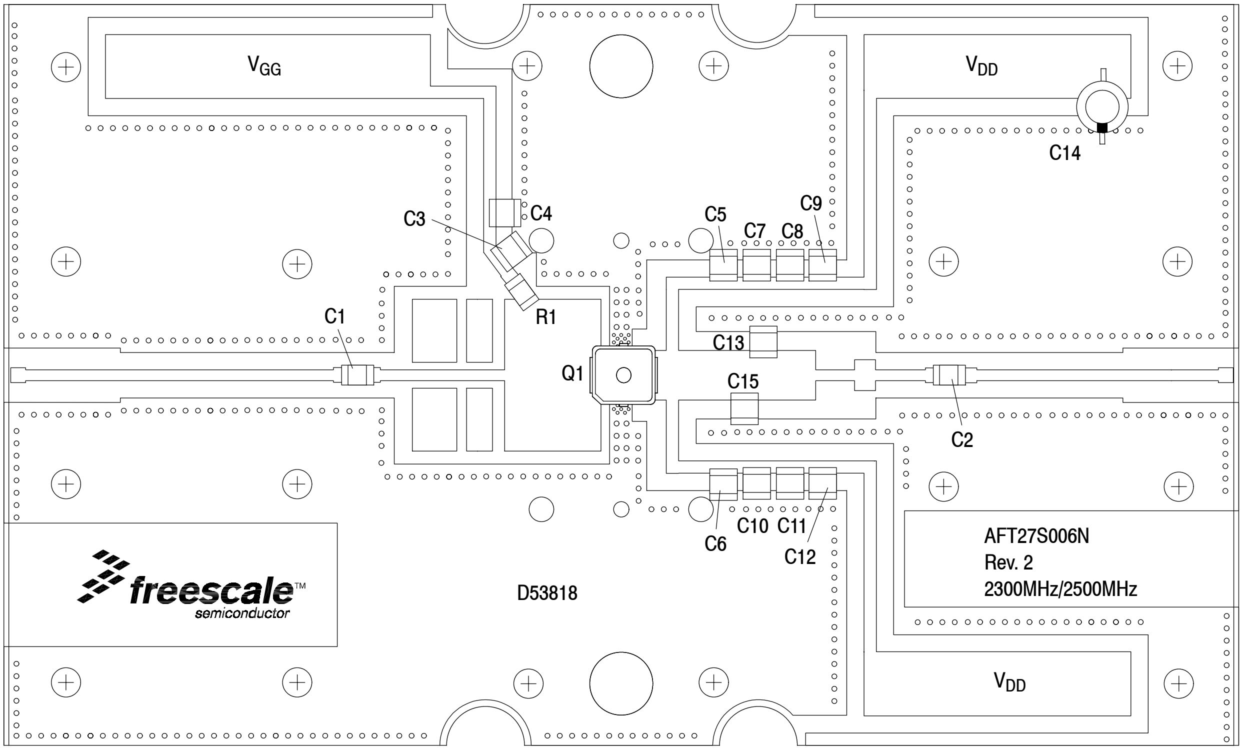
Gain

Drain Efficiency

Linearity

Output Power

2500-2700 MHz



NOTE: All data measured in fixture with device soldered to heatsink.

Figure 16. AFT27S006NT1 Test Circuit Component Layout — 2500-2700 MHz

Table 9. AFT27S006NT1 Test Circuit Component Designations and Values — 2500-2700 MHz

Part	Description	Part Number	Manufacturer
C1	8.2 pF Chip Capacitor	GQM2195C2E8R2CB12D	Murata
C2	7.5 pF Chip Capacitor	GQM2195C2E7R5CB12D	Murata
C3	8.2 pF Chip Capacitor	ATC100B8R2BT500XT	ATC
C4, C7, C8, C9, C10, C11, C12	10 μF, Chip Capacitors	GRM32E61H106KA12L	Murata
C5, C6	7.5 pF Chip Capacitors	ATC100B7R5BT500XT	ATC
C13	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C14	220 μF, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
C15	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
Q1	RF Power LDMOS Transistor	AFT27S006NT1	Freescale
R1	4.75 Ω, 1/4 W Chip Resistor	CRCW12064R75FNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D53818	MTL

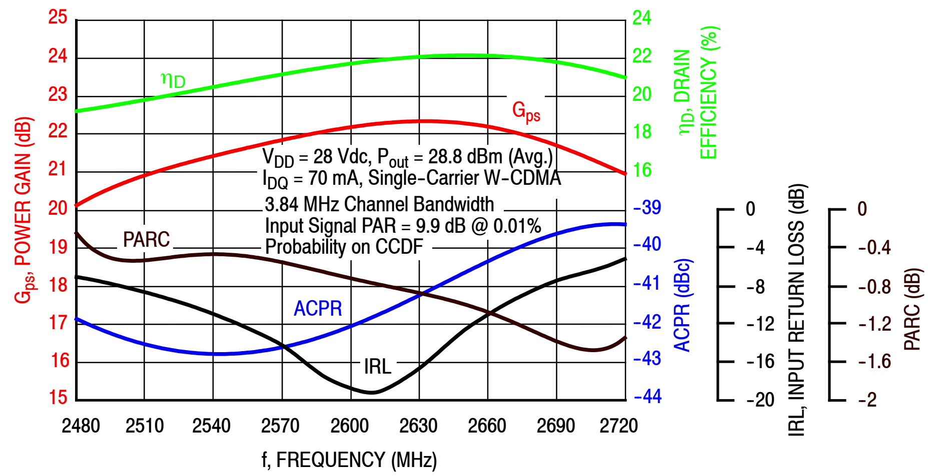


Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28.8 dBm Avg.

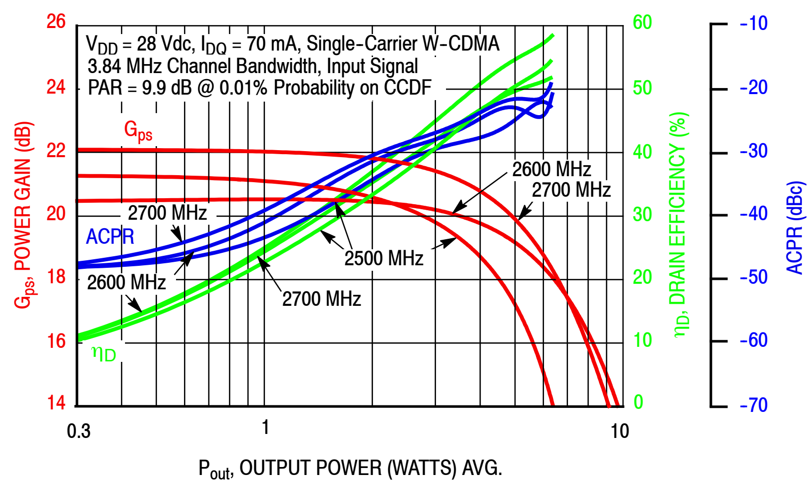


Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

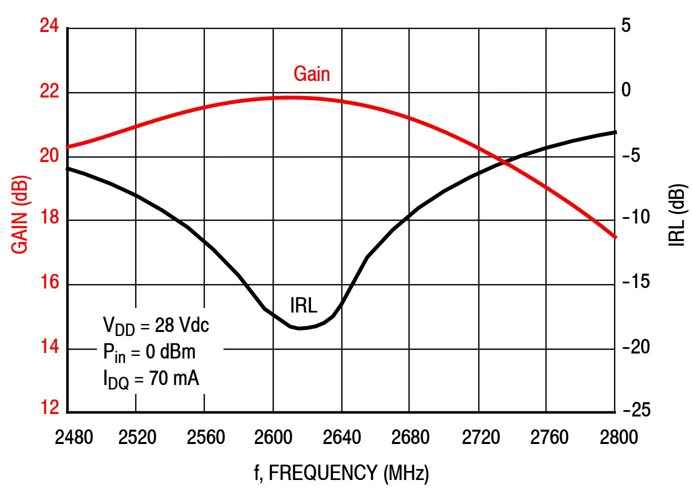
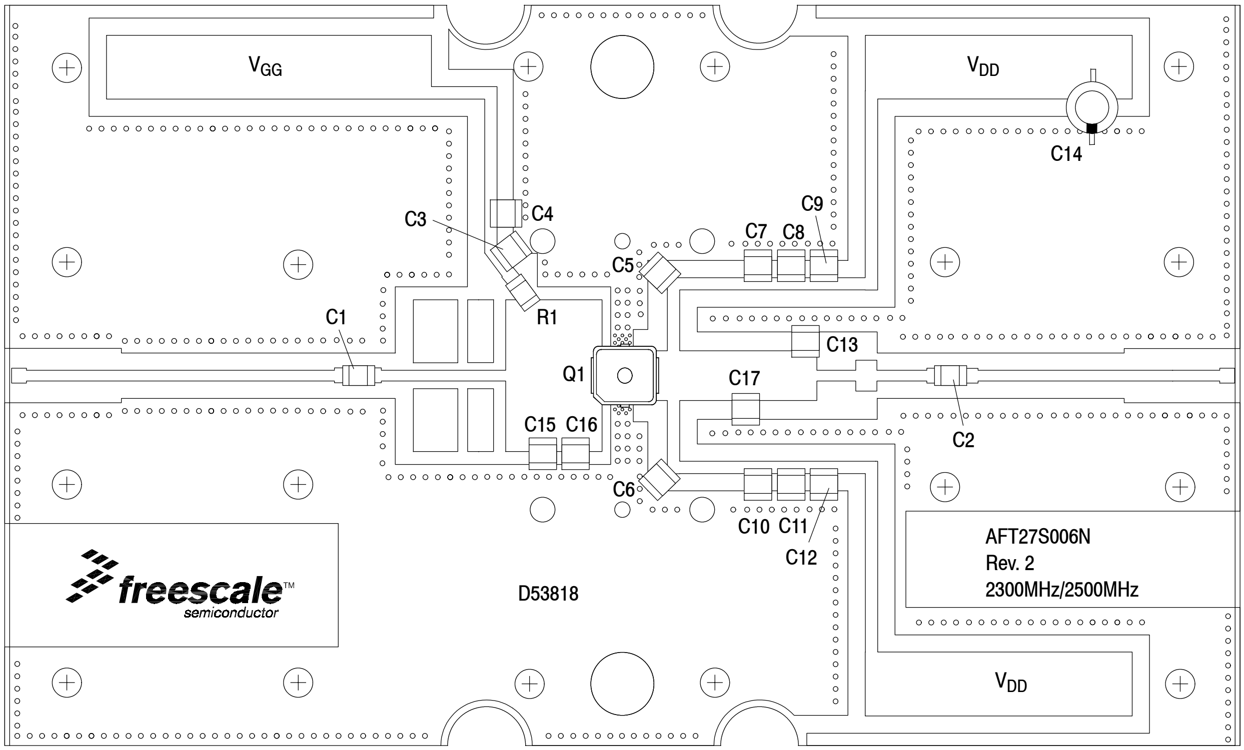


Figure 19. Broadband Frequency Response

2300-2400 MHz



NOTE: All data measured in fixture with device soldered to heatsink.

Figure 20. AFT27S006NT1 Test Circuit Component Layout — 2300-2400 MHz

Table 10. AFT27S006NT1 Test Circuit Component Designations and Values — 2300-2400 MHz

Part	Description	Part Number	Manufacturer
C1	8.2 pF Chip Capacitor	GQM2195C2E8R2CB12D	Murata
C2	7.5 pF Chip Capacitor	GQM2195C2E7R5CB12D	Murata
C3	8.2 pF Chip Capacitor	ATC100B8R2BT500XT	ATC
C4, C7, C8, C9, C10, C11, C12	10 μF Chip Capacitors	GRM32E61H106KA12L	Murata
C5, C6	7.5 pF Chip Capacitors	ATC100B7R5BT500XT	ATC
C13	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C14	220 μF, 50 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
C15	0.8 pF Chip Capacitor	ATC100B0R8CT500XT	ATC
C16	1.5 pF Chip Capacitor	ATC100B1R5CT500XT	ATC
C17	1.2 pF Chip Capacitor	ATC100B1R2CT500XT	ATC
Q1	RF Power LDMOS Transistor	AFT27S006NT1	Freescale
R1	4.75 Ω, 1/4 W Chip Resistor	CRCW12064R75FNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D53818	MTL

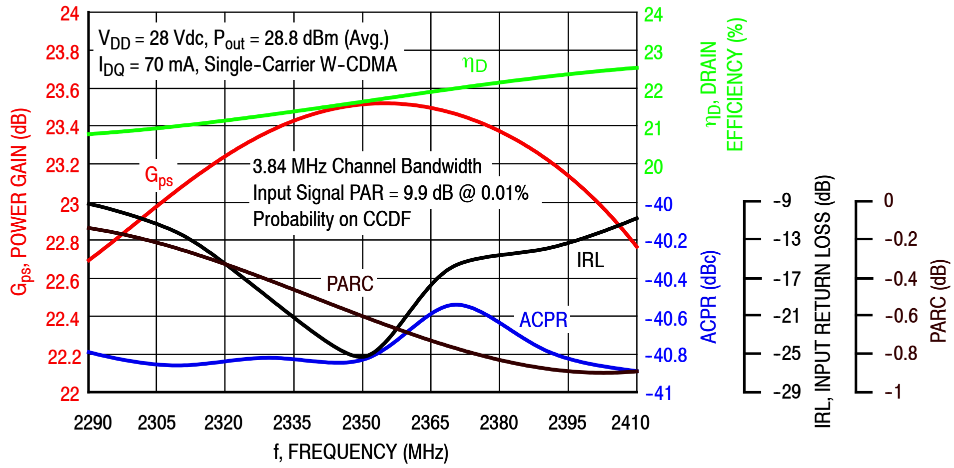


Figure 21. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28.8 dBm Avg.

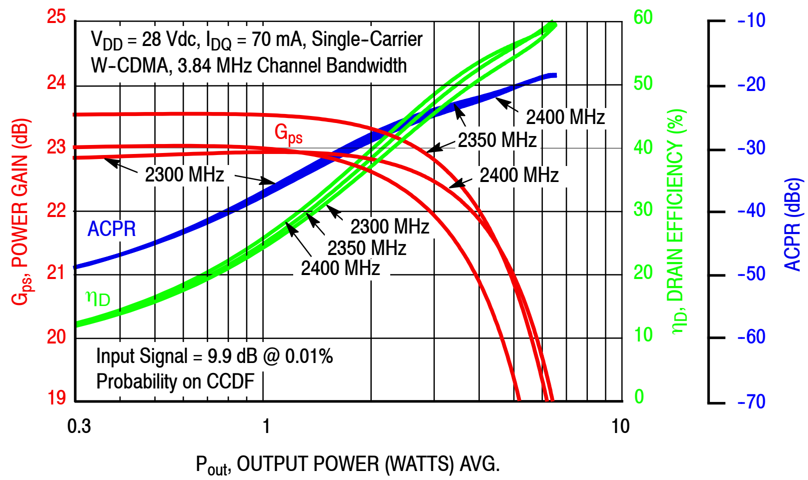


Figure 22. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

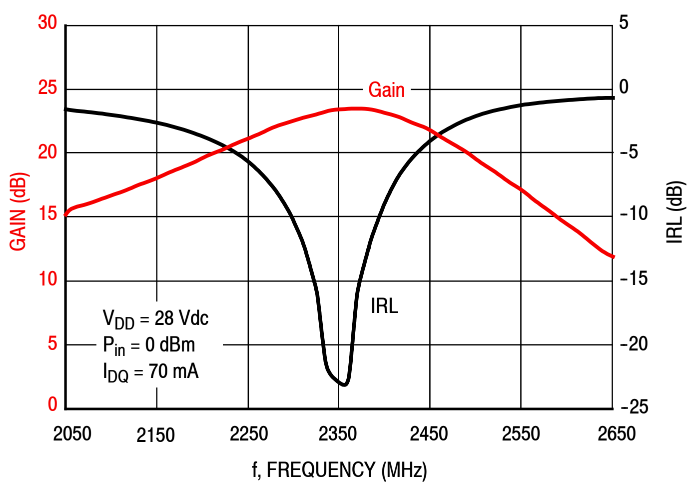


Figure 23. Broadband Frequency Response

Table 11. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 67 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 + j0.579	0.964 - j0.336	8.27 + j7.08	21.4	39.1	8	56.9	–14
2400	1.06 – j0.483	0.915 + j0.365	8.19 + j6.26	20.7	39.3	8	56.2	–15
2500	1.01 – j0.337	1.00 + j0.405	6.75 + j5.85	20.8	39.0	8	56.5	–14
2600	0.983 – j1.95	0.793 + j2.06	7.30 + j5.57	20.0	39.5	9	57.6	–16
2690	1.47 – j1.30	1.32 + j1.75	6.16 + j5.48	20.1	39.1	8	58.9	–11

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 + j0.579	0.908 - j0.0973	10.0 + j6.49	19.0	39.9	10	56.0	–20
2400	1.06 – j0.483	0.831 + j0.588	9.48 + j5.93	18.5	40.0	10	55.6	–22
2500	1.01 – j0.337	1.05 + j0.711	8.55 + j5.79	18.6	39.9	10	57.3	–21
2600	0.983 – j1.95	0.633 + j2.21	8.30 + j5.44	17.9	40.2	10	57.5	–23
2690	1.47 – j1.30	1.40 + j2.16	7.60 + j5.25	17.8	40.0	10	58.8	–17

(1) Load impedance for optimum P1dB power. (2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

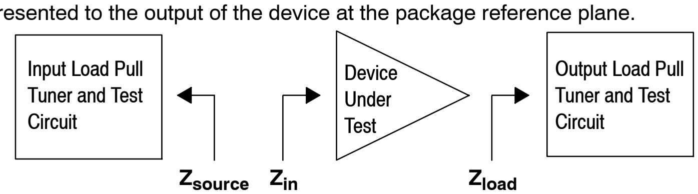
Table 12. Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 67 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 + j0.579	0.833 – j0.40	5.09 + j10.3	23.4	37.6	6	63.8	–20
2400	1.06 – j0.483	0.805 + j0.29	5.09 + j9.23	22.5	38.0	6	62.8	–22
2500	1.01 – j0.337	0.835 + j0.341	4.51 + j8.31	22.6	37.9	6	63.1	–19
2600	0.983 – j1.95	0.755 + j1.96	4.88 + j7.74	21.3	38.7	7	63.3	–21
2690	1.47 – j1.30	1.08 + j1.64	4.12 + j7.31	21.7	38.2	7	64.6	–17

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2300	1.12 + j0.579	0.807 – j0.161	5.41 + j10.0	21.1	38.5	7	63.2	–29
2400	1.06 – j0.483	0.77 + j0.525	6.38 + j9.17	20.2	39.1	8	61.6	–26
2500	1.01 – j0.337	0.921 + j0.637	5.16 + j8.53	20.5	38.8	8	63.4	–27
2600	0.983 – j1.95	0.608 + j2.13	5.61 + j7.84	19.3	39.4	9	62.7	–28
2690	1.47 – j1.30	1.18 + j2.01	4.38 + j7.31	19.6	38.8	8	64.8	–25

(1) Load impedance for optimum P1dB efficiency. (2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 2500 MHz

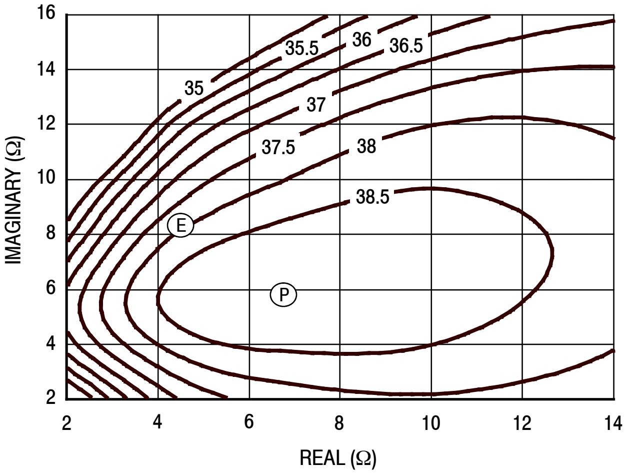


Figure 24. P1dB Load Pull Output Power Contours (dBm)

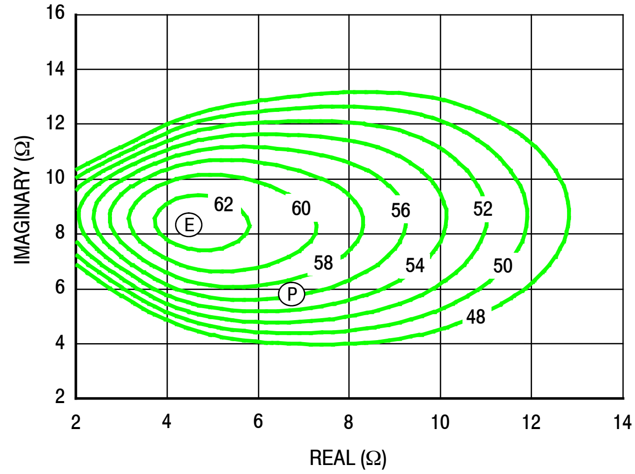


Figure 25. P1dB Load Pull Efficiency Contours (%)

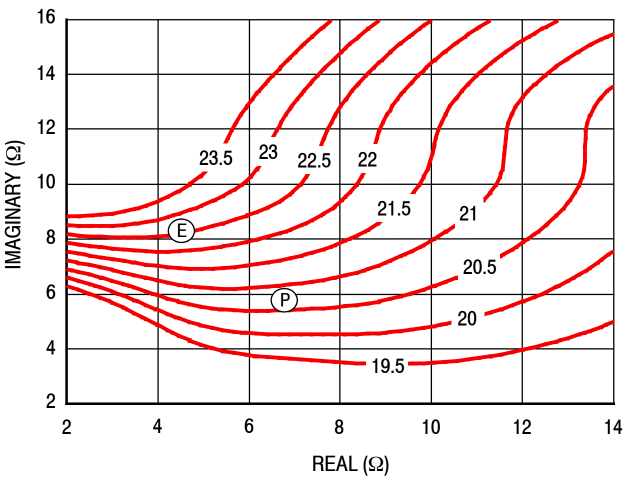


Figure 26. P1dB Load Pull Gain Contours (dB)

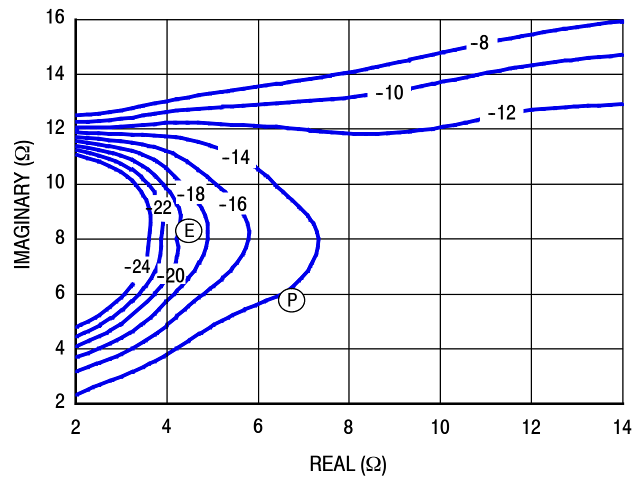


Figure 27. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2500 MHz

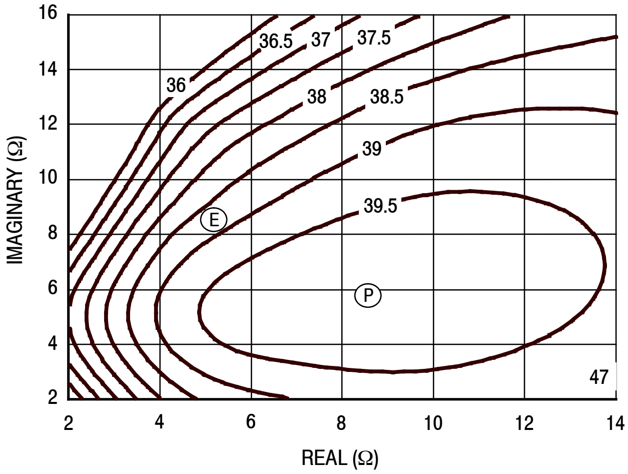


Figure 28. P3dB Load Pull Output Power Contours (dBm)

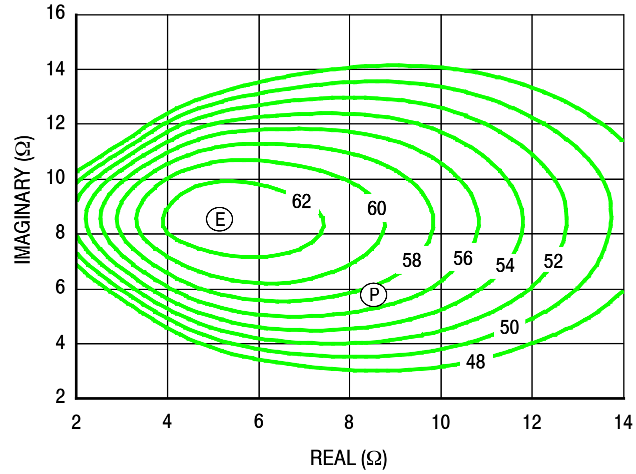


Figure 29. P3dB Load Pull Efficiency Contours (%)

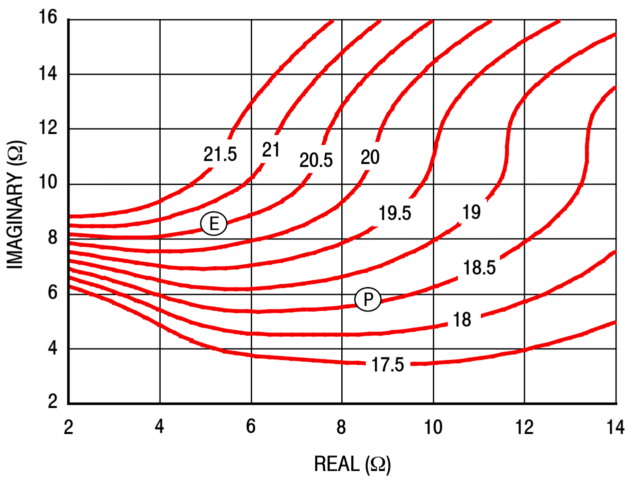


Figure 30. P3dB Load Pull Gain Contours (dB)

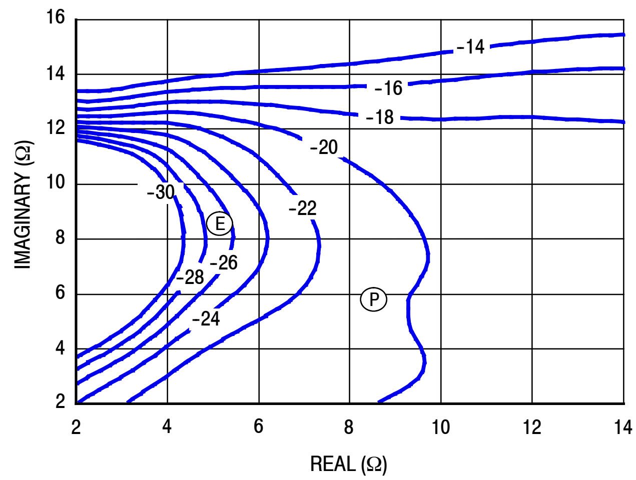


Figure 31. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

TYPICAL CHARACTERISTICS — 3400–3600 MHz

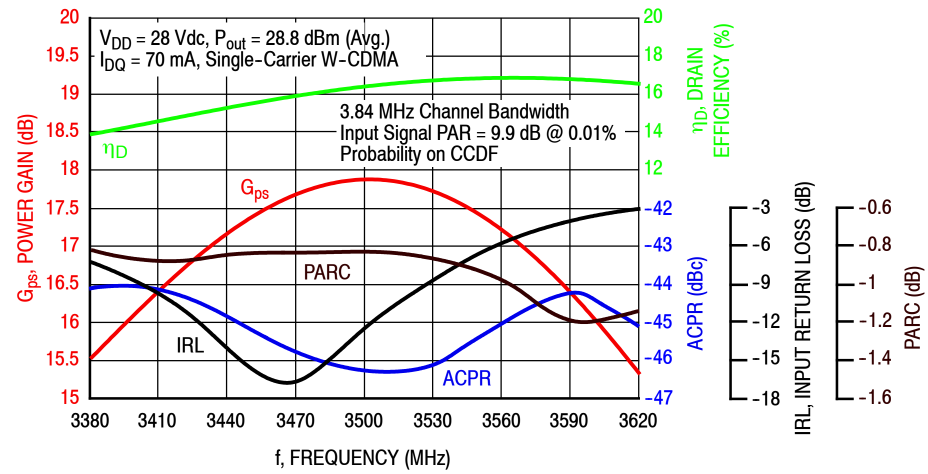


Figure 32. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28.8 dBm Avg.

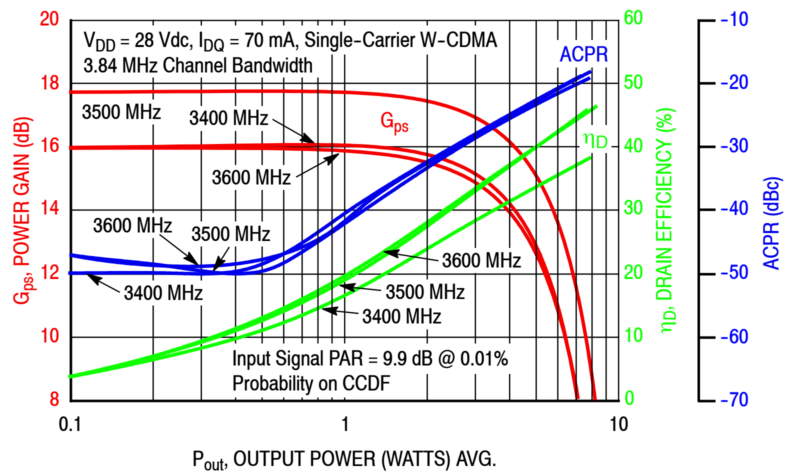


Figure 33. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

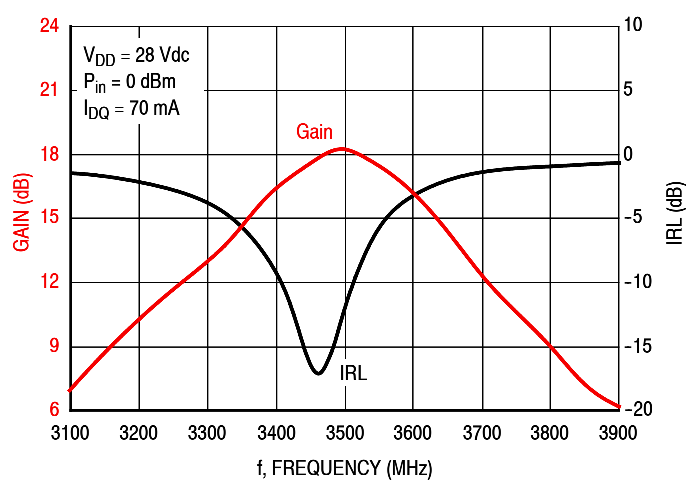
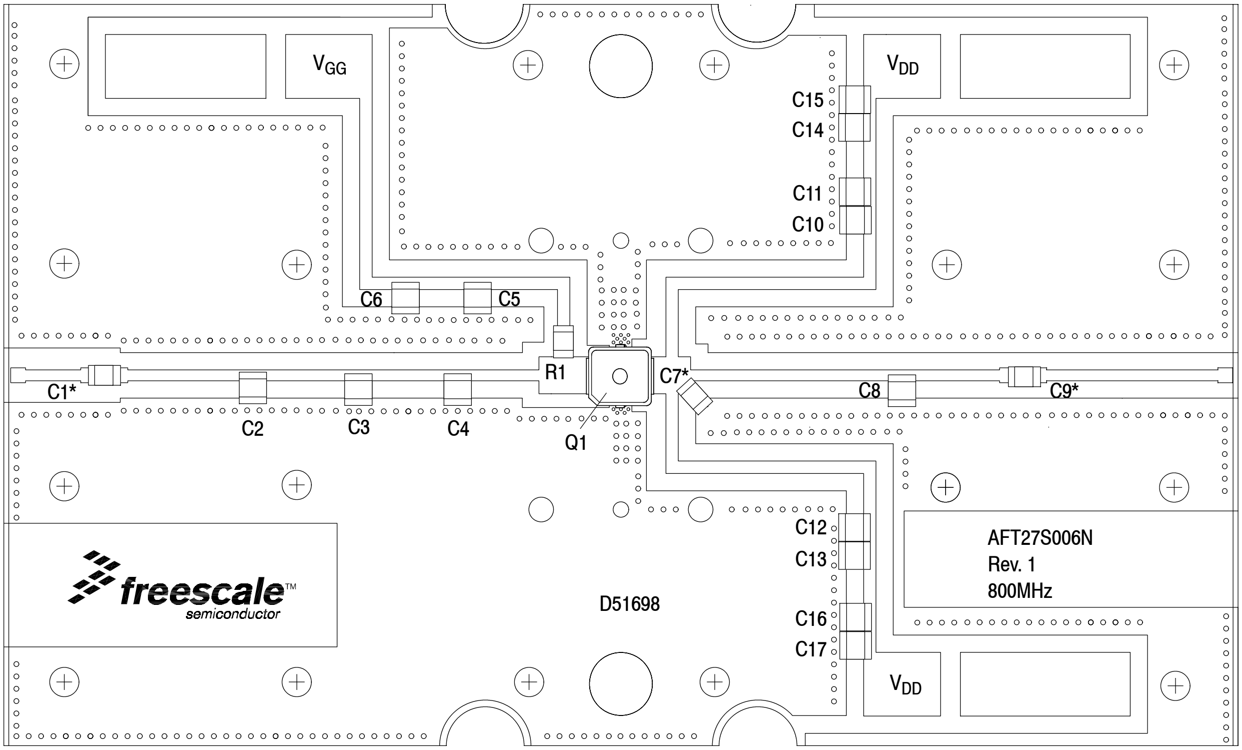


Figure 34. Broadband Frequency Response

728-768 MHz



*C1, C7 and C9 are mounted vertically.

NOTE: All data measured in fixture with device soldered to heatsink.

Figure 35. AFT27S006NT1 Test Circuit Component Layout — 728-768 MHz

Table 13. AFT27S006NT1 Test Circuit Component Designations and Values — 728-768 MHz

Part	Description	Part Number	Manufacturer
C5, C10, C11, C12, C13	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C2	4.7 pF Chip Capacitor	ATC100B4R7JT500XT	ATC
C3	6.8 pF Chip Capacitor	ATC100B6R8JT500XT	ATC
C4, C7	3.9 pF Chip Capacitors	ATC100B3R9JT500XT	ATC
C1, C9	82 pF Chip Capacitors	ATC100B820JT500XT	ATC
C8	0.5 pF Chip Capacitor	ATC100B0R5JT500XT	ATC
C6, C14, C15, C16, C17	10 μF Chip Capacitors	GRM32ER61H106KA12L	Murata
Q1	RF Power LDMOS Transistor	AFT27S006NT1	Freescale
R1	10 Ω, 1/4 W Chip Resistor	CRCW120610R0JNEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D51698	MTL

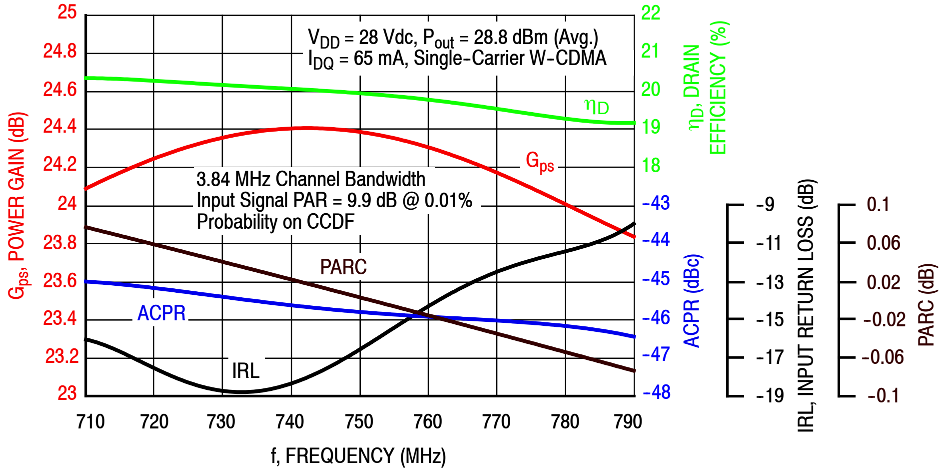


Figure 36. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28.8 dBm Avg.

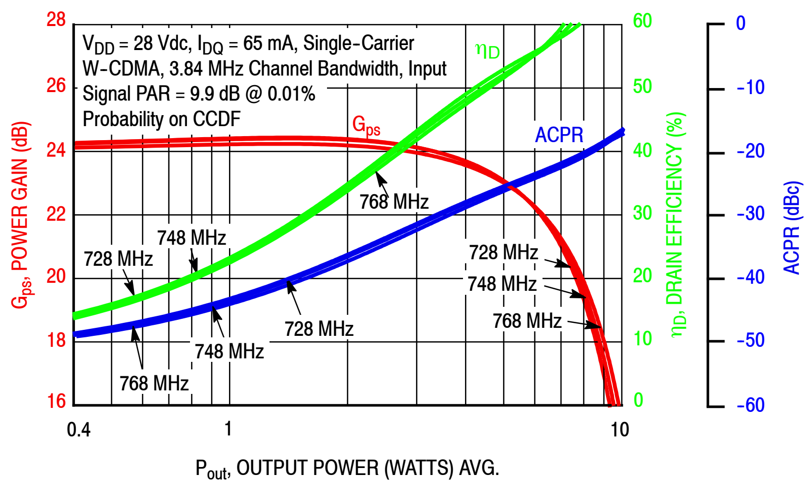


Figure 37. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

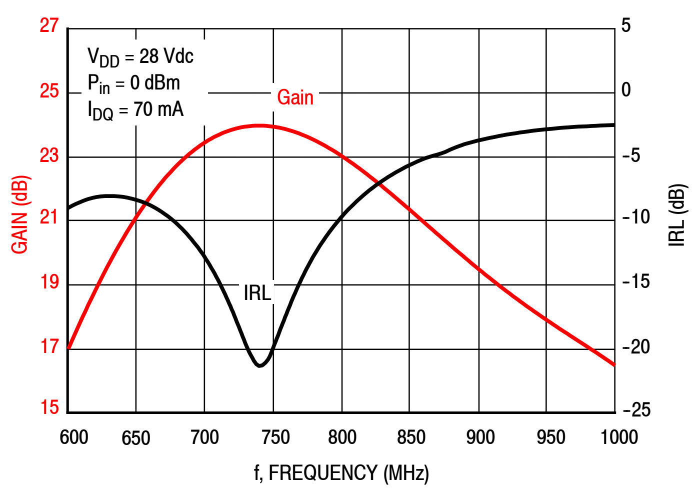


Figure 38. Broadband Frequency Response

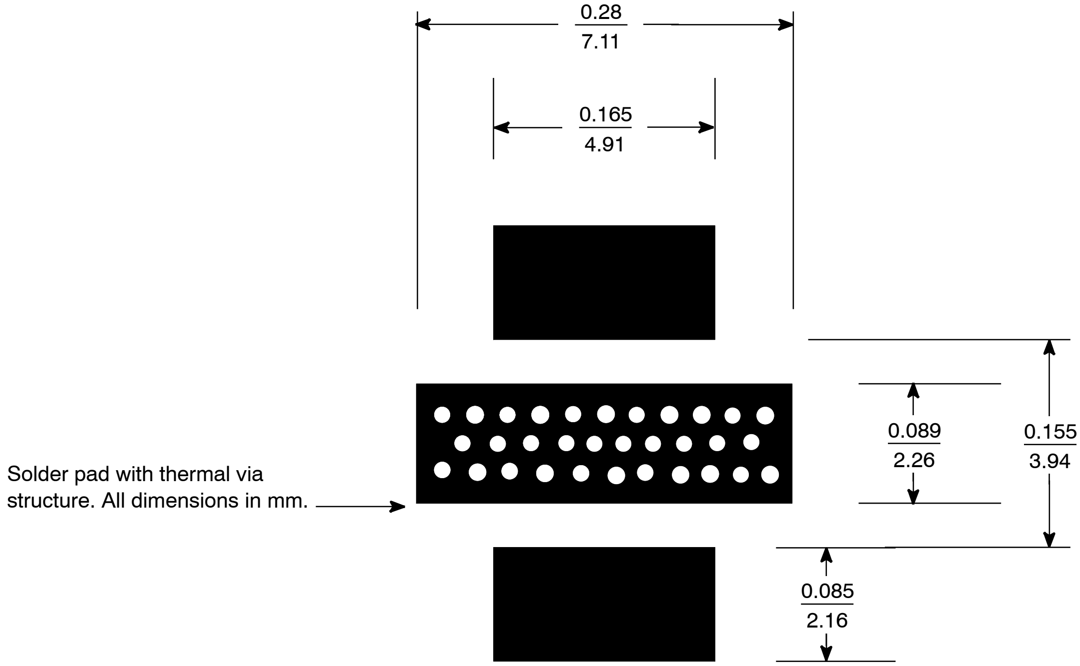


Figure 39. PCB Pad Layout for PLD-1.5W

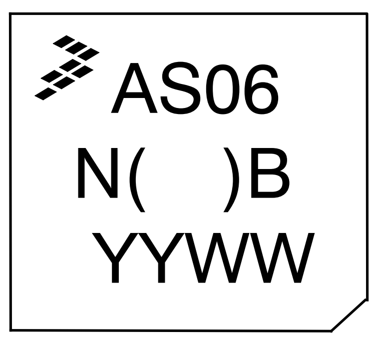
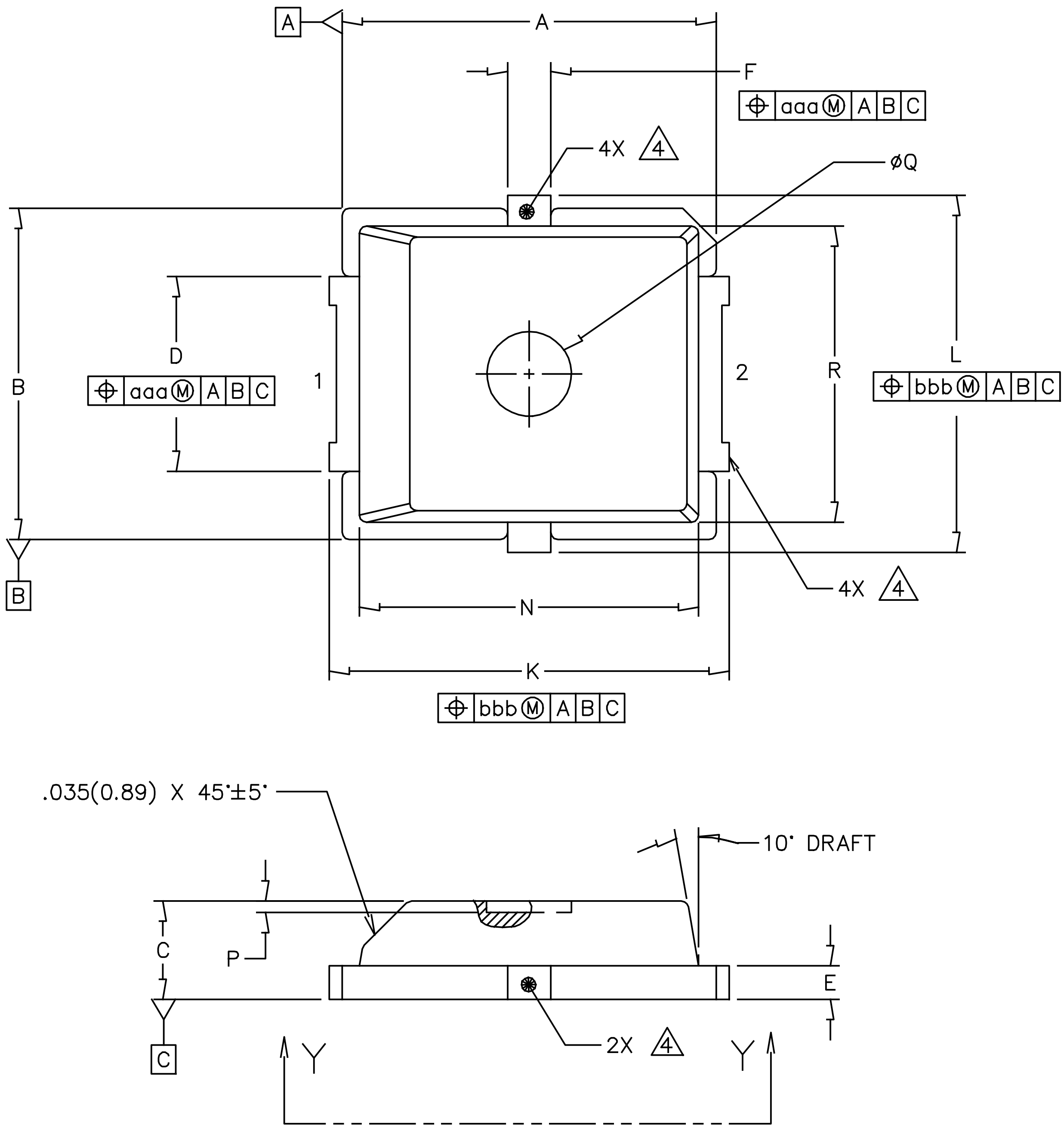
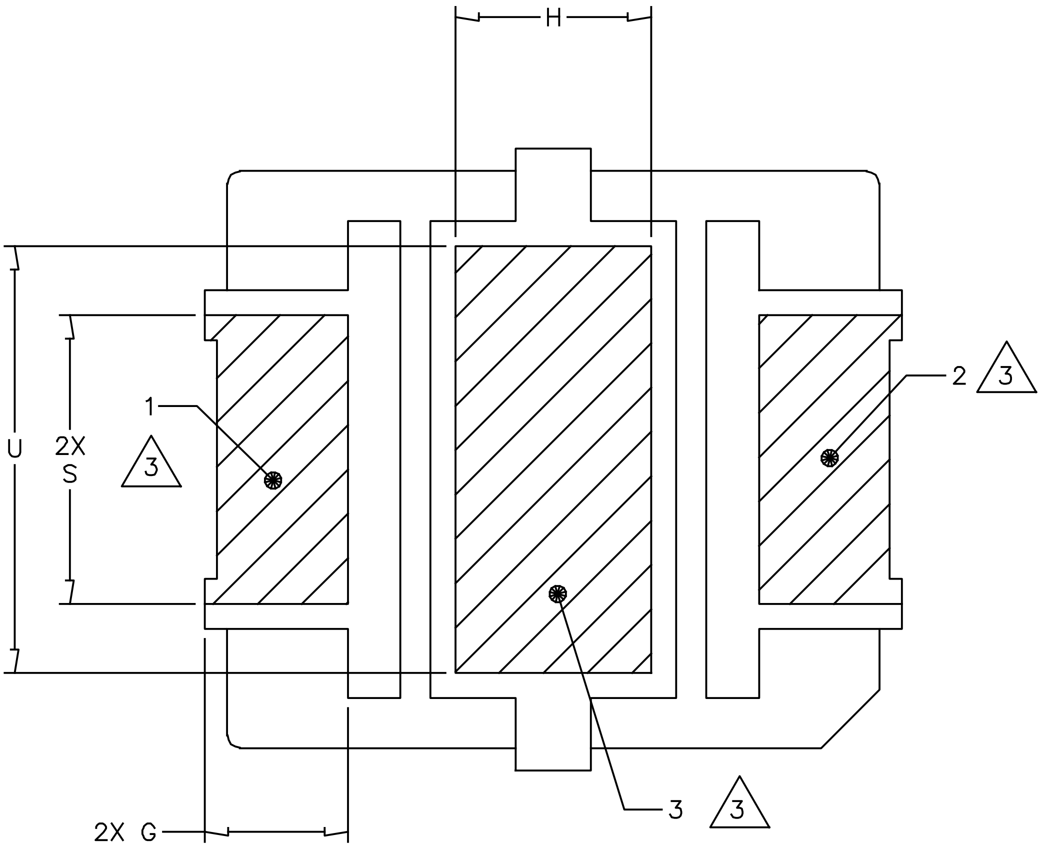


Figure 40. Product Marking

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE
TITLE: PLD–1.5W		DOCUMENT NO: 98ASA00476D	REV: O
		CASE NUMBER: 2297–01	14 JUN 2012
		STANDARD: NON–JEDEC	



VIEW Y–Y

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PLD–1.5W		DOCUMENT NO: 98ASA00476D	REV: 0
		CASE NUMBER: 2297–01	14 JUN 2012
		STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA. DIMENSIONS G, S, H AND U REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA.

4. THESE SURFACES ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.255	.265	6.48	6.73	Q	.055	.063	1.40	1.60
B	.225	.235	5.72	5.97	R	.200	.210	5.08	5.33
C	.065	.072	1.65	1.83	S	.110	—	2.79	—
D	.130	.150	3.30	3.81	U	.156	—	3.96	—
E	.021	.026	0.53	0.66	aaa	.004		0.10	
F	.026	.044	0.66	1.12	bbb	.005		0.13	
G	.038	—	0.97	—					
H	.069	—	1.75	—					
J	.160	.180	4.06	4.57					
K	.273	.285	6.93	7.24					
L	.245	.255	6.22	6.48					
N	.230	.240	5.84	6.10					
P	.000	.008	0.00	0.20					

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: PLD−1.5W	DOCUMENT NO: 98ASA00476D	REV: 0
	CASE NUMBER: 2297−01	14 JUN 2012
	STANDARD: NON−JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to Software & Tools on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2013	• Initial Release of Data Sheet
1	Nov. 2013	• Table 5, Functional Tests table: gain min and max limits improved and typical values updated to reflect large volume production data, p. 3 • Tables 6, 7, 8, 9, Test Circuit Component Designations and Values: updated PCB description to reflect most current board specifications from Rogers, pp. 4, 10, 12, 17
2	Sept. 2014	• Tape and Reel information: corrected tape width information from 13-inch reel to 7-inch reel to reflect actual reel size, p. 1 • Changed operating frequency from 728–2700 MHz to 728–3600 MHz due to expanded device frequency capability resulting from additional test data, p. 1
3	Nov. 2014	• Added 3400-3600 MHz performance information as follows: - Typical Frequency Band table, p. 1 - Fig. 32, Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 28.8 dBm Avg., p. 17 - Fig. 33, Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power, p. 17 - Fig. 34, Broadband Frequency Response, p. 17

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AFT27S006N
Rev. 3, 11/2014